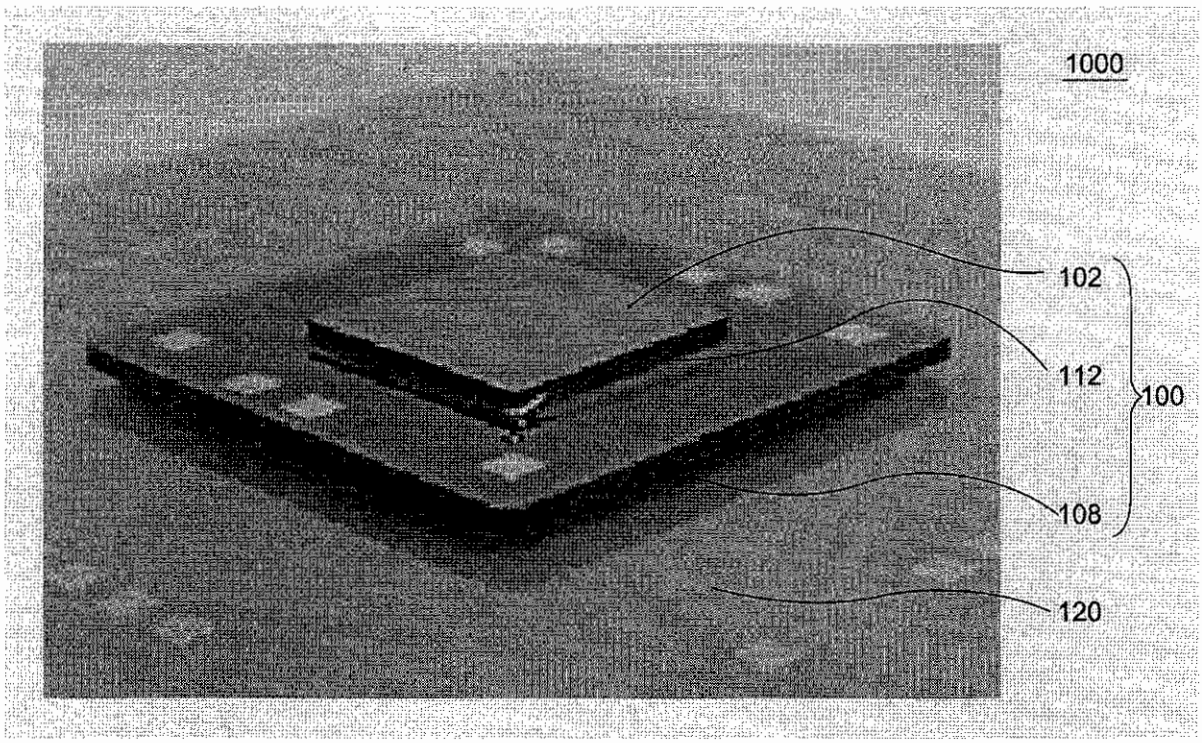
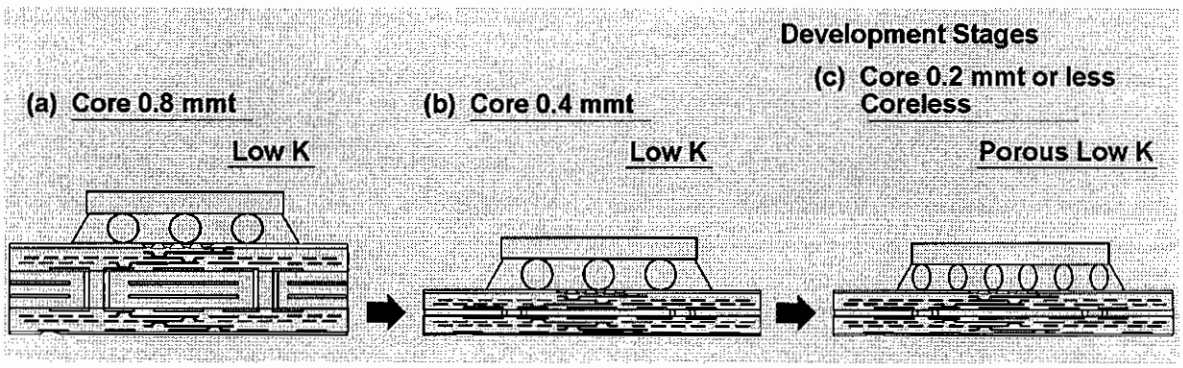
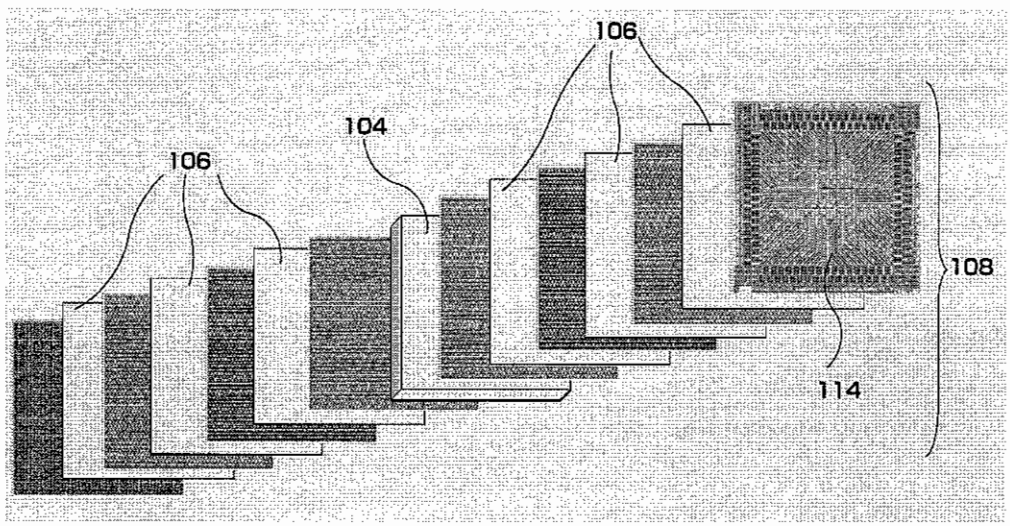
[Fig. 1]


1000
102
112
100
108
120

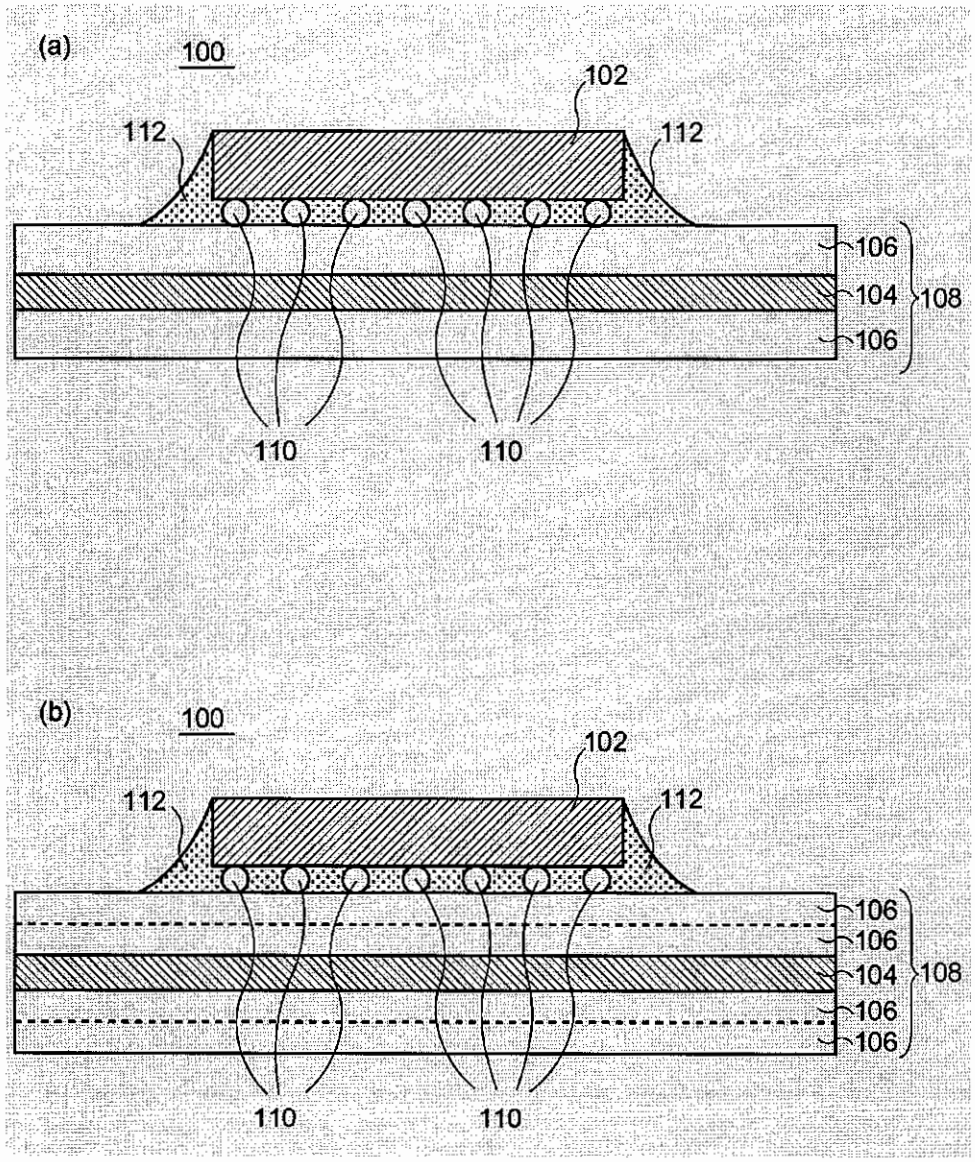
[Fig. 2]


Development Stages
(a) Core 0.8 mmt
Low K
(b) Core 0.4 mmt
Low K
(c) Core 0.2 mmt or less
Coreless
Porous Low K

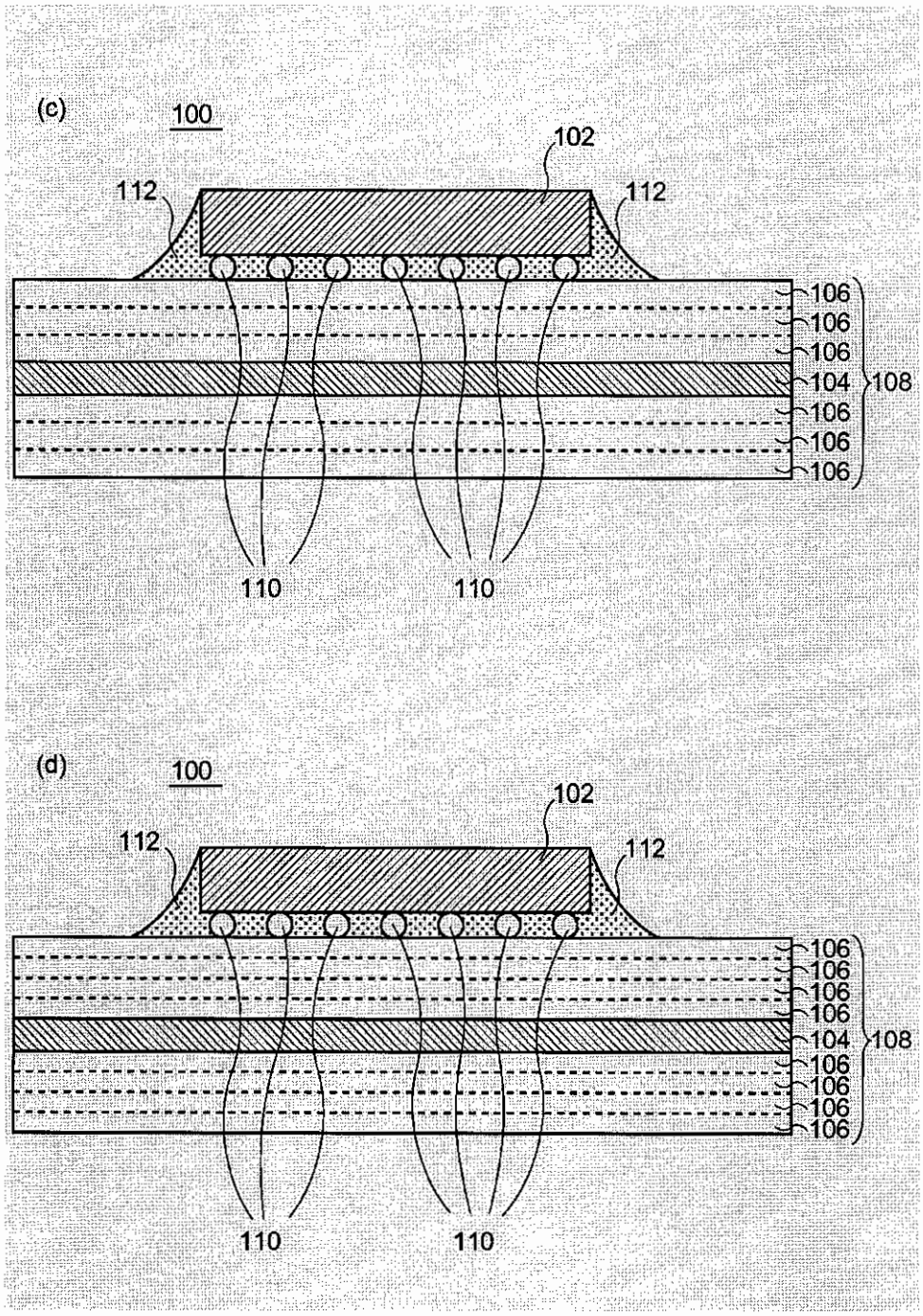
[Fig. 3]



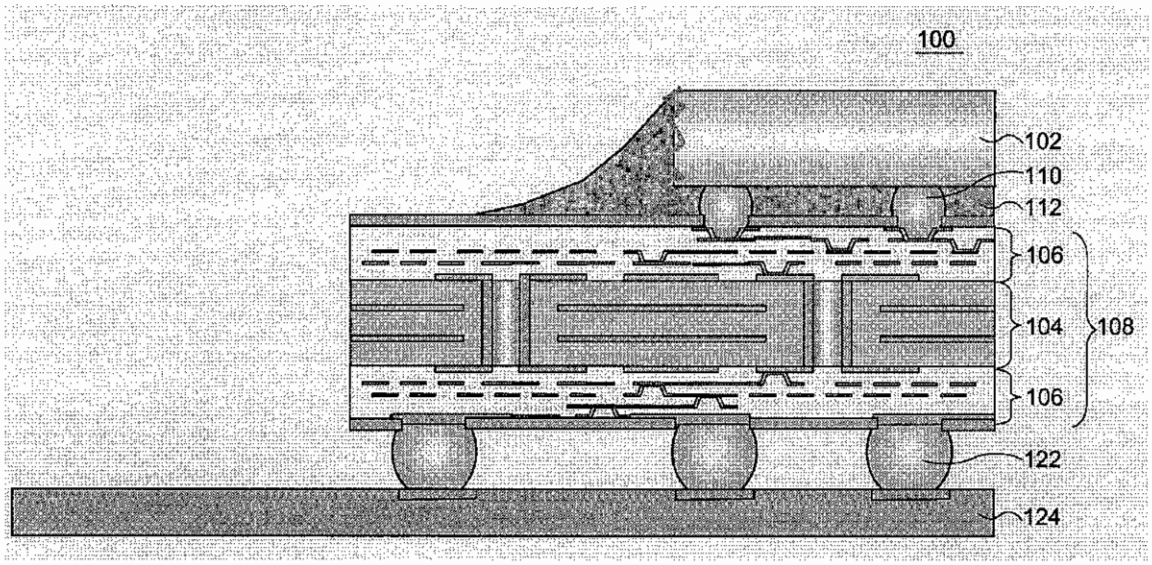
[Fig. 4]


(a)
100
102
112
112
106
104
108
106
110
110
(b)
100
102
112
112
106
106
104
108
106
106
110
110

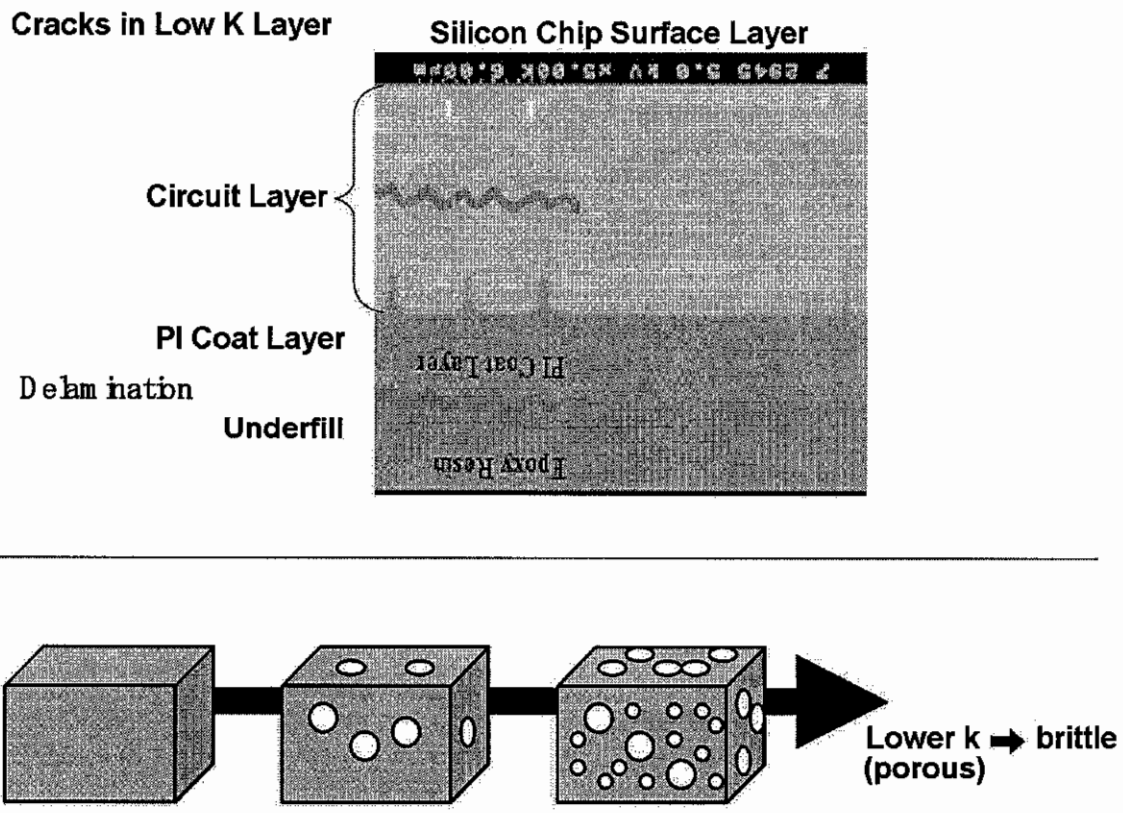
[Fig. 5]


(c)
100
102
112
112
106
106
106
104
108
106
106
106
110
110
(d)
100
102
112
112
106
106
106
106
104
108
106
106
106
106
110
110

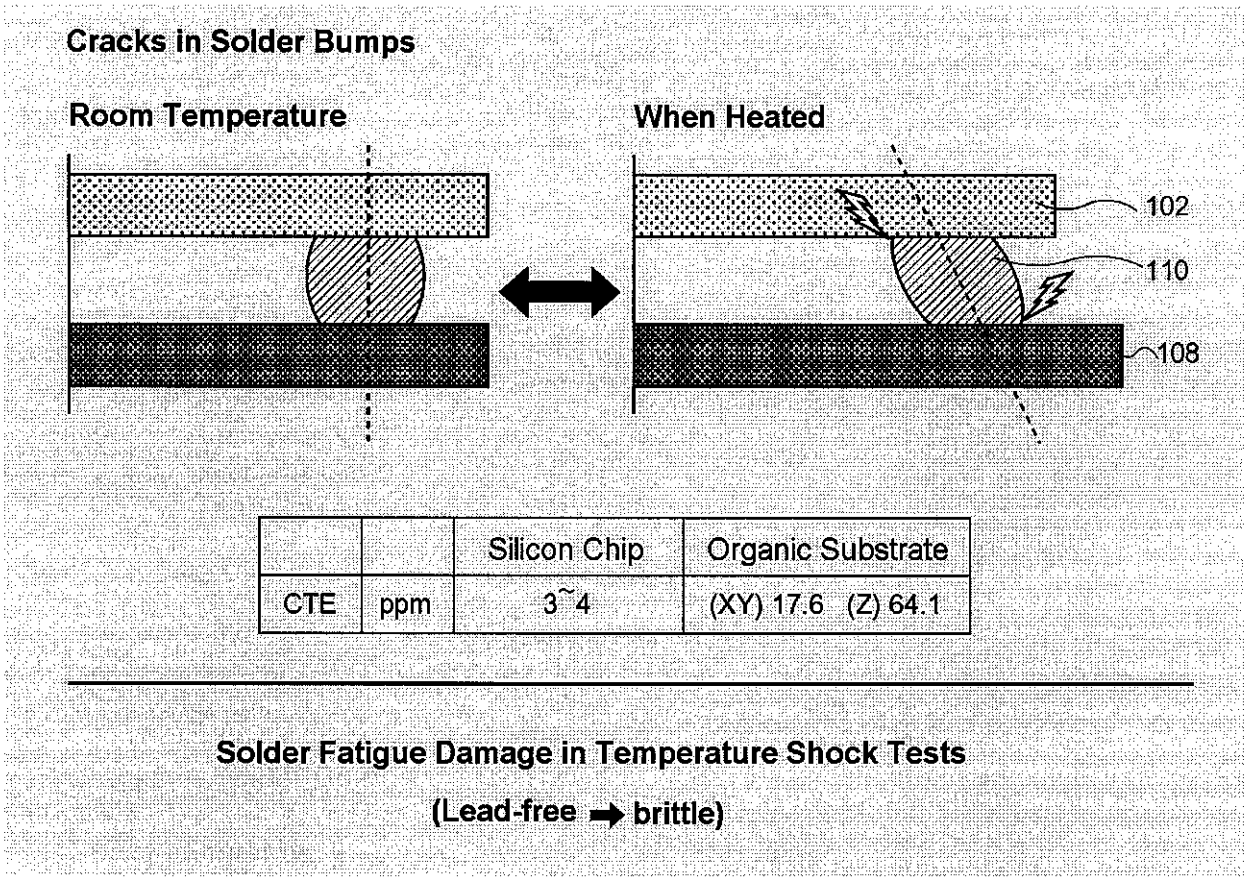
[Fig. 6]


100
102
110
112
106
104
108
106
122
124

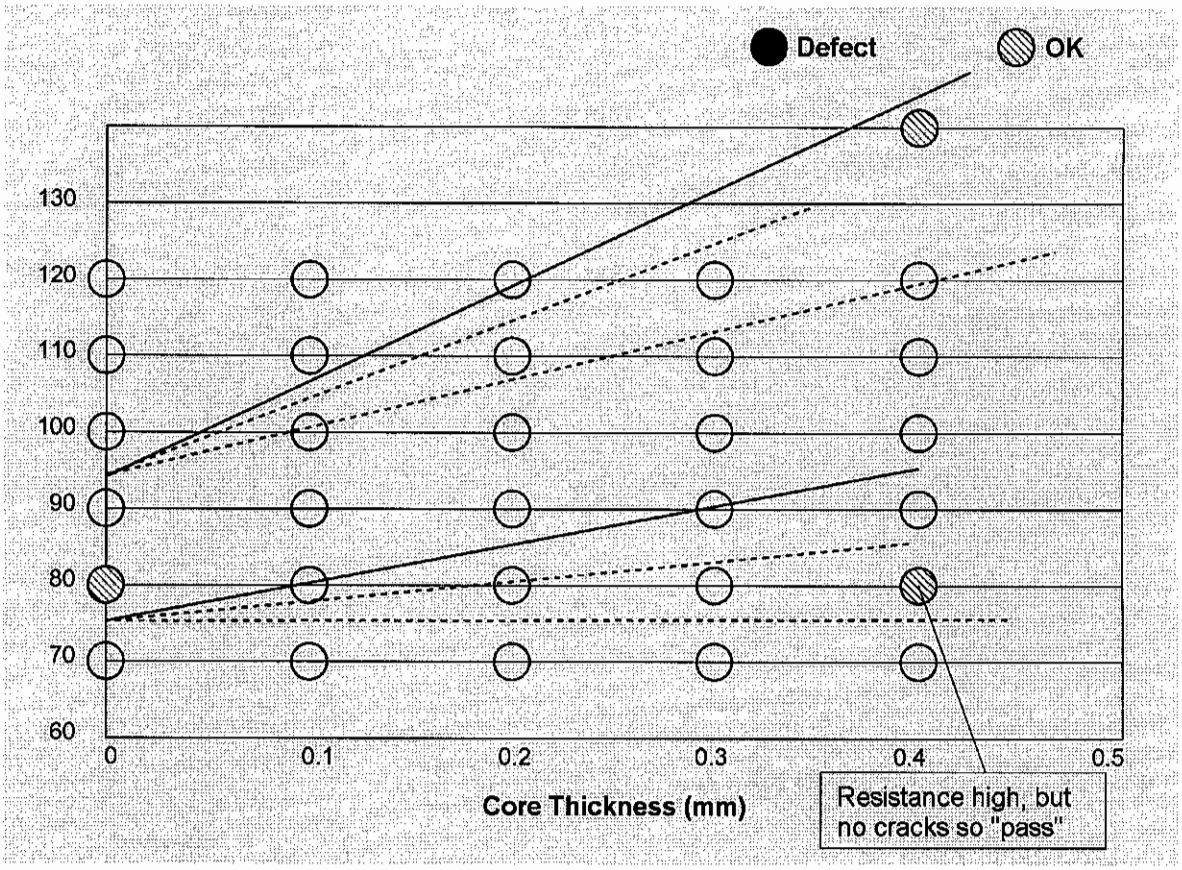
[Fig. 7]


Cracks in Low K Layer
Silicon Chip Surface Layer
Circuit Layer
PI Coat Layer
Delamination
Underfill
Lower k ➡ brittle
(porous)

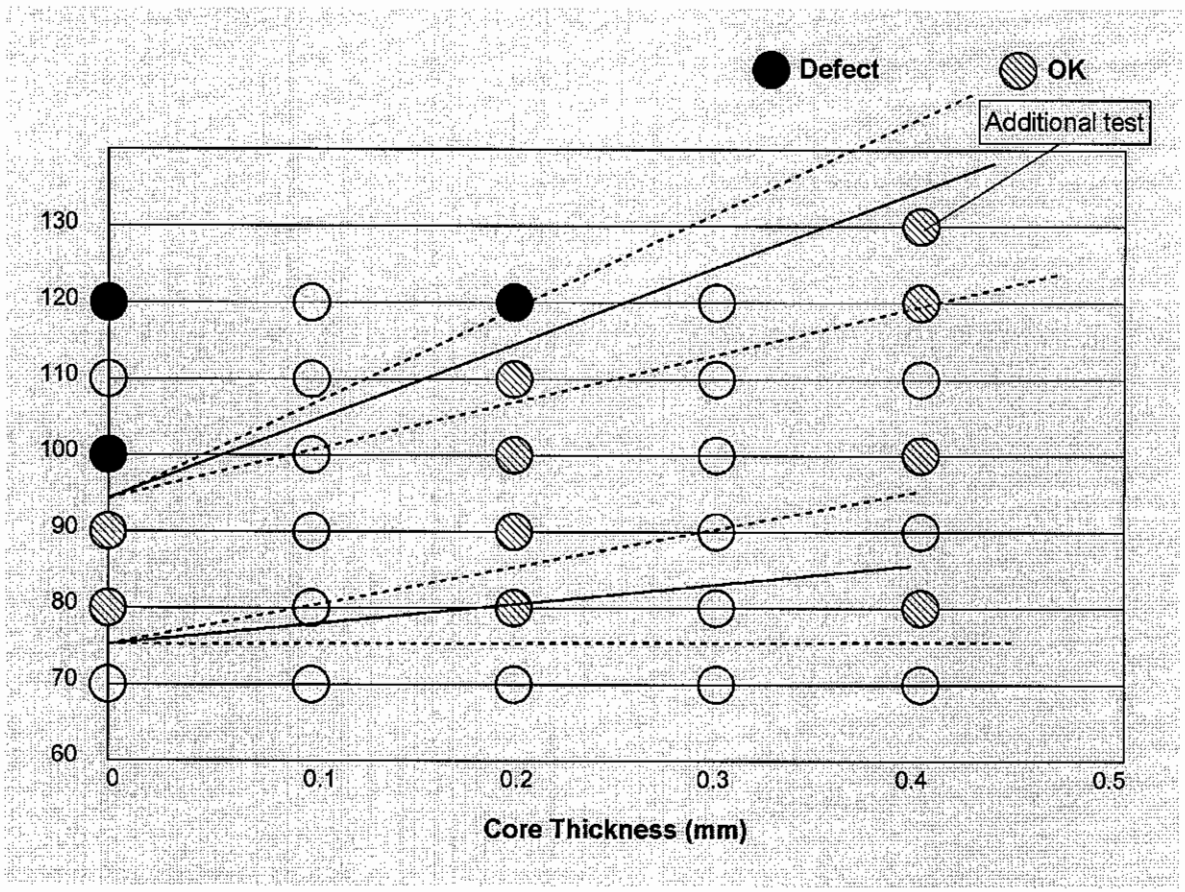
[Fig. 8]


Cracks in Solder Bumps
Room Temperature
When Heated
102
110
108
Silicon Chip
Organic Substrate
CTE
ppm
3~4
(XY) 17.6 (Z) 64.1
Solder Fatigue Damage in Temperature Shock Tests
(Lead-free ➡ brittle)

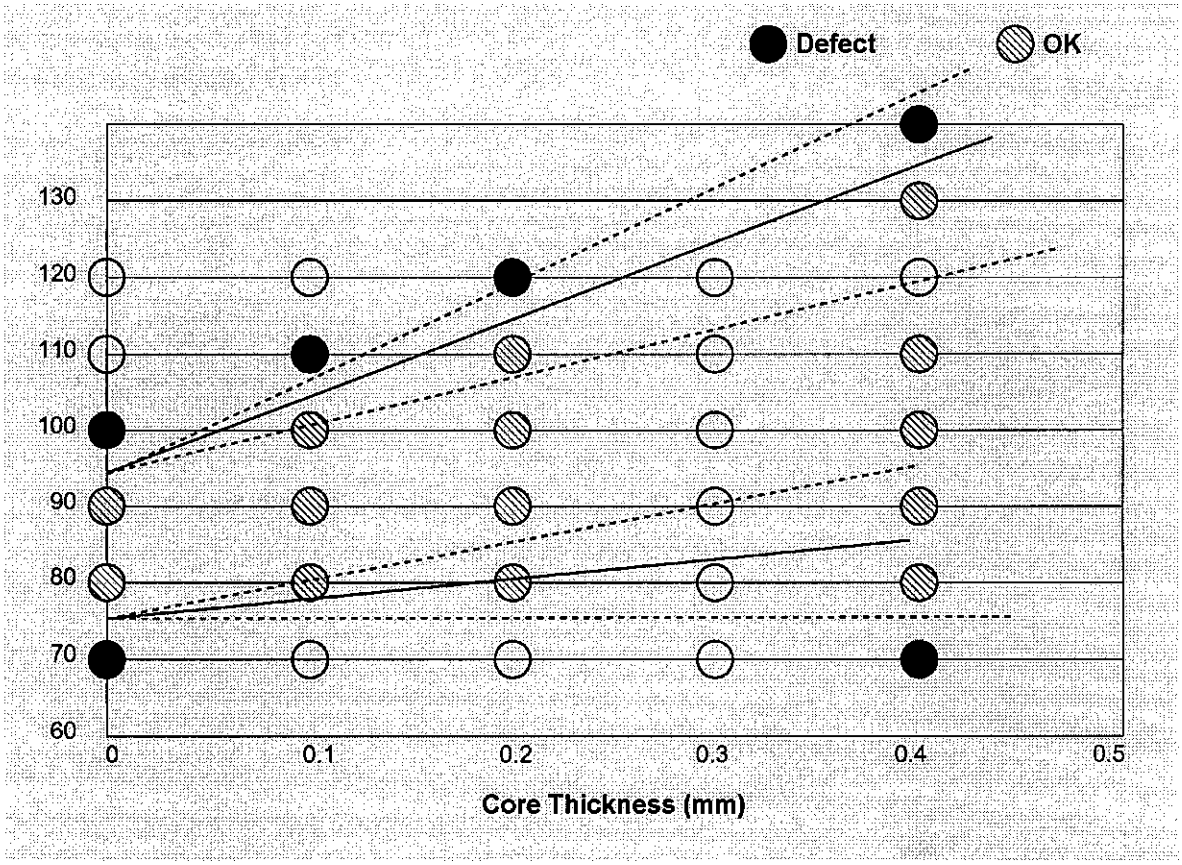
[Fig. 9]


Defect
OK
130
120
110
100
90
80
70
60
0
0.1
0.2
0.3
0.4
0.5
Core Thickness (mm)
Resistance high, but no cracks so "pass"

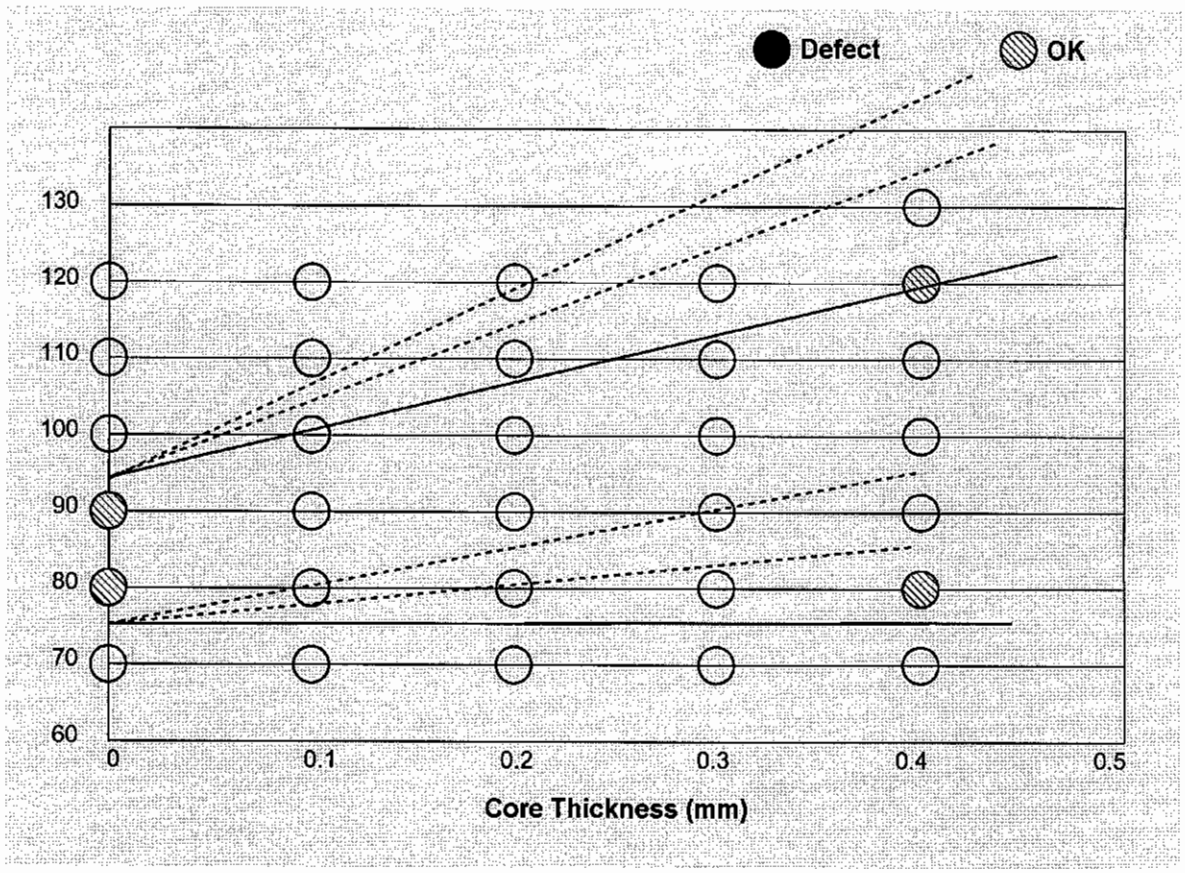
[Fig. 10]


Defect
OK
Additional test
130
120
110
100
90
80
70
60
0
0.1
0.2
0.3
0.4
0.5
Core Thickness (mm)

[Fig. 11]


Defect
OK
130
120
110
100
90
80
70
60
0
0.1
0.2
0.3
0.4
0.5
Core Thickness (mm)

[Fig. 12]


Defect
OK
130
120
110
100
90
80
70
60
0
0.1
0.2
0.3
0.4
0.5
Core Thickness (mm)