CLAIMS

1. A method for improved linearity of a phase change memory (PCM) cell structure, the method comprising:

forming a bottom electrode over a substrate;

forming a heating element in direct contact with a top surface of the bottom electrode;

forming a resistive liner defining a planar surface across its entire length, such that the planar resistive liner surface extends, in its entirety, above a top surface of the heating element;

constructing a PCM stack including a plurality of PCM layers each having a different crystallization temperature over the bottom electrode, the PCM stack directly contacting a top surface of the resistive liner; and

forming a top electrode over the PCM stack,

wherein the crystallization temperature varies in an ascending order from the bottom electrode to the top electrode.

2. The method of claim 1, wherein each of the plurality of PCM layers includes a Ge—Sb—Te (germanium-antimony-tellurium or “GST”) alloy.

3. The method of claim 1, wherein the plurality of PCM layers includes four layers.

4. The method of claim 3, wherein the first layer includes germanium (Ge) content of less than 20%, the second layer includes Ge content of between 20-40%, the third layer includes Ge content of between 40-70%, and the fourth layer includes Ge content of greater than 60%.

5. The method of claim 1, wherein a width of the heating element is less than a width of the bottom electrode.

6. The method of claim 5, wherein the resistive liner is employed for resistance drift correction.

7. The method of claim 1, wherein the different crystallization temperatures are achieved by doping and/or different material content.

8. A semiconductor structure comprising:

a bottom electrode disposed over a substrate;

a heating element disposed in direct contact with a top surface of the bottom electrode;

a resistive liner defining a planar surface across its entire length, such that the planar resistive liner

surface extends, in its entirety, above a top surface of the heating element;

a phase change memory (PCM) stack including a plurality of PCM layers each having a different crystallization temperature disposed over the bottom electrode, the PCM stack directly contacting a top surface of the resistive liner; and

a top electrode disposed over the PCM stack,

wherein the crystallization temperature varies in a descending order within a portion or an entirety of the PCM stack.

9. The semiconductor structure of claim 8, wherein each of the plurality of PCM layers includes a Ge—Sb—Te (germanium-antimony-tellurium or “GST”) alloy.

10. The semiconductor structure of claim 8, wherein the different crystallization temperatures are achieved by doping and/or different material content.

11. The semiconductor structure of claim 8, wherein a first layer of the PCM stack includes germanium (Ge) content of less than 20%, a second layer of the PCM stack includes Ge content of between 20-40%, a third layer of the PCM stack includes Ge content of between 40-70%, and a fourth layer of the PCM stack includes Ge content of greater than 60%.

12. The semiconductor structure of claim 8, wherein the descending order is from the top electrode to the bottom electrode.

13. A semiconductor structure comprising:

a bottom electrode disposed over a substrate;

a heating element disposed in direct contact with a top surface of the bottom electrode;

a resistive liner defining a planar surface across its entire length, such that the planar resistive liner surface extends, in its entirety, above a top surface of the heating element;

a phase change memory (PCM) stack including a plurality of PCM layers each having a different crystallization temperature disposed over the bottom electrode, wherein each of the plurality of PCM layers includes a Ge—Sb—Te (germanium-antimony-tellurium or “GST”) alloy, the PCM stack directly contacting a top surface of the resistive liner; and

a top electrode disposed over the PCM stack,

wherein the crystallization temperature varies in an ascending order from the bottom electrode to the top electrode.