Abstract

METHOD FOR PLANARIZING LOCAL INTERCONNECTS

A method for planarizing metal plugs for device interconnections. The process begins by providing a semiconductor structure with at least one device thereon. A dielectric layer is formed over the device and the semiconductor structure. A first barrier metal layer is formed on the dielectric layer, and a sacrificial oxide layer is formed on the first barrier metal layer. The sacrificial oxide layer, the first barrier metal layer, and the dielectric layer are patterned to form contact openings. A second barrier metal layer is formed over the semiconductor structure, and a metal contact layer is formed on the second barrier metal layer. The metal contact layer and the second barrier metal layer are planarized using a first chemical mechanical polishing process and the sacrificial oxide layer is removed. The metal contact layer and the first barrier metal layer are planarized using a second chemical mechanical polishing process.

(FIGURE 3 IS SUGGESTED FOR PUBLICATION)