

【ABSTRACT】

A smart IC substrate according to an embodiment includes a substrate including a first surface and a second surface opposite the first surface; a bonding layer disposed on the first surface; a buffer layer disposed on the bonding layer; a metal layer disposed on the buffer layer; and a plating layer disposed on a lower surface of the metal layer, wherein the metal layer includes an alloy including nickel (Ni), iron (Fe), and chromium (Cr), wherein the buffer layer includes a first buffer layer a second buffer layer, wherein the first buffer layer is disposed between the second buffer layer and the metal layer, wherein the second buffer layer comprises a second-first buffer layer and a second-second buffer layer, wherein the second-first buffer layer is disposed between the first buffer layer and the second-second buffer layer, and wherein a surface roughness of the second-second buffer layer is greater than a surface roughness of the second-first buffer layer.