SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of priority of application Serial Number 177864/1996, filed July 8, 1996 in Japan, the subject matter of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the invention:

The present invention relates to a semiconductor device, particularly to a layout of a power field effect transistor (FET).

Description of the Related Art:

In a conventional semiconductor device, a high power FET and a medium power FET are respectively fabricated as a single-chip discrete device. These are connected together on a circuit substrate. Gate widths of these FETs vary based on utilized frequencies and power supplies. For example, in 900MHz cellar phones, gate widths of the high power FETs are about 10 mm and gate widths of the medium power FETs are about 3 mm. A gate width usually differs between respective FETs .

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Fig. 4(a) is a plane view showing a high power FET in accordance with the prior art.

Fig. 4(b) is a plane view showing a medium power FET having the same gate width, in accordance with the prior art.

Referring to Fig. 4(a), the high power FET comprises a plurality of source pads S41-S44, a plurality of gate pads G41-G43, a plurality of drain pads D41-D44, and a plurality of gates F41, formed on a semiconductor chip C41. An array has the source pads S41-S44 and the gate pads G41-G43 alternately arranged, and they are separated from the drain pads D41-D44, by the gates F41. A gate width of the gates F41 set to L41.

Referring to Fig. 4(b), the medium power FET comprises a plurality of source pads S47, S48, a gate pad G45, a plurality of drain pads D47, D48, and a plurality of gates F42, formed on a semiconductor chip C43. An array has the source pads S47, S48 and the gate pad G45 arranged alternately, and they are separated from the drain pads D47, D48, by the gates F41. A gate width of the gates F42 set L42 shorter than L41.

Since the high power FET and the medium power FET, in accordance with the prior art, have respectively different gate widths, a pinch off voltage(Vp) of each FETs is also respectively different when an implantation condition and a recess condition for forming the conducting layers of the FETs are the same.

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SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device that is able to have the same Vp in all of FETs formed on one chip, to make it easy to control a process, and to make it easy to construct a control circuit of the FETs.

According to one aspect of the present invention, for achieving the above object, there is provided a semiconductor device, comprising:

a semiconductor substrate having a first region and a second region on a main surface;

a first field effect transistor formed on the main surface of the first region, the first field effect transistor having first gates arranged in a plurality of rows and having a first total gate width, the first gates respectively establishing a first gate length and a first gate width; and

a second field effect transistor formed on the main surface of the second region, the second field effect transistor having second gates arranged a plurality of rows and having a second total gate width smaller than the first total gate width, the second gates respectively establishing a second gate length substantially the same as the first gate length and a second gate width substantially same as the first gate width,.

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According to another aspect of the present invention, for achieving the above object, there is provided a semiconductor device further comprising:

a first plurality of source pads and a first plurality of gate pads commonly connecting between first gates at one side and formed on the main surface close to the commonly connecting portion;

a first plurality of drain pads arranged opposite to the first plurality of source pads and the first plurality of gate pads and formed on the main surface through the first gates;

a second plurality of source pads and a second plurality of gate pads commonly connecting between second gates at one side and formed on the main surface close to the commonly connecting portion; and

a second plurality of drain pads arranged opposite to the second plurality of source pads and the second plurality of gate pads and formed on the main surface through the second gates.

According to one aspect of the present invention, for achieving the above object, there is provided a semiconductor device, wherein the source pad, among the first plurality source pads, that is closest to the second plurality of drain pads, is electrically connected the source pad, among the second plurality of source pads, that is closest to the second plurality of drain pads.

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BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter that is regarded as the invention, the invention, along with the objects, features, and advantages thereof, will be better understood from the following description taken in connection with the accompanying drawings, in which:

Fig. 1 is a plane view showing a semiconductor device according to a first embodiment of the present invention.

Fig. 2 is a plane view showing a semiconductor device according to a second embodiment of the present invention.

Fig. 3 is a plane view showing a semiconductor device according to a third embodiment of the present invention.

Fig. 4 is a plane view showing power FETs in accordance with the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A. A first embodiment

A first embodiment of a semiconductor device according to the present invention will hereinafter be described in detail with reference to the accompanying drawings.

Fig. 1 is a plane view showing a semiconductor device according to a first embodiment of the present invention.

As shown in Figs. 1, the semiconductor device comprises

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a high power FET and a medium power FET. The high power FET and the medium power FET are formed on a semiconductor chip C1.

The high power FET comprises first gate-source pads having a plurality of source pads S11-S14 and a plurality of gate pads G11-G13, a plurality of drain pads D11-D14, and a plurality of gates F11 positioned between the first gate-source pads and the drain pads D11-D14, which are formed on a semiconductor chip C1. The source pads S11-S14 and the gate pads G11-G13 are alternately arranged on the semiconductor chip C1. The gates F11 have a gate width L11. The gates F11 are commonly connected at one end. The gates F11 form a comb like arrangement. The commonly connected end of the gates is opposite to the first gate-source pads.

Furthermore, the medium power FET comprises second gate-source pads having a plurality of source pads S15, S16 and a gate pad G14, a plurality of drain pads D15, D16, and a plurality of gates F12 positioned between the second gate-source pads and the drain pads D15, D16, which are formed on a semiconductor chip C1. The source pads S15, S16 and the gate pad G14 are alternately arranged on the semiconductor chip C1. The gates F11 have a gate width L12 which is the same as the gate width L11 of the gates F12. The gates F12 are commonly connected one end. The gates F12 form a comb type arrangement. The commonly connected portion of the gates is opposite to the second gate-source pads.

Furthermore, the high power FET and the medium power

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FET are separately arranged. The first gate-source pads, the source pads S15, S16 and the gate pad G14 are formed on one side of the semiconductor chip C1. The drain pads D11-D14 and D15, D16 are formed on the other side of the semiconductor chip C1.

Accordingly, a semiconductor device of the first embodiment of the present invention is able to have the same Vp in all of FETs formed on one-chip.

B. A second embodiment

Fig. 2 is a plane view showing a semiconductor device according to a second embodiment of the present invention.

As shown in Figs. 2, the semiconductor device comprises the high power FET and the medium power FET. The high power FET and the medium power FET are formed on a semiconductor chip C2.

The high power FET comprises first gate-source pads having a plurality of source pads S21-S24 and a plurality of gate pads G21-G23, a plurality of drain pads D21-D24, and a plurality of gates F21 positioned between the first gate-source pads and the drain pads D21-D24, which are formed on a semiconductor chip C2. The source pads S21-S24 and the gate pads G21-G23 are alternately arranged on the semiconductor chip C2. The gates F21 have a gate width L21 and are commonly connected at one end. The gates F21 form a comb type arrangement. The commonly connected portion is opposite to the first gate-source pads.

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Furthermore, the medium power FET comprises second gate-source pads having a plurality of source pads S25, S26 and a gate pad G24, a plurality of drain pads D25, D26, and a plurality of gates F22 positioned between the second gate-source pads and the drain pads D25, D26, which are formed on a semiconductor chip C2. The source pads S25, S26 and the gate pad G24 are alternately arranged on the semiconductor chip C2. The gates F21 have a gate width L22 which is the same as the gate width L21 of the gates F22. The gates F22 are commonly connected at one end, and form a comb type arrangement. The commonly connected portion is opposite to the second gate-source pads.

Furthermore, the high power FET and the medium power FET are separately arranged. The first gate-source pads and the drain pads D25, D26 are formed one side of the semiconductor chip C2. The drain pads D21-D24, the source pads S25, S26 and gate pad G24 are formed on the other side of the semiconductor chip C2.

Accordingly, a semiconductor device of the second embodiment of the present invention is able to have the same Vp in all of FETs formed on one chip, and it is easy to fabricate matching circuits between FETs.

C. A third embodiment

Fig. 3 is a plane view showing a semiconductor device according to a first embodiment of the present invention.

As shown in Figs. 3, the semiconductor device comprises

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the high power FET and the medium power FET. The high power FET and the medium power FET are formed on a semiconductor chip C3.

The high power FET comprises a first gate-source pads having a plurality of source pads S31-S34 and a plurality of gate pads G31-G33, a plurality of drain pads D31-D34, and a plurality of gates F31 positioned between the first gate-source pads and the drain pads D31-D34, which are formed on a semiconductor chip C3. The source pads S31-S34 and the gate pads G31-G33 are alternately arranged on the semiconductor chip C3. The gates F31 have a gate width L31 and are commonly connected at one end, forming a comb type arrangement. The commonly connected portion is opposite to the first gate-source pads.

Furthermore, the medium power FET comprises second gate-source pads having a plurality of source pads S35, S36 and a gate pad G34, a plurality of drain pads D35, D36, and a plurality of gates F32 positioned between the second gate-source pads and the drain pads D35, D36, which are formed on a semiconductor chip C3. The source pads S35, S36 and the gate pad G34 are alternately arranged on the semiconductor chip C3. The gates F31 have a gate width L31 which is the same as the gate width L32 of the gates F32. The gates F32 are commonly connected at one end, and form a comb type arrangement. The commonly connected portion is opposite to the second gate-source pads.

Furthermore, the high power FET and the medium power

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FET are separately arranged. The first gate-source pads and the drain pads D35, D36 are formed on one side of the semiconductor chip C3. The drain pads D31-D34, the source pads S35, S36 and gate pad G34 are formed on the other side of the semiconductor chip C3. The source pad S34 is connected with the source pad S35 using a shield pattern SL1.

Accordingly, a semiconductor device of the third embodiment of the present invention is able to have the same Vp in all of FETs formed on one-chip, and is able to isolate and shield between FETs.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate having a first region and a second region on a main surface;

a first field effect transistor formed on the first

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FET are separately arranged. The first gate-source pads and the drain pads D35, D36 are formed on one side of the semiconductor chip C3. The drain pads D31-D34, the source pads S35, S36 and gate pad G34 are formed on the other side of the semiconductor chip C3. The source pad S34 is connected with the source pad S35 using a shield pattern SL1.

Accordingly, a semiconductor device of the third embodiment of the present invention is able to have the same Vp in all of FETs formed on one-chip, and is able to isolate and shield between FETs.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.

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1. A semiconductor device, comprising:

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a first field effect transistor formed on the first

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region of the main surface, the first field effect transistor having first gates arranged in a plurality of rows and having a first total gate width, the first gates respectively establishing a first gate length and a first gate width; and

a second field effect transistor formed on the second region of the main surface, the second field effect transistor having second gates arranged a plurality of rows and having a second total gate width smaller than the first total gate width, the second gates respectively establishing a second gate length substantially the same as the first gate length and a second gate width substantially the same as the first gate width.

2. A semiconductor device as claimed in claim 1, further comprising:

a first plurality of source pads and a first plurality of gate pads commonly connecting between first gates at one side and formed on the main surface close to the commonly connecting portion;

a first plurality of drain pads arranged opposite to the first plurality of source pads and the first plurality of gate pads, and formed on the main surface through the first gates;

a second plurality of source pads and a second plurality of gate pads commonly connecting between second gates at one side, and formed close to the commonly connecting portion on

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the main surface; and

a second plurality of drain pads arranged opposite to the second plurality of source pads and the second plurality of gate pads and formed on the main surface through the second gates.

3. A semiconductor device as claimed in claim 1, wherein the first and second gates form a comb type arrangement.

4. A semiconductor device as claimed in claim 1, wherein the source pad, among the first plurality source pads, being closest to the second plurality drain pad, is electrically connected the source pad, among second plurality source pads , being closest to the second plurality drain pad of the.

5. A semiconductor device as claimed in claim 4, wherein the electrically connected portion forms a shield pattern.

6. A semiconductor device as claimed in claim 1, wherein the first and second gates form a comb type arrangement.

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