

GTL EDGE RATE CONTROL CIRCUIT

ABSTRACT OF THE DISCLOSURE

A GTL phased-output driver is provided which employs a pre-driver, a set of phasing elements or delay elements, and a set of output transistors. The pre-driver includes pull up devices, such as PMOS devices, and pull down devices, such as NMOS devices. The PMOS devices of the pre-driver are configured to route output transistor-triggering signals through the phasing elements in one direction whereas the NMOS devices are configured to route output transistor-releasing signals through the phasing devices in an opposite direction. Output transistors of differing sizes are employed. During a pull down operation, controlled by the PMOS pre-driver transistors, the output transistors are triggered sequentially in order from smallest to largest. During a pull up phase, controlled by the NMOS pre-driver transistors, the output transistors are released in a reverse order from largest to smallest. Hence, the largest transistor is triggered first during a pull down phase but is released last during a pull up phase. Within this configuration, improved edge rates and system noise levels are achieved. An edge rate control circuit is also described wherein time delays provided by each of the phasing elements may be varied to thereby vary the triggering times of the output transistors to also vary the edge rate of the output signal. Test circuitry for allowing individual testing of the output transistors is also described.