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(21) International Application Number: PCT/US96/19808 (22) International Filing Date: 12 December 1996 (12.12.96) (30) Priority Data: 08/575,295 20 December 1995 (20.12.95) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): ROLLENDER, Matthew [US/US]; 702 West Spur Avenue, Gilbert, AZ 85233 (US). HIRT, Ray [US/US]; 1124 E. Glencove, Mesa, AZ 85203 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>

(54) Title: SECURE SEMICONDUCTOR DEVICE**(57) Abstract**

A method for securing confidential circuitry from observation by unauthorized inspection, and a secure circuit immune from unauthorized inspection according to the method. In one embodiment, confidential data or circuitry is placed on a face of separate silicon layers (42, 44), each silicon layer having part of a circuit. Neither silicon layer is intelligible without the other, yet neither can be observed without destroying the other. The two silicon layers are juxtaposed, the face of the first silicon layer (42) flush against and fused to the face of the second silicon layer (44), the confidential circuits on each silicon layer connecting directly with circuits on the other silicon layer without external connectors. Data stored on each face is erased or destroyed when the silicon layers are separated or one of the silicon layers is destroyed. Violence to either silicon layer, or exposure of either silicon layer to light, destroys the data or circuitry on at least one silicon layer of silicon, making the data or circuitry unreadable.

