CLAIMS

What is claimed is:

1. A memory system, said system comprising:

a memory array wherein said memory array has a plurality of memory cells, wherein said plurality of memory cells store encryption data;

a heater integrated into said memory array between said plurality of memory cells; and

a processor in communication with said heater, wherein said processor notifies said heater to activate when a trigger event occurs.

2. The system of claim 1 wherein:

said plurality of memory cells are nonvolatile phase change memory cells.

3. The system of claim 2 wherein:

an activation of said heater heats at least a portion of said memory array and changes at least one of said nonvolatile phase change memory cells from a first phase to a second phase.

4. The system of claim 3 wherein:

said first phase is an amorphous phase and said second phase is a crystalline phase.

5. The system of claim 1 further comprising:

a material separating said heater from said plurality of memory cells, wherein said material is thermally conductive and electrically insulating.

6. The system of claim 1 further comprising:

at least one package integrity sensor in communication with said processor.

7. The system of claim 1 further comprising:

a power source in communication with at least one of said processor and said heater.

8. The system of claim 1 wherein:

said processor is a tamper detection unit.

9. A computer system, said computer system comprising:

a storage memory;

a memory cluster, wherein said memory cluster comprises:

one or more heaters interdigitated between a plurality of memory cells, wherein said plurality of memory cells store one or more encryption keys for encrypting or decrypting data stored in said storage memory; and

a tampering detector in communication with said one or more heaters, wherein said tampering detector notifies said one or more heaters to activate when a tampering event occurs.

10. The system of claim 9 wherein:

said plurality of memory cells are nonvolatile phase change memory cells.

11. The system of claim 10 wherein:

an activation of said one or more heaters heats at least a portion of said plurality of memory cells and changes at least one of said nonvolatile phase change memory cells from a first phase to a second phase.

12. The system of claim 11 wherein:

said first phase is an amorphous phase and said second phase is a crystalline phase.

13. The system of claim 9 further comprising:

a material separating said heater from said plurality of memory cells, wherein said material is thermally conductive and electrically insulating.

14. The system of claim 9 further comprising:

at least one package integrity sensor in communication with said tampering detector.

15. The system of claim 9 further comprising:

a power source in communication with at least one of said one or more heaters and said tampering detector.

16. The system of claim 9 wherein said tampering event is an unauthorized removal of at least one of a memory system or its components.

17. A method for memory erasure, said method comprising:

monitoring, by a processor, a memory array, wherein said memory array has a plurality of memory cells, wherein said plurality of memory cells store encryption data;

determining that a trigger threshold is exceeded; and

heating, by said processor communicating with at least one heater, at least one of said plurality of memory cells, wherein the at least one heater is disposed between said plurality of memory cells.

18. The method of claim 17 wherein:

said at least one of said plurality of memory cells is a phase change memory cell.

19. The method of claim 18 wherein:

said heating anneals said phase change memory cell.

20. A computer program product for memory erasure, said computer program product comprising a computer readable storage medium having program instructions embodied therewith, said program instructions executable by a processor to cause said processor to perform a function, said function comprising:

monitoring, by said processor, a memory array, wherein said memory array has a plurality of memory cells, wherein said plurality of memory cells store encryption data;

determining that a trigger threshold is exceeded; and

heating, by said processor communicating with at least one heater, at least one of said plurality of memory cells, wherein the at least one heater is interdigitated between said memory cells.

21. The computer program product of claim 20 wherein:

said at least one of said plurality of memory cells is a phase change memory cell.

22. The computer program product of claim 21 wherein:

said heating anneals said phase change memory cell.

23. A method for manufacturing an integrated circuit, said method comprising:

forming a non-volatile memory cell on top of a first electrode, wherein said first electrode is embedded in a dielectric material;

forming a heater on top of a second electrode, wherein said second electrode is embedded in said dielectric material, and wherein said heater is proximate said non-volatile memory cell;

forming a first top electrode on top of said non-volatile memory cell; and

forming a second top electrode on top of said heater.

24. The method of claim 23 further comprising:

forming a material between said heater and said non-volatile memory cell wherein said material is thermally conductive and electrically insulating.

25. The method of claim 23 wherein:

said non-volatile memory cell is a phase change memory cell.

~~26. A computer program comprising program code adapted to perform the method steps of any of claims 23 to 25 when said program is run on a computer.~~