Asymmetrical Layout Structure for ESD Protection

TECHNICAL FIELD

[0001] This invention relates generally to electrostatic discharge devices, and more specifically to obtaining uniformity of current flow in a grounded gate nMOS.

BACKGROUND

[0002] Electrostatic discharge (ESD) is a phenomenon where electrostatic charges migrate from a non-conductive surface via a conductive material. Since an electrostatic voltage is usually quite high, the ESD can easily damage the substrate and other components of an integrated circuit. For example, an electrostatic voltage from hundreds to thousands of volts can be created on a human body walking on a carpet under a higher relative humidity, while more than 10,000 volts can be created under a lower relative humidity. Also, an electrostatic voltage from hundreds to thousands of volts can be created in machines for packaging or testing integrated circuits. Therefore, when a human body or a machine carrying electrostatic charges contacts a chip, a large transient ESD current is generated, damaging or destroying the integrated circuits on the chip.

[0003] To protect the integrated circuits from being damaged by ESD, ESD devices capable of conducting an ESD current to ground are incorporated into the integrated circuits. Grounded gate NMOS (GGNMOS) devices are commonly used in protecting circuits.

[0004] A typical GGNMOS ESD protection circuit is illustrated in Figure 1. The ESD protection circuit includes a GGNMOS 8 for protecting the circuit 6. The gate 14 and source 12 of the GGNMOS 8 are coupled to the power line V_{SS} 4, where V_{SS} is typically grounded. Under normal operation, GGNMOS 8 is turned off so that it does not affect circuit 6. When an ESD

transient occurs to the circuit 6, the GGNMOS 8 is turned on, and the ESD current is conducted to V_{SS} 4. In order to conduct a high ESD current, the GGNMOS 8 typically has a great device dimension, such as W/L=500/0.5 in a typical 0.35μ CMOS technology. With such a device dimension, the GGNMOS 8 typically has a multiple-finger poly gate. It has been found that a GGNMOS with a large layout area and a great device dimension may only sustain a low ESD current because all portions of the GGNMOS cannot be uniformly turned-on during the ESD stress. Only a portion of the large-dimension GGNMOS is turned on to bypass the ESD current, but most of the portions stay off during the ESD stress.

[0005] Figure 2 illustrates a top view of a conventional GGNMOS. Only one finger is shown with a gate electrode 18, a drain region 14 and a source region 16. Contact plugs 26_1 through 26_7 connect to the drain region 14. A metal line 28 connects drain side contact plugs 26_1 through 26_7 to the circuit being protected. Contact plugs 22_1 through 22_7 connect to the source region 16. A metal line 24 couples contact plugs 22_1 through 22_7 to the p-well pick-up regions 20 and 21 that are located at the ends of the gate electrode 18. P-well pick-up regions 20 and 21 are typically grounded.

[0006] Multiple contact plugs divide the source region 14 and drain region 16 into sub regions. For simplicity purposes, each sub drain region and sub source region is referred to as the contact plug number next to it. The GGNMOS can be treated as sub nMOS transistors 32_1 through 32_7 connected in parallel. Each sub nMOS transistor 32_1 through 32_7 is formed of a drain 26_1 through 26_7, a gate electrode 18 and a source 22_1 through 22_7, respectively. When an ESD current occurs, it first flows from metal line 28 to contact plugs 26_1 through 26_7, then to the sub transistors 32_1 through 32_7 that are turned on. The ESD current then goes through contact plugs 22_1 through 22_7, then to metal 24, and finally to p-well pick-up regions 20 and 21. It is to be

noted that besides the current flowing from the drain to the source of each transistor, there is also a substrate current flowing at a direction from sub transistor 32_4 to transistors 32_5, 32_6 and 32_7, and a substrate current flowing at a direction from sub transistor 32_4 to transistors 32_3, 32_2 and 32_1.

[0007] Figure 3 illustrates a transmission-line model for the GGNMOS shown in Figure 2. Each of the sub transistors 32_1 through 32_7 illustrated in Figure 2 is modeled by an equivalent circuit 40_1 through 40_7. Circuits 40_1 through 40_7 are coupled in parallel. The equivalent circuit of the GGNMOS has an n-p-n structure, which is formed of drain(n)-substrate(p)-source(n). The resistors G_1 through G_7 are the substrate resistance of vertical path (from the top channel between the source 14 and drain 16 to the deep substrate, i.e., direction from gate to substrate or direction which penetrates into paper). Resistors R_{sub1} through R_{sub7} are the lateral substrate resistance from the deep substrate to the p-well pick-up regions. When an ESD current I_{ESD} occurs, it is distributed to circuits 40_1 through 40_7 and sunk to ground at node 4. As discussed in Figure 2, the ESD current I_{ESD} also goes through substrate resistors R_{sub3}, R_{sub2} and R_{sub1} to ground at node 4. It is appreciated that sub transistor 32_4 has the highest substrate resistance since it is furthest from the ESD sink point 4. The substrate resistances induce a voltage drop on the substrate 2. Therefore, the sub transistor 32_4 is likely to be turned on earlier than any other transistor. Similar analysis reveals that transistors in the center are more likely to be turned on earlier than transistors at the ends.

[0008] Turning on sub transistors at different times causes current crowding. At a lower ESD current, only sub transistors in the center, such as transistors 32_4, 32_3 and 32_5 are turned on. When current increases, from the center to the end, more and more sub transistors are turned on until at a certain time all sub transistors are turned on. It is noted that even when all the sub

transistors are on, the center transistors carry more ESD current than the transistors at the ends so that they are more prone to damage.

[0009] In order to improve the ESD level of such a large dimension GGNMOS, the multiple fingers of the large dimension GGNMOS have to be uniformly triggered on to share ESD current. If all the fingers and the sub transistors of the large dimension GGNMOS can be uniformly turned on during the ESD stress condition, the GGNMOS can sustain a much higher ESD level. Therefore, there is the need to achieve uniformity among the multiple sub transistors of the large-dimension GGNMOS.

SUMMARY OF THE INVENTION

[0010] The preferred embodiment of the present invention presents a semiconductor structure for electrostatic discharge protection.

[0011] In accordance with one aspect of the present invention, the semiconductor structure comprises a grounded gate nMOS (GGNMOS) having a substrate, a gate electrode, a source region and a drain region. A plurality of contact plugs is formed on the source and drain side. A plurality of first level vias is electrically coupled to the GGNMOS and has a substantially asymmetrical layout in the source and drain regions. A second level via(s) re-routes the ESD current to the desired first level vias.

[0012] The present invention provides a novel structure and method to improve the uniformity of a GGNMOS. By making the sub transistors turn on more uniformly, the preferred embodiment of the present invention makes the ESD protection circuit more efficient. This in turn improves the breakdown current and voltages, and the GGNMOS can be made smaller, therefore saving layout space without sacrificing protection ability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0014] Figure 1 illustrates a typical electrostatic discharge protection circuit using a grounded gate nMOS (GGNMOS);

[0015] Figure 2 illustrates a top view of one finger of a conventional GGNMOS;

[0016] Figure 3 illustrates a transmission-line model for a conventional GGNMOS;

[0017] Figures 4 illustrates a top view of a preferred embodiment of the present invention;

[0018] Figure 5 illustrates a cross-sectional view of the preferred embodiment along line A-A' in Figure 4;

[0019] Figure 6 illustrates a cross-sectional view of the preferred embodiment along line B-B' in Figure 4;

[0020] Figure 7 illustrates a variation of the preferred embodiment having via groups;

[0021] Figure 8a illustrates a prior art GGNMOS having one p-well pick-up region;

[0022] Figure 8b illustrates an embodiment of the present invention having one p-well pick-up region; and

[0023] Figure 9 shows the current in a GGNMOS as a function of the voltage applied.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0024] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0025] The preferred embodiments are illustrated in Figures 4 through 9 wherein like reference numbers are used to designate like elements throughout the various views and illustrative embodiments of the present invention. Figures 4, 5 and 6 illustrate different views of the preferred embodiment. Figure 4 illustrates a top view. A gate dielectric is formed on a substrate. A gate electrode 18 is formed on the gate dielectric with a preferred length of about 0.06μm to 0.4μm and a preferred width of about 1μm to about 90μm. More preferably, the gate length is between 0.1μm to 0.3μm and the gate width is between about 10μm to about 60μm. The gate electrode 18 is preferably coupled to at least one of the pick-up regions 20 and 21 located at two ends of the gate electrode 18. More preferably, the gate electrode 18 is coupled to both pick-up regions 20 and 21 for a better grounding. The pick-up regions 20 and 21 are preferably doped-well pick-up regions. Preferably, the pick-up regions 20 and 21 are grounded and each comprises at least 3 connection points such as vias connecting ground potentials. In Figure 4, there are 6 connection points connecting ground potentials on each of the pick-up regions 20 and 21. In the preferred embodiment, the pick-up regions 20 and 21 are p-well pickup regions and they will be referred to as p-well pick-up regions 20 and 21. In other embodiments, they are n-well pick-up regions. The details of forming the gate electrode 18, drain region 14, source region 16, and doped pick-up regions 20 and 21 are well known in the art so that they are not repeated herein.

[0026] The present invention is related to an asymmetrical layout of openings on drain and source sides of a GGNMOS device for improving ESD performance. The asymmetrical layout of openings may be contact plugs, via openings or trench openings, where in each case, the openings are filled with conductive materials. A preferred embodiment is described in Figures 4, 5 and 6. As shown in Figure 4, contact plugs 26_1 through 26_7 are coupled to the drain region 14. First level vias 52_1 and 52_2 are coupled to the drain side contact plugs 26_1 through 26_7 by a first level metal 56 (not shown). A second level via 50 couples the device being protected to two first level vias 52_1 and 52_2 through a second level metal 58 (not shown). Source contact plugs 22_1 through 22_7 are coupled to a via 54 located close to the middle of the gate. Via 54 is coupled to the p-well pick-up regions 20 and 21. The dimension of the vias is typically related to the technology. For example, in 0.13μm technology, a first level or a second level via preferably has a length and a width of about 0.05μm to about 0.5μm. In the preferred embodiment, the vias 50, 52_1, 52_2 and 54 are formed by a well-known damascene process. In other embodiments, vias can be formed using a plug process.

[0027] In order to explain the structure of the preferred embodiment in detail, cross-sectional views of Figure 4 are illustrated in Figures 5 and 6. Figure 5 illustrates a cross-sectional view of the preferred embodiment along line A-A' in Figure 4. For simplicity purposes, the contact plugs 26_1 through 26_7, and the vias 52_1, 52_2 and 50 are shown as in one plan. One skilled in the art will recognize that they can be in different plans as shown in Figure 4. Multiple drain side contact plugs 26_1 through 26_7 couple the drain 14 of the GGNMOS to a first level metal 56. The width of the first level metal 56 is preferably about 0.4μm to 3μm. Typically the contact plugs 26_1 through 26_7 are distributed evenly. Two first level vias 52_1 and 52_2 located at the ends of the drain region 14 connect the first level metal 56 to a second level metal 58. The second

level metal 58 is then connected to a second level via 50 that is coupled to the circuit being protected. Due to the large current that the GGNMOS may have to sink, it is desired that each of the vias 50, 52_1 and 52_2 comprise a group of vias. It is preferred that both the first level vias 52 comprise at least 2 vias on the drain side. Preferably, the number of first level vias 52 is higher than the number of second level vias 50. In one embodiment, the first level vias comprise two vias located on each end of the drain side and the second level vias comprise one via on the middle of the drain side, as shown in Figure 5. More preferably, for ESD performance, the 1st and 2nd level vias may each comprise at least three vias on the drain side. The embodiment referred to in Figure 4 comprises two first level vias and one second level via, but ESD performance can be improved if more vias, for example, more than three, are put on the drain side for the first and second levels.

[0028] Figure 6 illustrates a cross sectional view of the preferred embodiment along line B-B' in Figure 4, which is on the source side. Multiple drain contact plugs 22_1 through 22_7 couple the source 14 of the GGNMOS to a metal line 66. Metal line 66 is preferably a first level metal although it can be formed at the same time as other levels on the drain side, such as the first level metal 56. There are also first level vias 54 coupled to the first level metal 66, a second level metal (not shown) coupled to the first level vias 54 and second level vias (not shown) coupled to the second level metal. The metal line 66 is coupled to p-well pick-up regions 20 and 21. It is preferred that the first level vias comprise at least one via on the source side. In one embodiment, the first level vias comprise a via on the middle of the source side. More preferably, to improve ESD performance, the first level vias comprises at least two vias on the source side. In the preferred embodiment of the present invention, to improve ESD performance, the number of vias comprised by the first level vias are asymmetrical on drain and source sides. The asymmetrical

layout of vias on the source and drain sides are also preferred for the second level vias. Also, the number of vias on the drain side are preferably more than the number of vias on the source side at the same level.

[0029] Compared to the prior art in Figure 2, the ESD current path is re-arranged by routing the ESD current to two vias 52_1 and 52_2 at two ends of the drain. The ESD current flows in metal 56 from vias 52_1 and 52_2 to sub transistors 32_1 through 32_7. Since the resistance of a metal line is proportional to the length of the metal line, the resistance in metal line 56 for transistors 32_1 and 32_7 are the lowest since they are closest to vias 52_1 and 52_2. The metal 56 resistance increases for transistors 32_2, 32_3 and 32_4 due to the metal line resistance between contact plugs 22_1 and 22_2, and 22_3 and 22_4. From transistor 32_7 to transistor 32_4, metal 56 resistances also increase. Lower metal 56 resistance causes the sub transistors 32_1 and 32_7 to more likely be turned on first because current flow has high possibility to flow through a lower resistance path. This counteracts the effect discussed in the prior art where the center resistors are turned on first. Therefore, the preferred embodiment of the present invention has a more uniform turn-on voltage.

[0030] Also, there is another effect that possibly contributes to the uniformity of the turn on voltages, although it has less effect than the one discussed in the previous paragraph. In Figure 4, the sub transistor 32_1 has a relatively low drain substrate resistance because its drain is close to the via 52_1. It has a relatively high source substrate resistance because the contact plug 22_1 is far away from the via 54. Conversely, the transistor 32_4 has a relatively high drain substrate resistance because its drain 26_4 is far away from the via 52_1, while it has a relatively low source substrate resistance because the contact plug 22_4 is close to the via 54. The transistors 32_2 and 32_3 have moderate drain substrate resistance and source substrate resistance. The combination of drain substrate resistance and source substrate resistance for transistors 32_1, 32_2, 32_3 and 32_4 are

close, thus the voltage drops induced are close. Similar conclusions can be drawn for sub transistors 32_5, 32_6, 32_7. Therefore, re-arranging the discharging current going into the drain of the GGNMOS has reduced the non-uniformity caused by the substrate resistance.

[0031] Figure 7 illustrates a variation of the preferred embodiment. If the potential ESD current is high, or the via numbers in one finger is great, then vias 50, 52_1, 52_2 and 54 can be via groups having multiple vias. The number of vias depends on how much current each via can safely conduct.

[0032] Figure 8a illustrates another prior art. If there is only one p-well pick-up region 21 coupled to the source side contact plugs 22_1 through 22_7 through a metal line 57, the sub transistor 32_1 has the highest substrate resistance since it is furthest from the ground 4, and it will be turned on first. The ESD current crowding effect causes the transistor 32_1 to be more prone to failure. To counteract this effect, a drain side via 52 is placed nearest the contact plug 26_7 and is connected to contact plugs 26_1 through 26_7 through a metal 56, as shown in Figure 8b. A source side via 54 is placed nearest contact plug 22_1. The source side contact plugs 22_1 through 22_7 are coupled to via 54 through a metal, then to the p-well pick-up region 21. The sub transistor 32_7 has the lowest metal 56 resistance causing it to be turned on first. This counteracts the substrate resistance effect, therefore the transistors 32_1 through 32_7 are turned on more uniformly.

[0033] In a typical layout of the GGNMOS using the present invention, the GGNMOS has multiple fingers. For a layout using 0.13μm technology, in order to sink an ESD current of about one to two amps at human body mode (HMB), a GGNMOS preferably has a total length of about 720μm and a width of a little greater than about 30μm. Each gate has a preferred length of about 0.2μm and a preferred width of about 30μm. The source and drain regions on each gate are within an active region in the substrate. The active region has a preferred length of about 1μm to

about 10μm, and more preferably about 1μm to about 3μm. The active region has a preferred width of about 10μm to about 100μm, and more preferably about 10μm to about 30μm.

[0034] Since the ESD current is distributed to multiple fingers, the more fingers the GGNMOS has, the less ESD current each finger needs to carry, hence less first level vias 52 are needed. For example, if a GGNMOS has 15 fingers, for each finger, two first level vias 52 are typically enough. Also since the ESD current is distributed to the vias, the more vias a GGNMOS has, the less ESD current one via needs to carry. Typically, for 0.13μm technology, 32 vias on each of the source and drain sides are enough for discharging the ESD current.

[0035] The improvement of the preferred embodiment of the present invention is illustrated in Figure 9. Figure 9 shows the current in a GGNMOS as a function of the voltage applied. Line 61 is the test result of a conventional GGNMOS and line 62 is the test result of the preferred embodiment. Both tests are conducted on the GGNMOSs made with 0.13μm technology. The conventional GGNMOS has a break down voltage at point 64, or 2.65A, while the preferred embodiment of the present invention has a break down voltage at point 66, or 2.90A. The results are shown in table 1.

TABLE 1

	IT2	+HBM	+MM
Prior Art	2.65A	2.5kV	100V
Present Invention	2.9A	4.0kV	225V

It is noted that besides the IT2 breakdown voltage improvement, the highest voltage sustained is also improved significantly. In human body mode (HBM), the highest voltage is increased to

4.0kV for the present invention from 2.5kV for the conventional GGNMOS. In machine mode (MM), the highest voltage is increased to 225V for the present invention from 100V for the conventional GGNMOS.

[0036] The present invention provides a novel structure and method to improve the uniformity of a GGNMOS. By making the sub transistors turn on more uniformly, the ESD protection circuit is made more efficient. This in turn improves the breakdown current and voltages, and the GGNMOS can be made smaller therefore saving layout space without sacrificing protection ability.

[0037] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. A semiconductor structure for electrostatic discharge protection comprising:

a substrate;

a gate electrode;

a source region and a drain region overlying the substrate;

a plurality of first level openings electrically coupled to the source and drain regions;

wherein the plurality of first level openings have a substantially asymmetrical layout in the source and drain regions; and

wherein the first level openings are filled with conductive materials.

2. The semiconductor structure of claim 1 wherein the plurality of first level openings comprises at least two first level openings on the source side.

3. The semiconductor structure of claim 1 wherein the plurality of first level openings has a width between about 0.05μm to about 0.5μm.

4. The semiconductor structure of claim 1 further comprising a p-well pick-up region coupled between the gate electrode and a ground potential.

5. The semiconductor structure of claim 1 further comprising an n-well pick-up region coupled between the gate electrode and a ground potential.

6. The semiconductor structure of claim 1 wherein the gate electrode is coupled to ground potentials through pick-up regions at two ends.

7. The semiconductor structure of claim 1 wherein the gate electrode has a gate length of about 0.06μm to about 0.4μm.

8. The semiconductor structure of claim 1 wherein the gate electrode has a gate width of about 1μm to about 90μm.

9. The semiconductor structure of claim 8 wherein the gate electrode has a gate width of about 10μm to about 60μm.

10. The semiconductor structure of claim 1 further comprising a plurality of second level openings electrically coupled to the plurality of first level openings on the drain side wherein the plurality of first level openings and the plurality of second level openings have a substantially asymmetrical layout on the drain side, and wherein the second level openings are filled with conductive materials.

11. The semiconductor structure of claim 10 wherein the second level openings have a width of between about 0.05μm and about 0.5μm.

12. The semiconductor structure of claim 10 wherein the second level openings comprise at least three second level openings on the drain side.

13. The semiconductor structure of claim 1 wherein the first level openings are via openings.

14. The semiconductor structure of claim 1 wherein the source and drain regions are within an active region in the substrate.

15. The semiconductor structure of claim 14 wherein the active region has a length of about 1μm to 10μm.

16. The semiconductor structure of claim 15 wherein the active region has a length of about 1μm to 3μm.

17. The semiconductor structure of claim 14 wherein the active region has a width of about 10μm to 100μm.

18. The semiconductor structure of claim 17 wherein the active region has a width of about 10μm to 30μm.

19. A semiconductor structure for electrostatic discharge protection comprising:

a substrate;

a gate electrode;

a source region and a drain region overlying the substrate;

a plurality of first level openings electrically coupled to the source and drain regions and having a substantially asymmetrical layout in the source and drain regions;

wherein the plurality of first level openings comprises at least three first level openings on the drain side; and

wherein the first level openings are filled with conductive materials.

20. The semiconductor structure of claim 19 wherein the plurality of first level openings comprises at least two first level openings on the source side.

21. The semiconductor structure of claim 19 wherein the plurality of first level openings have a width of between about 0.05μm and about 0.5μm.

22. The semiconductor structure of claim 19 wherein the gate electrode is electrically coupled to ground potentials through pick-up regions.

23. The semiconductor structure of claim 19 wherein the gate electrode is coupled to ground potentials through pick-up regions at two ends.

24. The semiconductor structure of claim 19 wherein the plurality of first level openings are via openings filled with conductive materials.

25. The semiconductor structure of claim 19 further comprising a plurality of second level openings electrically coupled to the first level openings on the drain side wherein the second level openings are filled with conductive materials, and wherein the first level openings and the second level openings have a substantially asymmetrical layout on the drain side.

26. The semiconductor structure of claim 25 wherein the plurality of second level openings have a width of between about 0.05μm and about 0.5μm.

27. The semiconductor structure of claim 25 wherein the plurality of second level openings comprises at least three second level openings on the drain side.

28. A semiconductor structure for electrostatic discharge protection comprising:

a substrate;

a gate electrode;

a source region and a drain region overlying the substrate;

a plurality of first level openings electrically coupled to the source and drain regions;

wherein the number of first level openings on the drain side is more than the number of first level openings on the source side; and

wherein the first level openings are filled with conductive materials.

29. The semiconductor structure of claim 28 further comprising a plurality of second level openings electrically coupled to the first level openings on the drain side wherein the first level openings and the second level openings have a substantially asymmetrical layout on the drain side, and wherein the second level openings are filled with conductive materials.

30. The semiconductor structure of claim 28 wherein the plurality of second level vias has a width of between about 0.05μm and about 0.5μm.

31. The semiconductor structure of claim 28 wherein the plurality of second level openings comprises at least three second level openings on the drain side.

32. The semiconductor structure of claim 28 wherein the first level openings are via openings.

33. A semiconductor structure for electrostatic discharge protection comprising:

a substrate;

a dielectric on the substrate;

a gate electrode on the dielectric;

a source region and a drain region overlying the substrate wherein the source and drain regions have a first end and a second end;

a plurality of drain side contact plugs coupled to the drain region;

a plurality of source side contact plugs coupled to the source region;

a first level metal coupled to the drain side contact plugs;

a first group of first level vias on the drain side coupled to the first level metal wherein the first group of first level vias comprises one or more vias;

a source side metal coupled to the source side contact plugs and to a ground potential; and

a group of source side vias coupled to the source side metal wherein the group of source side vias comprises one or more vias and wherein the first group of first level vias has a substantially asymmetrical layout with the group of source side vias.

34. The semiconductor structure of claim 32 wherein the first group of first level vias is at the first end of the drain region and the group of source side vias is at the second end of the source region.

35. The semiconductor structure of claim 32 further comprising a second group of first level vias wherein the first group of first level vias is at the first end of the drain region, and the

second group of first level vias is at the second end of the drain region and the group of source side vias is at the middle of the source region.

36. The semiconductor structure of claim 32 further comprising:

a second level metal coupled to the first group of first level vias and the second group of second level vias; and

a group of second level vias coupled to the second level metal wherein the group of second level vias comprises one or more vias.

37. The semiconductor structure of claim 32 wherein the group of source side vias is coupled to a doped-well region wherein the doped-well region is selected from a group consisting of a p-well pick-up region and an n-well pick-up region.

38. The semiconductor structure of claim 37 wherein the doped-well region is grounded.