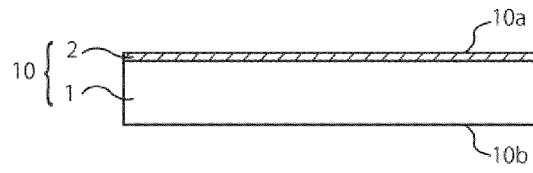
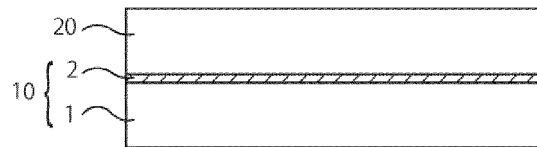


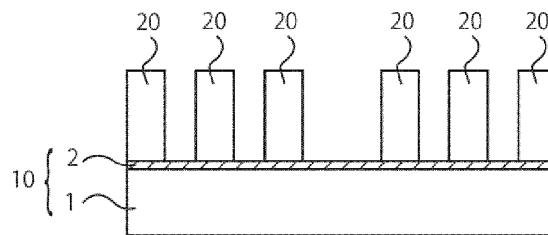
[図1]



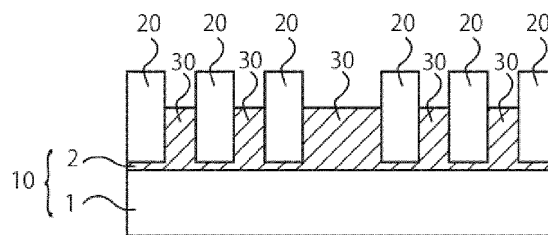
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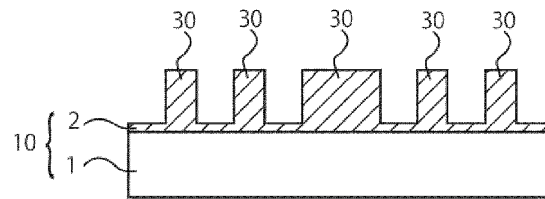
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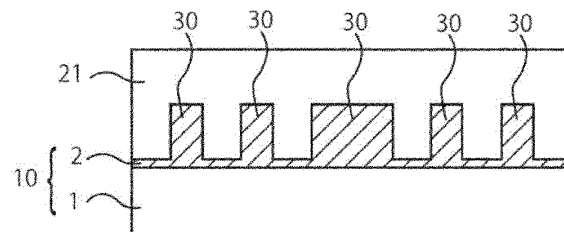
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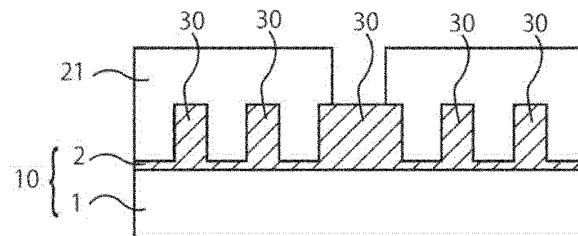
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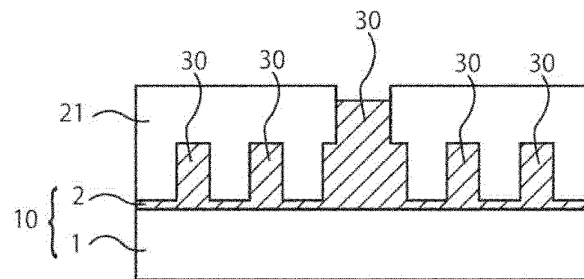
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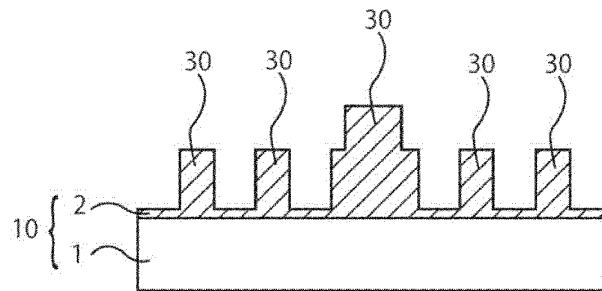
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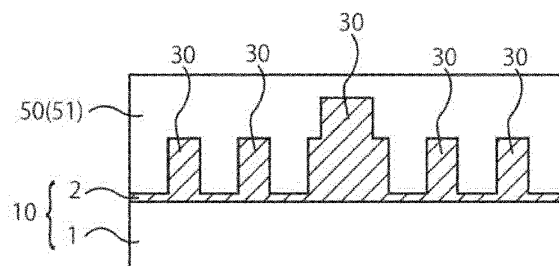
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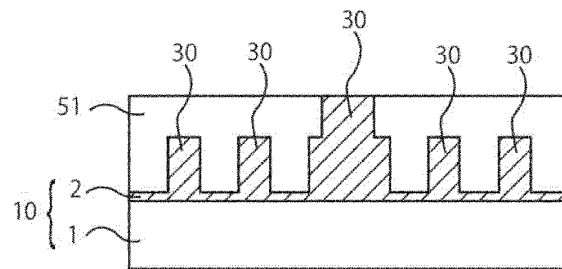
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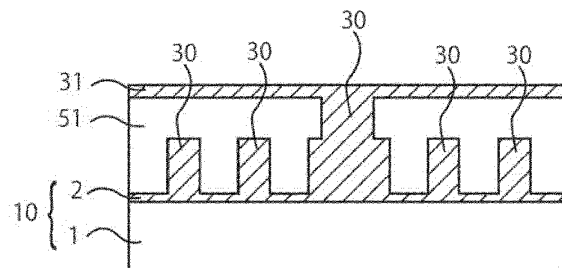
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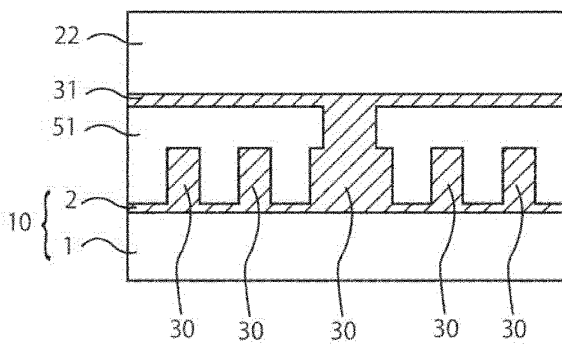
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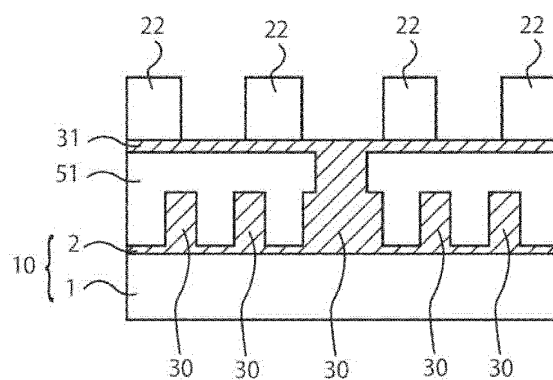
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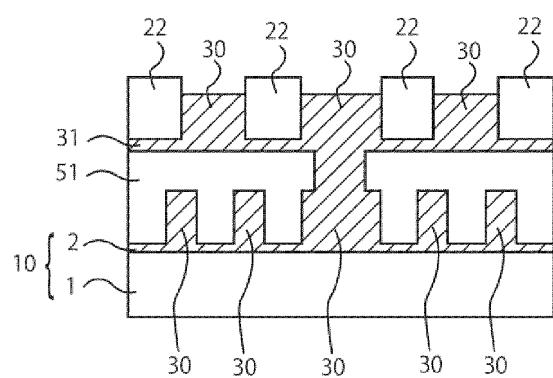
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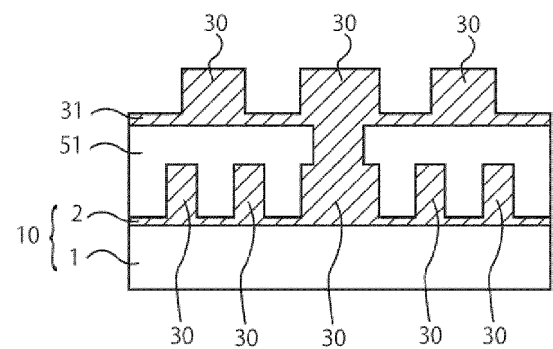
[図14]



[図15]



[図16]

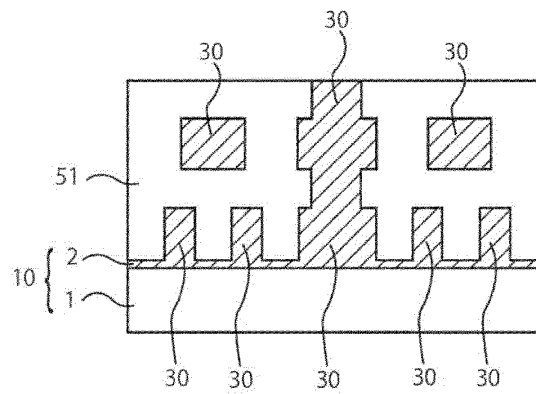


A cross-sectional view of a semiconductor device. A substrate 10 is shown with a thin layer 1 on its top surface. A patterned layer 2 is formed on layer 1, with openings filled with material 30. A thick layer 51 is formed on layer 2, with openings filled with material 30. The top surface of layer 51 is also covered with material 30.

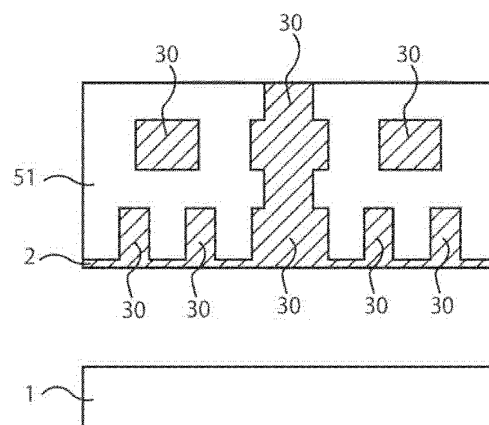
A cross-sectional view of a semiconductor device. It shows a substrate with a thin layer 1, a patterned layer 2, and a top layer 50(51) with openings 30. The openings 30 are filled with a material, and the top layer 50(51) has a dashed line 51 indicating a boundary.

Figure 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 10, which is divided into a first layer 1 and a second layer 2. A patterned layer 30 is formed on the second layer 2. A central structure 51v is formed on the second layer 2, and a layer 51 is formed on top of layer 30.

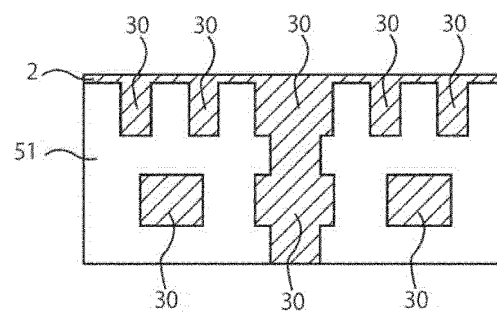
[図20]



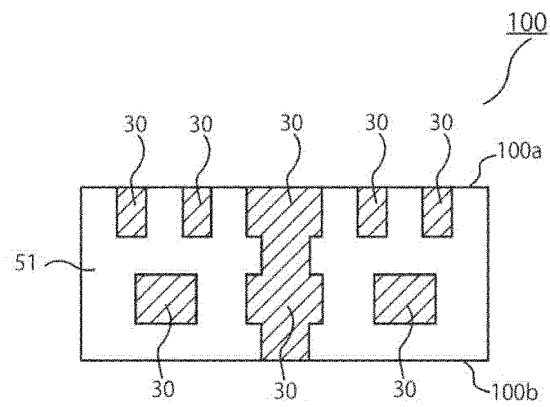
[図21]



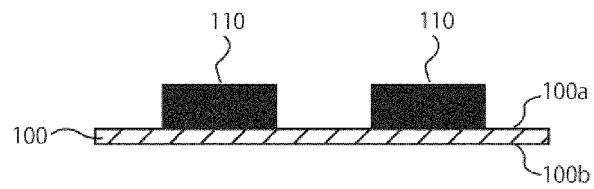
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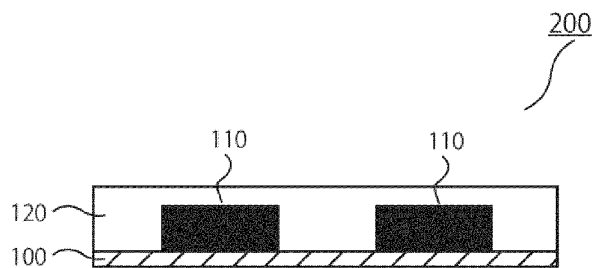
[図23]



[図24]



[図25]



[図26]

