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PEAK PROGRAM CURRENT REDUCTION APPARATUS AND METHOD

ABSTRACT OF THE DISCLOSURE

5 Apparatus and method for reducing peak program
current in memories include providing a memory with
an array of memory cells (29) arranged in rows and
columns and having a plurality of current terminals
and sequentially supplying current to each current
10 terminal of the plurality of current terminals (30).
The array is fabricated in a semiconductor chip with
connections to a current supply within the
semiconductor chip (32) including a plurality of
layers of metal connected by vias in the
15 semiconductor chip. In one embodiment, the array
includes tunnel junction MRAM cells integrated into a
semiconductor chip with current sources. The current
sources are integrated between the array of memory
cells and the connections to the current supply
20 within the semiconductor chip and are sequentially
operated.

Fig 2 accompanies this abstract.



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