SPLIT GATE MEMORY CELL

Abstract

A split gate memory cell is described which is fabricated from two-polysilicon layers and comprises a silicon substrate having a source and a drain electrode and a storage node, a tunnel oxide on the substrate, a first control gate electrode and a floating gate electrode spaced from each other and fabricated from the same polysilicon layer and a second control gate electrode of a second poly material formed between and over the first control gate and floating gate and isolated therefrom by a dielectric layer therebetween.

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