LINE END SHORTENING REDUCTION DURING ETCH

RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Patent Application No. 11/521,810 entitled "Line End Shortening Reduction during Etch," by Kota et al. filed September 14, 2006, which is hereby incorporated by reference.

FIELD OF INVENTION

[0002] The present invention relates to the formation of semiconductor devices. More particularly, the present invention relates to reducing line end shortening during the formation of semiconductor devices.

BACKGROUND OF THE INVENTION

[0003] During semiconductor wafer processing, features of the semiconductor device are defined in the wafer using well known patterning and etching processes. In these processes, a photoresist (PR) material is deposited on the wafer and is then exposed to light filtered by a reticle. The reticle is generally a glass plate that is patterned with exemplary feature geometries that block light from propagating through the reticle.

[0004] After passing through the reticle, the light contacts the surface of the photoresist material. The light changes the chemical composition of the photoresist material such that a developer can remove a portion of the photoresist material. In the case of positive photoresist materials, the exposed regions are removed, and in the case of negative photoresist materials, the unexposed regions are removed. Thereafter, the wafer is etched to remove the underlying material from the areas that are no longer protected by the photoresist material, and thereby define the desired features in the wafer.

[0005] The minimum feature size of integrated circuits (ICs) continues to shrink with each generation of semiconductor wafer processing improvements. As transistors and metal lines get smaller and move closer together, previously insignificant third-order variables now dominate IC design and fabrication. One problem that has arisen is “line end shortening” (LES). Figs. 1A and 1B illustrate one line end shortening problem. LES is characterized as the difference between the actual printed position of the end of a line and the intended (designed) position. Fig.

1A illustrates the design of a transistor 10 with a polysilicon line 12 running from left to right, that may form a gate region used to electrically couple an upper diffusion region with a lower diffusion region.

[0006] Fig. 1B illustrates the actual printed image that results from the design with the dotted lines 16 illustrating the desired design. Due to the etch effects and photoresist pullback, there is a significant amount of line end shortening 14. An LES ratio may be defined, with reference to Fig. 1B, as $(Y-Y_1)/(X-X_1)$, which is the ratio of the reduction of the length to the reduction of the width, which is currently greater than 2.

[0007] Figs. 2A and 2B illustrate another LES problem. The design illustrated in Fig. 2A may have a photoresist line 20 having a width W_1, side walls 24, and line ends 22 between an active source 26 and drain 28. The resulting printed image is illustrated in Fig. 2B. The resulting image has a photoresist line 30 with a width W_2, sidewalls 32, and line ends 34. The width, W_3, between the design line end 22 and the printed image line end 34 results in a gap between the source 26 and drain 28 that causes leakage and failure of the device. As stated above, and illustrated in Fig. 2B, LES at W_3, is much greater than the difference between W_1 and W_2. Thus, LES is greater at the line ends 22 as compared to the sidewalls 24. Although extensions may be added to the line to print a longer photoresist line, it is typically not possible because there is not enough room in the mask design to compensate for LES. The LES ratio may be defined as $(W_1-W_2)/(2\cdot W_3)$.

[0008] Others have added "hammer heads" onto line ends to compensate for LES. However, hammer heads may give rise to the design rule violations that can potentially cause bridging between the hammer head and polysilicon line. Although this bridging problem may be alleviated by a separation between the hammer head and polysilicon lines, the separation would increase the size of the circuit element, which means fewer circuit elements that can be integrated into a semiconductor device. Additionally, the use of hammer heads may cause larger line width roughness.

[0009] LES may result in degraded device performance, reduced reliability, lost yield, leakage in the device, limitations on critical dimensions (CD) and other related problems.

SUMMARY OF THE INVENTION

[0010] To achieve the foregoing and in accordance with the purpose of the present invention, a method for etching features in an etch layer is provided. A patterned photoresist mask is provided over the etch layer, the photoresist mask having at least one photoresist line having a pair of sidewalls ending at a line end is provided. A polymer layer is placed over the at least one photoresist line, wherein a thickness of the polymer layer at the line end of the photoresist line is greater than a thickness of the polymer layer on the sidewalls of the photoresist line. Features are etched into the etch layer through the photoresist mask, wherein a line end shortening (LES) ratio is less than or equal to 1.

[0011] Another manifestation of the invention provides for a method for etching features in an etch layer. A patterned photoresist mask is provided over the etch layer, the photoresist mask having at least one photoresist line having a pair of sidewalls ending at a line end. A polymer layer is placed over the at least one photoresist line, comprising flowing a deposition gas, transforming the deposition gas into a plasma, and stopping the deposition gas. The polymer layer is trimmed, wherein a thickness of the trimmed polymer layer at the line end of the photoresist line is greater than a thickness of the trimmed polymer layer on the sidewalls of the photoresist line, comprising flowing a trimming gas, transforming the trimming gas into a plasma, and stopping the trimming gas. Features are etched into the etch layer through the photoresist mask, wherein a line end shortening (LES) ratio is no more than 1.

[0012] In another manifestation of the invention, an apparatus for etching a feature in an etch layer, below a photoresist mask, having at least one photoresist line having a pair of sidewalls ending at a line end is provided. A plasma processing chamber has a chamber wall forming a plasma processing chamber enclosure, a substrate support for supporting a substrate within the plasma processing chamber enclosure, a pressure regulator for regulating the pressure in the plasma processing chamber enclosure, at least one electrode for providing power to the plasma processing chamber enclosure for sustaining a plasma, a gas inlet for providing gas into the plasma processing chamber enclosure, and a gas outlet for exhausting gas from the plasma processing chamber enclosure. A gas source in fluid connection with the gas inlet comprises a polymer deposition gas source and an etch layer etch gas source. A controller may be

controllably connected to the gas source and at least one electrode. The controller comprises at least one processor and computer readable media comprising computer readable code for reducing the shrinkage of the sidewalls and the line ends of the photoresist line, comprising at least one cycle, wherein each cycle comprises computer readable code for providing a deposition gas to form a polymer over the line, wherein an amount of polymer at the line ends is greater than an amount of polymer on the sidewalls, computer readable code for etching the etch layer, wherein a line end shortening (LES) is no more than 1, and computer readable code for removing the photoresist mask.

[0013] These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG.'s 1A and 1B illustrate one line end shortening problem.

FIG.'s 2A and 2B illustrate another line end shortening problem.

FIG. 3 is a high level flow chart of a process that may be used in an embodiment of the invention.

FIG.'s 4A-F are schematic cross-sectional and top views of a stack processed according to an embodiment of the invention.

FIG. 5 is a more detailed flow chart of a step of reducing line end shortening.

FIG. 6 is a schematic view of a plasma processing chamber that may be used in practicing the invention.

FIG.'s 7A-B illustrate a computer system, which is suitable for implementing a controller used in embodiments of the present invention.

FIG.'s 8A-D are schematic cross-sectional and top views of a stack processed according to an embodiment of the invention.

FIG. 9 is another more detailed flow chart of a step of reducing line end shortening.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

[0016] To facilitate understanding, FIG. 3 is a high level flow chart of a process that may be used in an embodiment of the invention. A patterned photoresist mask is provided (step 304). FIG. 4A is a schematic cross-sectional view of a layer to be etched 408 over a substrate 404, with a patterned photoresist mask 412 with photoresist features 414, over an underlayer 410, over the layer 408 to be etched forming a stack 400. The patterned photoresist mask 412 has at least one photoresist line having a pair of sidewalls 424 ending at a line end 420. To provide the patterned photoresist mask, a photoresist layer may be first formed over the layer to be etched. Then the photoresist layer is patterned to form photoresist lines with photoresist sidewalls and line ends. The photoresist features may have a width W_e, as shown.

[0017] FIG. 4B is a top view of the photoresist mask 412. As discussed above, manufacturing processes, such as lithography, result in LES of the printed image. The dotted lines 416 illustrate the printed pattern provided for the photoresist mask 412. The actual etched image may have sidewalls 434 and line ends 436 that are shortened, as illustrated.

[0018] The underlayer 410 may be any known organic, inorganic, or metal layer. For exemplary purposes and not intended to be limiting, the underlayer may be an anti-reflective layer (ARL), bottom anti-reflective coating (BARC), dielectric anti-reflective coating (DARC), amorphous carbon, hard mask such as Si_xO_y, Si_xN_y, $Si_xO_yN_Z$, or any other known underlayers.

[0019] A coating may be placed over the photoresist mask (step 308). FIG. 5 is a more detailed flow chart of this step. As shown in FIG. 5, the reduction of LES comprises at least one cycle of a cyclic process comprising the steps of depositing a

polymer layer 504 and hardening the polymer layer 508. The photoresist lines may be coated or deposited with a polymer layer so that spaces between the photoresist features 412 have widths "S_p" that are less than the widths "S_e" of the photoresist features, before the coating of the polymer layer, as shown in FIG. 4C, which is a cross-sectional view of the stack after the photoresist lines are coated with the polymer layer.

[0020] FIG. 4D is a top view of the photoresist mask 412 of FIG. 4C with the photoresist line coated with the polymer layer 226. The polymer layer 226 coats the photoresist line to protect the line ends 420 and sidewalls 424 during etching such that the LES ratio is equal to or less than 1. The coating reduces LES to increase the length and width of the photoresist line. As illustrated, the amount of polymer deposited at the line end 420, y, is greater than the amount of polymer deposited on the sidewalls 424, x, since shrinkage occurs to a greater degree at the line ends 420 than at the sidewalls 424. In one embodiment, it is preferable that the amount of coating deposited at the line ends be three times as much as the amount deposited on the sidewalls. The amount of coating deposited may be used to obtain an LES to sidewall reduction ratio of less than 1.

[0021] The polymer layer may contain a carbon, hydrogen, fluorine, or a combination thereof. The gases used may be a hydrocarbon such as methane (CH_4), fluorocarbon, hydrofluorocarbon, helium, argon, or a combination thereof. The fluorocarbon may have a chemical formula C_4F_8. Preferably, the fluorocarbon has a chemical formula $C_xH_yF_z$. The process of depositing the polymer over the photoresist mask may take between about 1 to 20 seconds.

[0022] The polymer may be hardened with a mixture of fluorocarbon and a hydrogen bromide gas. Preferably, the fluorocarbon may be CF_4. The cyclic process may be repeated until the desired layer is achieved. It is preferable that the cycle be repeated no more than 10 times, preferably at least one time.

[0023] Features 428 may then be etched into the etch layer 408 through the photoresist mask 412 (step 316), as shown in FIG. 4E. A portion or all of the polymer coating 226 may also removed during this step, thereby protecting the line ends and sidewalls to reduce the amount of LES such that the LES ratio is equal to or less than 1. The photoresist mask 412 is then removed (step 320), as shown in FIG. 4F.

Example

In an example of this process, a patterned photoresist layer is formed (step 304). A substrate 404, with the etch layer 408, an underlayer 410, and a patterned photoresist mask 412 is placed in an etch chamber.

[0024] FIG. 6 is a schematic view of a plasma processing system 600 that may be used for placing a polymer layer over a photoresist mask, hardening the polymer layer, etching, and stripping. Plasma processing system 600 may include a plasma processing tool 601. The plasma processing tool 601 is an inductively coupled plasma etching tool and includes a plasma reactor 602 having a plasma processing chamber 604 therein. A transformer coupled power (TCP) controller 650 and a bias power controller 655, respectively, control a TCP power supply 651 and a bias power supply 656 influencing the plasma 624 created within plasma chamber 604.

[0025] The TCP power controller 650 sets a set point for TCP power supply 651 configured to supply a radio frequency signal at 13.56MHz, tuned by a TCP match network 652, to a TCP coil 675 located near the plasma chamber 604. An RF transparent window 654 is provided to separate TCP coil 675 from plasma chamber 604 while allowing energy to pass from TCP coil 675 to plasma chamber 604. An optically transparent window 665 may be provided by a circular piece of sapphire having a diameter of approximately 2.5 cm (1 inch) located in an aperture in the RF transparent window 654.

[0026] The bias power controller 655 sets a set point for bias power supply 656 configured to supply an RF signal, tuned by bias match network 657, to a chuck electrode 608 located within the plasma chamber 604 creating a direct current (DC) bias above electrode 608 which is adapted to receive a substrate 606, such as a semiconductor wafer work piece, being processed.

[0027] A gas supply mechanism or gas source 610 includes a source or sources of gas or gases 616 attached via a gas manifold 617 to supply the proper chemistry required for the process to the interior of the plasma chamber 604. A gas exhaust mechanism 618 includes a pressure control valve 619 and exhaust pump 620 and removes particles from within the plasma chamber 604 and maintains a particular pressure within plasma chamber 604.

[0028] A temperature controller 680 controls the temperature of heaters 682 provided within the chuck electrode 608 by controlling a heater power supply 684. The plasma processing system 600 also includes electronic control circuitry 670.

[0029] FIG.'S 7A and 7B illustrate a computer system 700, which is suitable for implementing a controller 670 used in embodiments of the present invention. FIG. 7A shows one possible physical form of the computer system. Of course, the computer system may have many physical forms ranging from an integrated circuit, a printed circuit board, and a small handheld device up to a huge super computer. Computer system 700 includes a monitor 702, a display 704, a housing 706, a disk drive 708, a keyboard 710, and a mouse 712. Disk 714 is a computer-readable medium used to transfer data to and from computer system 700.

[0030] FIG. 7B is an example of a block diagram for computer system 700. Attached to system bus 720 is a wide variety of subsystems. Processor(s) 722 (also referred to as central processing units or CPUs) are coupled to storage devices, including memory 724. Memory 724 includes random access memory (RAM) and read-only memory (ROM). As is well known in the art, ROM acts to transfer data and instructions uni-directionally to the CPU and RAM is used typically to transfer data and instructions in a bi-directional manner. Both of these types of memories may include any suitable of the computer-readable media described below. A fixed disk 726 is also coupled bi-directionally to CPU 722; it provides additional data storage capacity and may also include any of the computer-readable media described below. Fixed disk 726 may be used to store programs, data, and the like and is typically a secondary storage medium (such as a hard disk) that is slower than primary storage. It will be appreciated that the information retained within fixed disk 726 may, in appropriate cases, be incorporated in standard fashion as virtual memory in memory 724. Removable disk 714 may take the form of any of the computer-readable media described below.

[0031] CPU 722 is also coupled to a variety of input/output devices, such as display 704, keyboard 710, mouse 712, and speakers 730. In general, an input/output device may be any of: video displays, track balls, mice, keyboards, microphones, touch-sensitive displays, transducer card readers, magnetic or paper tape readers, tablets, styluses, voice or handwriting recognizers, biometrics readers, or other

computers. CPU 722 optionally may be coupled to another computer or telecommunications network using network interface 740. With such a network interface, it is contemplated that the CPU might receive information from the network, or might output information to the network in the course of performing the above-described method steps. Furthermore, method embodiments of the present invention may execute solely upon CPU 722 or may execute over a network such as the Internet in conjunction with a remote CPU that shares a portion of the processing.

[0032] In addition, embodiments of the present invention further relate to computer storage products with a computer-readable medium that have computer code thereon for performing various computer-implemented operations. The media and computer code may be those specially designed and constructed for the purposes of the present invention, or they may be of the kind well known and available to those having skill in the computer software arts. Examples of computer-readable media include, but are not limited to: magnetic media such as hard disks, floppy disks, and magnetic tape; optical media such as CD-ROMs and holographic devices; magneto-optical media such as floptical disks; and hardware devices that are specially configured to store and execute program code, such as application-specific integrated circuits (ASICs), programmable logic devices (PLDs) and ROM and RAM devices. Examples of computer code include machine code, such as produced by a compiler, and files containing higher level code that are executed by a computer using an interpreter. Computer readable media may also be computer code transmitted by a computer data signal embodied in a carrier wave and representing a sequence of instructions that are executable by a processor.

[0033] A polymer layer is placed over the photoresist mask (step 308). Using multiple cycles of the cycle shown in FIG. 5, an example recipe of depositing a polymer layer (step 504) would use, for example, a gas of at least one of CH_4, C_4F_8, and $C_xH_yF_z$. An etch chamber or plasma processing chamber may have a pressure of 1-100 mT. More preferably, the pressure for laterally etching the mask is between 2-8 mT. 500 to 1000 Watts of power are supplied to the plasma processing chamber at 13.56 MHz. The temperature may be between about 40°C -60°C. In one embodiment of a recipe, 20 sccm CH_4 and 100 sccm of He is used at a temperature of 40°C for 15 seconds at a pressure of 5mT, 500 Watts of power, and zero bias power.

[0034] The plasma layer is hardened (step 508). An example recipe for the hardening of the polymer layer provides a fluorocarbon and hydrogen bromide containing gas, such as 100 sccm CF_4 and 25 sccm HBr. A pressure of 5 mTorr is provided to the chamber. A RF power source provides 500 Watts at a frequency of 13.56 MHz and a temperature of 40°C.

[0035] Features are then etched into the etch layer (step 316). In this example, the etch layer is a polysilicon for forming a gate. In other embodiments, the layer to be etched may be a conventional etch layer, such as SiN, SiC, an oxide, a metal layer, or low-k dielectric. A conventional etch recipe may be used to etch the layer to be etched.

[0036] To remove the mask (step 320) an oxygen ashing may be used.

[0037] In a preferred embodiment of the invention, the placement of the polymer layer, hardening of the polymer layer, and etching the features into the etch layer are done in situ in the same etch chamber, as shown. Preferably, the placement and hardening of the polymer layer is performed over less than ten cycles. More preferably, the placement and hardening of the polymer layer is performed over at least one cycle.

[0038] An example of a recipe for a deposition provides a chamber pressure of 25 mTorr. A deposition gas of 100 sccm C_4F_8 is provided. The deposition gas is transformed into a plasma by providing 500 watts of TCP power at 13.56 MHz, where the bias voltage is 0 volts. Another example of a deposition recipe uses a CH_4 recipe. This example provides a chamber pressure of 5 mTorr. A deposition gas of 20 sccm CH_4 and 100 sccm He is provided into the chamber. The deposition gas is transformed into a plasma by providing 600 watts of TCP power at 13.56 MHz where the bias voltage is 0 volts. The deposition steps are followed by a HBr and CF_4 hardening step.

[0039] More generally, a deposition may have a gas chemistry comprising of at least one of CHF_3, CF_4, CH_2F_2, CH_4, or $SiCl_4$.

[0040] In an alternative embodiment, a hardening step is not used. For example, the photoresist and deposited polymer are sufficiently etch resistant so that a hardening step is not needed. In the above example where the deposition gas of 100 sccm C_4F_8 is provided and the above example where the deposition gas of 20 sccm

CH_4 and 100 sccm He is provided a separate hardening step may be omitted. Such a process is able to eliminate the hardening step making such a process simpler with a higher through put. In another example of a deposition recipe that does not require a separate hardening step the chamber pressure is set at 5-10 mTorr. A deposition gas of 100 sccm CF_4 and 20 sccm HBr is flowed into the chamber. The deposition gas is formed into a plasma by providing 300-500 watts of TCP power at 13.56 MHz with a bias voltage of 100-200 volts. In another example of a deposition recipe that does not require a separate hardening step the chamber pressure is set to 5-10 mTorr. A deposition gas of 200 sccm N_2 and 20-50 sccm of CF_4 is flowed into the chamber. The deposition gas is formed into a plasma by providing 300-900 watts of TCP power at 13.56 MH with a bias voltage of 100-300 volts. These processes do not trim. They deposit at tip to tip and harden the photoresist.

[0041] Another example is a process that does not use a hardening step and that provides a polymer forming process with a deposition phase and a trim phase. According to the process of FIG. 3, a patterned photoresist mask is provided (step 304). FIG. 8A is a schematic cross-sectional view of a layer to be etched 808 over a substrate 804, with a patterned photoresist mask 812 with photoresist features 814, over an underlayer 810, over the layer 808 to be etched forming a stack 800. The patterned photoresist mask 812 has at least one photoresist line having a pair of sidewalls 824 ending at a line end. To provide the patterned photoresist mask, a photoresist layer may be first formed over the layer to be etched. Then the photoresist layer is patterned to form photoresist lines with photoresist sidewalls and line ends. The photoresist features may have a width S_e, as shown.

[0042] FIG. 8B is a top view of the photoresist mask 812. The patterned photoresist mask 812 has at least one photoresist line having a pair of sidewalls 824 ending at line ends 820.

[0043] A coating is placed over the photoresist mask (step 308). FIG. 9 is a more detailed flow chart of this step. As shown in FIG. 9, the reduction of the LES ratio comprises at least one cycle of a cyclic process comprising the steps of depositing a polymer layer (step 904) and trimming the sidewalls (step 908). FIG. 8C is a top view of the photoresist mask 812 after a polymer layer 828 is deposited over the photoresist mask 812 (step 904). The polymer layer 828 coats the photoresist line to protect the

line ends 820 and sidewalls 824. In this example, the thickness of the polymer layer deposited on the sidewalls 824 is about the same as the thickness of the polymer deposited on the line end 820. In other examples, the thicknesses may have different relationships. In an example recipe for such a process, a deposition provides a chamber pressure of 5 mTorr. A deposition has of 20 sccm HBr, 80 sccm CF_4, and 5 sccm O_2 is flowed into the chamber. The deposition gas is formed into a plasma by providing 300-500 watts of TCP power at 13.56 MHz with a bias voltage of 0 volts. FIG. 8D is a top view of the photoresist mask 812 after the sidewalls are trimmed (step 908).

[0044] An example of a trim recipe provides a chamber pressure of 8 mTorr. A trim gas of 20 sccm Cl_2, 20 sccm O_2, and 60 sccm He is flowed into the chamber. The trim gas is formed into a plasma by providing 300 watts of TCP power at 13.56 MHz with a voltage bias of 0 volts. The trimming selectively etches the polymer and possibly even the photoresist on the sidewalls faster than on the line ends, so that the polymer on the line ends is thicker than on the sidewalls, as shown in FIG. 8D. Although the example in FIG. 8D shows that only polymer is trimmed, in other examples, the polymer on the sidewalls may be completely trimmed away so that some of the sidewall of the photoresist mask is trimmed. Features are then etched into the etch layer (step 316). The mask and polymer layer are removed (step 320). Because as in the previous embodiments, the resulting polymer layer is thicker on the ends and thinner on the sidewalls, LES is reduced. The addition of a trim, also allows a reduction in CD. By not having a hardening step, the trimming is made easier.

[0045] In another example of a deposition and trim process, at least four cycles of a deposition and then trim are performed, so that each deposition deposits a thin layer before a trim is performed, which trims a small amount before the next deposition. It has been found that such multiple cycle processes provide improved control.

[0046] In another example deposition and trimming may be done simultaneously, so that that the deposition and trimming may be done in a single step. An example recipe that performs a trim and deposition in a single step is as follows: The chamber pressure is set to 5 mTorr. A deposition and trim gas of 80-150 sccm CF_4, 20 sccm HBr, and 0-5 sccm O_2 is provided. The deposition and trim gas is formed into a plasma by providing 300-625 watts at a frequency of 13.56 MHz, where the bias

voltage is 0 volts. This is a single deposition and trim process that hardens photoresist, so that a separate hardening step is not needed.

[0047] In another example of a deposition and trim process in a single step, a pressure of 5 mTorr is provided. A deposition and trim gas of about 80-100 sccm CF_4 and about 20 sccm CHF_3 or CH_2F_2 is provided. The deposition and trim gas is converted to a plasma by providing about 300 watts TCP power at 13.56 MHz with a bias voltage of 0 volts. This recipe trims lines but deposits at tip to tip and improve the LES ratio, without requiring a hardening step. Gas injection and TESC temperature are not fixed here as those may be used to tune out uniformity.

[0048] In another embodiment, the placing a coating over the photoresist mask (step 308), simultaneously deposits polymer over the photoresist mask and etches the under layer, for example BARC, in a single step. The hardening step can be avoided by using the BARC as part of the etch mask. In an example of a deposition and BARC etch recipe, a chamber pressure is set to 5-8mTorr. A deposition and BARC etch gas of 200 sccm N_2 and 20-50 sccm CF_4 is flowed to the chamber. The deposition and BARC etch gas is formed into a plasma by providing 300-900 watts of TCP power at 13.56 MHz.

[0049] In another example a recipe for providing a BARC etch provides a chamber pressure of 8 mTorr. A BARC etch gas of 20 sccm Cl_2, 20 sccm O_2, 4 sccm $SiCl_4$, and 60 sccm He is provided. The BARC etch gas is formed into a plasma by providing 300-400 watts of TCP power at 13.56 MHz with a bias voltage of -150 volts. In another example recipe, a chamber pressure of 8 mTorr is provided. A BARC etch gas of 80-100 CF_4 and 20 sccm of CHF_3 or CH_2F_2 is flowed into the chamber. The BARC etch gas is formed into a plasma by providing 300-400 watts TCP power at 13.56 MHz with a bias voltage of 100-200 volts.

[0050] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and various substitute equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and various substitute equivalents as fall within the true spirit and scope of the present invention.

CLAIMS

What is claimed is:

1. A method for etching features in an etch layer, comprising:

providing a patterned photoresist mask over the etch layer, the photoresist mask having at least one photoresist line having a pair of sidewalls ending at a line end;

placing a polymer layer over the at least one photoresist line, wherein a thickness of the polymer layer at the line end of the photoresist line is greater than a thickness of the polymer layer on the sidewalls of the photoresist line; and

etching features into the etch layer through the photoresist mask, wherein a line end shortening (LES) ratio is less than or equal to 1.

2. The method of claim 1, wherein the placing the polymer layer over the at least one photoresist line simultaneously etches an underlayer while depositing the polymer layer to form an etch mask with the underlayer for a subsequent etching of the etch layer.

3. The method of claim 2, wherein the depositing the polymer layer, comprises:

flowing a deposition gas;

forming the deposition gas into a plasma; and

providing a bias voltage with a magnitude of at least 100 volts.

4. The method of claim 1, wherein the placing the polymer layer over the at least one photoresist line, comprises at least one cycle, wherein each cycle comprises:

a deposition phase, which deposits polymer on the at least one photoresist line; and

a trim phase which selectively trims the deposited polymer, so that polymer deposited over the sidewalls of the at least one photoresist line is trimmed more than polymer deposited over the line end of the at least one photoresist line.

5. The method, as recited in claim 4, wherein the placing the polymer layer over the at least one photoresist line comprises at least four cycles.

6. The method, as recited in any of claims 4-5, wherein the deposition phase, comprises:

flowing a deposition gas;

forming a plasma from the deposition gas; and

stopping the deposition gas; and wherein the trim phase comprises:

flowing a trim gas;

forming a plasma from the trim gas; and

stopping the flow of the trim gas.

7. The method, as recited in claim 6, wherein the trim gas comprises an oxygen containing gas.

8. The method, as recited in claim 7, wherein the trim gas further comprises Cl_2.

9. The method of claim 1, wherein the placing the polymer layer over the at least one photoresist line, comprises:

providing a deposition gas, comprising a polymer forming gas and HBr; and

forming a plasma from the deposition gas.

10. The method of claim 1, wherein the placing the polymer layer over the at least one photoresist line, comprises:

flowing a deposition gas and trim gas simultaneously; and

forming the deposition gas and trim gas into a plasma.

11. The method of any of claims 1-10, further comprising providing an oxygen ashing.

12. The method of claim 1, wherein the placing the polymer layer over the at least one photoresist line, comprises:

providing a deposition gas, comprising at least one of CHF_3, CF_4, CH_2F_2, CH_4, or $SiCl_4$; and

forming the deposition gas into a plasma.

13. A semiconductor device formed by the method of any of claims 1-12.

14. A method for etching features in an etch layer, comprising:

providing a patterned photoresist mask over the etch layer, the photoresist mask having at least one photoresist line having a pair of sidewalls ending at a line end;

placing a polymer layer over the at least one photoresist line, comprising:

flowing a deposition gas;

transforming the deposition gas into a plasma; and

stopping the deposition gas;

trimming the polymer layer, wherein a thickness of the trimmed polymer layer at the line end of the photoresist line is greater than a thickness of the trimmed polymer layer on the sidewalls of the photoresist line, comprising:

flowing a trimming gas;

transforming the trimming gas into a plasma; and

stopping the trimming gas; and

etching features into the etch layer through the photoresist mask, wherein a line end shortening (LES) ratio is no more than 1.

15. The method, as recited in claim 14, wherein the trimming gas comprises an oxygen containing gas.

16. The method, as recited in claim 15, wherein the trim gas further comprises Cl_2.

17. An apparatus for etching a feature in an etch layer, below a photoresist mask, having at least one photoresist line having a pair of sidewalls ending at a line end, comprising:

a plasma processing chamber, comprising:

a chamber wall forming a plasma processing chamber enclosure;

a substrate support for supporting a substrate within the plasma processing chamber enclosure;

a pressure regulator for regulating the pressure in the plasma processing chamber enclosure;

at least one electrode for providing power to the plasma processing chamber enclosure for sustaining a plasma;

a gas inlet for providing gas into the plasma processing chamber enclosure; and

a gas outlet for exhausting gas from the plasma processing chamber enclosure;

a gas source in fluid connection with the gas inlet, comprising:

a polymer deposition gas source; and

an etch layer etch gas source; and

a controller controllably connected to the gas source and the at least one electrode, comprising:

at least one processor; and

computer readable media, comprising:

computer readable code for reducing the shrinkage of the sidewalls and the line ends of the photoresist line, comprising at least one cycle, wherein each cycle comprises:

computer readable code for providing a deposition gas to form a polymer over the line, wherein an amount of polymer at the line ends is greater than an amount of polymer on the sidewalls;

computer readable code for etching the etch layer, wherein a line end shortening (LES) is no more than 1; and

computer readable code for removing the photoresist mask.