SEMICONDUCTOR MEMORY AND CAPACITY CONFIGURION METHOD FOR STORAGE BLOCK THEREON

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority to Chinese patent application No. 202110783912.0 filed on July 12, 2021 and entitled “SEMICONDUCTOR MEMORY AND METHOD FOR CONFIGURING DENSITY OF BANK OF SEMICONDUCTOR MEMORY”, the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The embodiments of the disclosure relate to the field of semiconductor technologies, and relate to, but are not limited to, a semiconductor memory and a method for density configuration of a bank of the semiconductor memory.

BACKGROUND

[0003] At present, in order to achieve different densities for the same type of chips, a set of trim commands may be adopted to trim same storage regions (arrays) of all the banks of each full-chip to obtain different densities.

[0004] Since the damaged arrays of different banks may be completely different, in order to utilize the chip whose arrays are partially damaged, the method of selecting the same arrays of the full-chip for trimming is obviously defective and results in the low effective utilization rate of the density configuration of the banks of the semiconductor memory.

SUMMARY

[0005] In view of this, an embodiment of the disclosure provides a semiconductor memory and a method for density configuration of a bank of the semiconductor memory, which is able to flexibly select a storage region to be trimmed and improve the effective utilization rate of the density configuration of banks of the semiconductor memory.

[0006] In a first aspect, an embodiment of the disclosure provides a method for density configuration of a bank of a semiconductor memory, including:

[0007] determining a target bank to be configured of the memory;

[0008] determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank;

[0009] determining, based on the density configuration parameter of the target bank, a target code from a set of codes of the target bank, the target code corresponding to a storage region to be trimmed in the target bank;

[0010] generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank; and

[0011] trimming, based on the region selection signal, the storage region to be trimmed to configure the density of the target bank.

[0012] In a second aspect, an embodiment of the disclosure provides a semiconductor memory, including:

[0013] a target bank, including at least two storage regions;

[0014] an address processing unit, configured to output an address of the target bank, an output terminal of the address processing unit being connected to the target bank;

[0015] a code acquisition unit, configured to receive a target code, the target code corresponding to at least one storage region to be trimmed in the target bank;

[0016] a region selection signal generation unit, configured to generate, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank, an output terminal of the region selection signal generation unit being connected to an input terminal of a trim unit; and

[0017] the trim unit, configured to trim the storage region to be trimmed based on the region selection signal to configure the density of the target bank, an output terminal of the trim unit being connected to the target bank.

[0018] According to the embodiments of the disclosure, since the density configuration parameters of different target banks to be configured may be different, the target codes determined based on the different density configuration parameters may be different, and the region selection signals generated based on the different target codes may be different. Therefore, different storage regions to be trimmed of different target banks to be configured can be trimmed through different region selection signals, so that the storage region to be trimmed can be flexibly selected, thereby improving the effective utilization rate of the density configuration of the banks of the semiconductor memory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] In the drawings (which are not necessarily drawn to scale), similar reference numerals may describe similar components in different views. Similar reference

numerals with different letter suffixes may represent different examples of similar components. The drawings generally illustrate, by way of examples and not limitation, various embodiments of the disclosure.

[0020] FIG. 1 is a diagram of composition structure of a Dynamic Random Access Memory (DRAM) in the related art.

[0021] FIG. 2 is a flowchart of implementation of a method for density configuration of a bank of a semiconductor memory according to an embodiment of the disclosure.

[0022] FIG. 3a is a structural diagram of storage regions and addresses of a full-chip according to an embodiment of the disclosure.

[0023] FIG. 3b is an enlarged structural diagram of Bank8 of FIG. 3a according to an embodiment of the disclosure.

[0024] FIG. 3c is a structural diagram of Bank8 after trimming according to an embodiment of the disclosure.

[0025] FIG. 3d is a logic circuit diagram of performing logic NOT operation on a target code according to an embodiment of the disclosure.

[0026] FIG. 3e is a logic circuit diagram of performing logic NOT operation on Ra<15:14> according to an embodiment of the disclosure.

[0027] FIG. 3f is a logic circuit diagram of performing logic operation on DensityTrim<0> and DensityTrim<1> according to an embodiment of the disclosure.

[0028] FIG. 3g is a logic circuit diagram of performing logic operation on DensityTrimB<0> and DensityTrimB<1> according to an embodiment of the disclosure.

[0029] FIG. 3h is a logic circuit diagram of obtaining a region selection signal Ra1514<0> based on a target code and a high 2-bit address according to an embodiment of the disclosure.

[0030] FIG. 3i is a logic circuit diagram of obtaining a region selection signal Ra1514<1> based on a target code and a high 2-bit address according to an embodiment of the disclosure.

[0031] FIG. 3j is a logic circuit diagram of obtaining a region selection signal Ra1514<2> based on a target code and a high 2-bit address according to an embodiment of the disclosure.

[0032] FIG. 4 is a structural diagram of a system for density configuration of a bank of a semiconductor memory according to an embodiment of the disclosure.

[0033] FIG. 5 is a structural diagram of a semiconductor memory according to an embodiment of the disclosure.

DETAILED DESCRIPTION

[0034] To make the objectives, technical solutions and advantages of the embodiments of the disclosure be understood more clearly, the specific technical solutions of the disclosure will be described in further detail below with reference to the drawings in the embodiments of the disclosure. The following embodiments are merely used to illustrate the disclosure, but are not intended to limit the scope of the embodiments of the disclosure.

[0035] In the following description, the suffixes such as “module” or “unit” used to represent the components are merely to facilitate the illustration of the embodiments of the disclosure and have no specific meaning. Therefore, “module” or “unit” may be used interchangeably.

[0036] In the related art, due to the high cost of each set of masks for memory chips, the trims are usually adopted to achieve different densities in the design of the same type of chips so as to quickly dominate the market. In actual production, there will also be some chips whose arrays are partially damaged. In this case, these chips may be sold as low-density chips to increase the yield. For example, 8Gb (Gigabit) chips may be used as 4Gb/2Gb chips. In order to achieve different densities for the same type of chips, a set of trims is generally adopted to select the same arrays of all the banks of the full-chip for trimming. Such a method is relatively simple in design, but not flexible enough. In order to utilize these chips whose arrays are partially damaged, considering that damaged arrays of different banks may be completely different, the method of selecting the same arrays of all the banks of the full-chip for trimming is obviously defective.

[0037] It should be understood that the banks refer to physical memory banks in the DRAM or the bank refers to logic storage repositories in the DRAM. A chip may include multiple banks, for example, the chip may include 8 banks. Each bank may include multiple arrays, and the number of the arrays in each bank represents the data bit-width of the chip. Each array includes multiple memory cells.

[0038] In a possible implementation, a semiconductor memory may be a DRAM. FIG. 1 is a diagram of composition structural of a DRAM in the related art. As shown in FIG. 1, a controller 10 is configured to control two DIMMs (Dual-Inline-Memory-Modules) 101, and each DIMM 101 includes at least two DIMM dies 1011.

[0039] In view of the foregoing technical problems, an embodiment of the disclosure provides a method for density configuration of a bank of a semiconductor memory. As shown in FIG. 2, the method includes the operation S202 to S210 including:

[0040] In S202, determining a target bank to be configured of the memory.

[0041] It should be understood that the memory may be a DRAM of the megabit-level monolithic storage density or may be another semiconductor memory which supports the trim function; and the target bank may be any bank to be configured of the memory. In an example, a bank may be an implementation of a memory block. Taking a chip including 16 banks as an example, when the 16 banks are Bank0 to Bank15 respectively, the target bank may be any one of the Bank0 to Bank15. For example, the target bank may be Bank8 or Bank0.

[0042] In some possible implementations, determining the target bank to be configured of the memory may include: determining each bank of the memory as the target bank to be configured, when each bank of the memory is required to be configured.

[0043] According to some embodiments, a density of the target bank is determined according to a density of the memory chip. For example, for a 16Gb chip including 16 banks, the density of each bank is 1Gb, i.e., the density of the target bank is 1Gb.

[0044] In S204, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank.

[0045] In some possible implementations, the density configuration parameter of the target bank may include at least one of: a target density of the target bank, a storage region to be trimmed in the target bank, or an available storage region in the target bank.

[0046] It should be understood that a storage region may be an implementation of an array, and the storage region may be represented by “Region”, for example, each bank may be divided into 6 regions, e.g., Region<5:0> including Region<0> to Region<5>, where Region<5> may be one of the storage regions.

[0047] In an example, the density of the target bank Bank8 without being damaged or trimmed may be 1Gb, and the target density of Bank8 may be less than or equal to 1Gb, for example, the target density may be (1/8)Gb, (1/4)Gb, (1/2)Gb, (2/3)Gb, or the like. Therefore, there are two situations as follows.

[0048] First situation: Bank8 includes 6 regions, e.g., Region<5:0>, and Bank8 is not damaged. When the density of 1Gb is required to be changed into the target density of (2/3)Gb to meet the demands, any storage region in Region<3:2>, Region<1:0> and Region<5:4> in Region<5:0> may be determined as the storage region to be trimmed in the target bank Bank8. Since Bank8 is not damaged, all the storage regions may be taken as the available storage region in the target bank.

[0049] It can be seen that when the target bank is not damaged, only the target density of the target bank is required to be determined, and there are three methods for implementing the density configuration.

[0050] Second situation: Bank8 includes 6 regions, e.g., Region<5:0>, and Region<1:0> is damaged. When the density of 1Gb is required to be changed into the target density of (2/3)Gb to meet the demands, Region<1:0> in Region<5:0> may be determined as the storage region to be trimmed in the target bank Bank8, and the remaining Region<5:2> is taken as the available storage region in the target bank. When the density of 1Gb is required to be changed into the target density of (1/3)Gb, the available storage region in the target bank may be Region<3:2>, and Region<1:0> and Region<5:4> may be determined as the storage region to be trimmed in the target bank Bank8.

[0051] It can be seen that when the target bank is ~~not~~ damaged, the corresponding remaining region may be taken as the available storage region in the target bank, and the

storage region including the damaged region is required to be determined as the storage region to be trimmed according to the determined target density of the target bank.

[0052] Determining the density configuration parameter of the target bank may include: determining the density configuration parameter of the target bank according to the damage information of the target bank and the density configuration requirement of the target bank.

[0053] In S206, determining, based on the density configuration parameter of the target bank, a target code from a set of codes of the target bank, the target code corresponding to a storage region to be trimmed in the target bank.

[0054] It should be understood that the set of codes of the target bank may be the codes representing different storage regions to be trimmed among the storage regions of the target bank. For example, each code among the set of codes of the target bank may be represented by trim_halfGoodBnk<1:0> or Density<1:0>, where trim_halfGoodBnk<1:0> or Density<1:0> may be 00, 01, 10, or 11. For example, trim_halfGoodBnk<1:0>=00 may represent that there is no storage region to be trimmed in Region<5:0> of the target bank Bank8; trim_halfGoodBnk<1:0>=01 may represent that the storage region to be trimmed in Region<5:0> of the target bank Bank8 is Region<5:4>; trim_halfGoodBnk<1:0>=10 may represent that the storage region to be trimmed in Region<5:0> of the target bank Bank8 is Region<3:2>; and trim_halfGoodBnk<1:0>=11 may represent that the storage region to be trimmed in Region<5:0> of the target bank Bank8 is Region<1:0>.

[0055] In an example, the target code is determined according to the storage region to be trimmed in the target bank, for example, the target code may be 10 when the storage region to be trimmed is Region<3:2>.

[0056] In a possible implementation, determining, based on the density configuration parameter of the target bank, the target code from the set of codes of a target bank may include: determining the target code corresponding to any storage region to be trimmed corresponding to the target density from the set of codes of the target bank according to the target density of the target bank, when the target bank is determined to be not damaged.

[0057] For example, the density of the target bank Bank8 without being damaged may be 1Gb, and Bank8 includes 6 regions, e.g., Region<5:0>. When the target density is (2/3)G, and trim_halfGoodBnk<1:0> or Density<1:0> may be 00, 01, 10, 11 which represent different storage regions to be trimmed, any code representing (2/3)G may be selected as the target code from the set of codes represented by rim_halfGoodBnk<1:0> or Density<1:0>, and therefore the target code may be any of 01, 10 or 11.

[0058] In another possible implementation, determining, based on the density configuration parameter of the target bank, the target code from the set of codes of a target bank may include: when the target bank is determined to be damaged, determining a storage region to be trimmed and an available storage region according to a damaged storage region and the target density, and determining the target code from the set of codes of the target bank according to the storage region to be trimmed and the available

storage region. It should be understood that the determined target code is unique, when the sum of the target density and the density of the damaged storage region is equal to the density of the target bank without being damaged.

[0059] For example, the density of the target bank Bank8 without being damaged may be 1Gb, and Bank8 includes 6 regions, e.g., Region<5:0>. When Region<5:4> is damaged, and when the target density is (2/3)G and trim_halfGoodBnk<1:0> or Density<1:0> may be 00, 01, 10, 11 which represent different storage regions to be trimmed, a code representing the storage region to be trimmed (i.e., Region<5:4>) may be selected, from the set of codes represented by trim_halfGoodBnk<1:0> or Density<1:0>, as the target code, and therefore the target code is unique, i.e., 01.

[0060] In S208, generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank.

[0061] It should be understood that the region selection signal is a target output level obtained by performing logic operation on the target code.

[0062] In S210, trimming, based on the region selection signal, the storage region to be trimmed to configure the density of the target bank.

[0063] It should be understood that trimming the storage region may be performed by changing a logic level of the storage region. For example, the level of the storage region before trimming may be low, and after the level of the storage region is converted from low to high, the storage region can be trimmed.

[0064] In a possible implementation, trimming, based on the region selection signal, the storage region to be trimmed to configure the density of the target bank may include: determining, according to the region selection signal, to apply a high voltage (high level) to the storage region to be trimmed, and to apply a low voltage (low level) to at least one storage region, other than the storage region to be trimmed, in the target bank so as to change a logic level of the storage region to be trimmed to trim the storage region to be trimmed and configure the density of the target bank.

[0065] According to the embodiments of the disclosure, since the density configuration parameters of different target banks to be configured may be different, the target codes determined based on the different density configuration parameters may be different, and the region selection signals generated based on the different target codes may further be different. Therefore, different storage regions to be trimmed of different target banks to be configured can be trimmed through different region selection signals, so that the storage region to be trimmed can be flexibly selected, thereby improving the effective utilization rate of the density configuration of the banks of the semiconductor memory.

[0066] An embodiment of the disclosure further provides a method for density configuration of a bank of a semiconductor memory, which includes the operations 101 to 117 including:

[0067] In 101, determining a target bank to be configured of the memory.

[0068] In 103, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank.

[0069] In 105, determining, when the density configuration parameter of the target bank includes a storage region to be trimmed in the target bank or an available storage region in the target bank, the storage region to be trimmed based on the storage region to be trimmed or the available storage region.

[0070] It should be understood that the available storage region may be at least one storage region in the target bank other than the storage region to be trimmed.

[0071] In some possible implementations, determining the storage region to be trimmed based on the storage region to be trimmed or the available storage region may include: determining a damaged region in the target bank, determining the available storage region based on the damaged region, and then determining the storage region to be trimmed.

[0072] In an example, the density of the target bank Bank8 may be 1Gb, and Bank8 includes 6 regions, e.g., Region<5:0>. When the target density is (~~8Gb~~ 2/3)Gb and Region<5:4> is damaged, the storage region to be trimmed may be determined as Region<5:4>; when the target density is (1/3)~~4~~Gb and Region<5:4> is damaged, the storage region to be trimmed may be determined as Region<5:2> or determined as Region<1:0> and Region<5:4>.

[0073] In 107, determining a target code from a set of codes of the target bank based on the storage region to be trimmed, each code among the set of codes of the target bank corresponding to at least one storage region to be trimmed in the target bank.

[0074] In a possible implementation, determining the target code from the set of codes of the target bank based on the storage region to be trimmed may include: determining a code corresponding to the storage region to be trimmed from the set of codes of the target bank according to the storage region to be trimmed, regardless of whether the target bank is damaged or not. For example, when the storage region to be trimmed is determined as Region<5:4>, a code 01 corresponding to Region<5:4> is determined as the target code.

[0075] In 109, determining, when the density configuration parameter of the target bank includes a target density of the target bank, multiple codes corresponding to the density configuration parameter of the target bank from a set of codes of the target bank.

[0076] It should be understood that the multiple codes corresponding to the density configuration parameter of the target bank may be determined from the set of codes of the target bank directly according to the target density of the target bank and the density of the target bank without being damaged, when the storage regions of the target bank are not damaged. For example, the density of the target bank Bank8 may be 1Gb, and Bank8 includes 6 regions, e.g., Region<5:0>. When the target density is (2/3)Gb and Bank8 is not damaged, the multiple codes corresponding to the target density of the target bank are determined as 01, 10 and 11 from the set of codes including 00, 01, 10 and 11.

[0077] In 111, randomly selecting a code as the target code from the multiple codes corresponding to the density configuration parameter of the target bank, the target code corresponding to a storage region to be trimmed in the target bank.

[0078] In a possible implementation, the densities of storage regions to be trimmed which correspond to the respective codes among the multiple codes corresponding to the density configuration parameter of the target bank are same, and the target bank is not damaged, therefore, any one of the multiple codes corresponding to the density configuration parameter of the target bank may be taken as the target code.

[0079] In 113, determining a row address of the storage region to be trimmed in the target bank based on the target code.

[0080] Herein, the row address of the storage region to be trimmed in the target bank may be a 16-bit row address, e.g., Ra<15:0>, and Ra<15>, Ra<14> and Ra<13> represent a high 3-bit address of the row address.

[0081] It should be understood that the storage region to be trimmed may be determined according to the target code, and the row address of the storage region to be trimmed may be determined according to the storage region to be trimmed.

[0082] In some possible implementations, row addresses corresponding to different storage regions to be trimmed in the target bank may be different. For example, the density of the target bank Bank8 is 1Gb, and Bank8 includes 6 regions, e.g., Region<5:0>. Memory addresses corresponding to the storage regions to be trimmed (e.g., Region<4> and Region<5>) in the target bank are different, where the high 3-bit address of the row address of Region<4> is 100, and the high 3-bit address of the row address of Region<5> is 101.

[0083] In 115, generating, based on the target code and the row address of the storage region to be trimmed, a region selection signal configured to select the storage region to be trimmed in the target bank.

[0084] In some possible implementations, generating, based on the target code and the row address of the storage region to be trimmed, the region selection signal configured to select the storage region to be trimmed in the target bank may include: inputting the target code and the row address of the storage region to be trimmed into a logic circuit including a NAND gate, the logic gate circuit being configured to output the region selection signal configured to select the storage region to be trimmed in the target bank.

[0085] In 117, trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

[0086] According to the embodiments of the disclosure, when the density configuration parameter of the target bank includes the storage region to be trimmed in the target bank or the available storage region in the target bank, the storage region to be trimmed may be determined according to the storage region to be trimmed in the target bank or the available storage region in the target bank, and the code corresponding to the storage region to be trimmed is determined as the target code; when the density

configuration parameter of the target bank includes the target density of the target bank, multiple codes corresponding to the target density of the target bank may be determined, and any one of the multiple codes may be taken as the target code. In such way, since the density configuration parameter is determined according to the actual situation of the target bank, the determined target code corresponds to the storage region to be trimmed which is determined according to the actual situation of the target bank, so that the determined target code can better meet the actual demands of the actual density configuration. Moreover, since the region selection signal is generated according to the target code and the row address of the storage region to be trimmed simultaneously, the determined region selection signal may be used to perform the trimming of the storage region to be trimmed in the target bank accurately.

[0087] An embodiment of the disclosure provides a method for density configuration of a bank of a semiconductor memory, which includes the operations 201 to 213 including:

[0088] In 201, determining a target bank to be configured of the memory.

[0089] In 203, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank.

[0090] In 205, determining a target code from a set of codes of the target bank based on the density configuration parameter of the target bank, the target code corresponding to a storage region to be trimmed in the target bank.

[0091] In 207, determining the storage region to be trimmed in the target bank based on the target code.

[0092] In 209, performing logic processing on the target code and a row address of the storage region to be trimmed corresponding to the target code to obtain a target level~~, the row address of the storage region to be trimmed being a high-bit address in a row address of the target bank, and the high-bit address being configured to distinguish different storage regions in the target bank~~.

[0093] In a possible implementation, performing the logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code to obtain the target level may include: performing the logic processing on the target code and a high-bit address of the row address of the storage region to be trimmed corresponding to the target code to obtain the target level. Here, the high-bit address is configured to distinguish different storage regions in the target bank.

~~[0093]~~[0094] It should be understood that the high-bit address of the row address of the storage region to be trimmed may be a high 3-bit address or a high 2-bit address in the row address. In an example, the density of the target bank Bank8 is 1Gb, and Bank8 includes 6 regions, e.g., Region<5:0>. The high 3-bit address of the row address of the storage region to be trimmed (e.g., Region<4>) is 100, and the high 3-bit address of the row address of the storage region to be trimmed (e.g., Region<5>) is 101.

[0094][0095] In an example, the target code may be understood as a mapping factor configured to map the row address.

[0095][0096] In a possible implementation, performing the logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code to obtain the target level may include: inputting the target code and the row address of the storage region to be trimmed corresponding to the target code into a decoder including a NAND gate, and performing logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code through the decoder to obtain the target level after the logic processing.

[0096][0097] In 211, taking the target level as a region selection signal; and

[0097][0098] In 213, trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

[0098][0099] According to the embodiments of the disclosure, logic processing is performed on the target code and the high-bit address of the row address of the storage region to be trimmed corresponding to the target code, the target level obtained through the logic processing is taken as the region selection signal. Since the target level is obtained by mapping the high-bit address of the row address by taking the code corresponding to the storage region to be trimmed as the mapping factor, the obtained region selection signal may be used to perform the trimming of the storage region to be trimmed more accurately.

[0099][00100] An embodiment of the disclosure provides a method for density configuration of a bank of a semiconductor memory, which includes the operations 301 to 311 including:

[00100][00101] In 301, determining a target bank to be configured of the memory.

[00101][00102] In 303, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank.

[00102][00103] In 305, determining a maximum density of the target bank, when the density configuration parameter of the target bank includes a target density of the target bank.

[00103][00104] It should be understood that the maximum density of the target bank may be the density of the target bank without being damaged or trimmed. For example, the maximum density of the target bank may be 1Gb.

[00104][00105] In 307, determining, when the target density is less than the maximum density, a target code from a set of codes of the target bank based on the target density, the target code corresponding to a storage region to be trimmed in the target bank.

[00105][00106] It should be understood that during the density configuration of the target bank of the semiconductor memory, the target density must be less than or equal to

the maximum density of the target bank, i.e., the density of the target bank can only be configured to be less than the maximum density of the target bank, and the density of the target bank cannot be configured to be greater than the maximum density of the target bank. For example, when the maximum density of the target bank of the semiconductor memory is 1Gb, the target density is required to be less than or equal to 1Gb, and cannot be greater than 1Gb.

[~~00106~~][00107] In a possible implementation, determining, when the target density is less than the maximum density, the target code from the set of codes of the target bank based on the target density may include: determining, when the target density of the target bank is less than the maximum density of the target bank, a density of the storage region to be trimmed according to a difference between the maximum density and the target density; determining whether the target bank has a damaged region or not; in response to determining that the target bank has a damaged region, determining the damaged region and a density of the damaged region, and determining the storage region to be trimmed according to the density of the storage region to be trimmed, the damaged region and the density of the damaged region; and determining a code corresponding to the storage region to be trimmed as the target code from the set of codes of the target bank.

[~~00107~~][00108] In another possible implementation, determining, when the target density is less than the maximum density, the target code from the set of codes of the target bank based on the target density may include: determining, when the target density of the target bank is less than the maximum density of the target bank, a density of the storage region to be trimmed according to a difference between the maximum density and the target density; determining whether the target bank has a damaged region or not; in response to determining that the target bank has no damaged region, determining, as the storage region to be trimmed, any storage region with the same density as the storage region to be trimmed; and determining a code corresponding to the storage region to be trimmed as the target code from the set of codes of the target bank.

[~~00108~~][00109] In 309, generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank.

[~~00109~~][00110] In 311, trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

[~~00110~~][00111] According to the embodiment of the disclosure, the target code is determined from the set of codes of the target bank based on the target density when the target density of the target bank is determined to be less than the maximum density. In such a way, the density of banks of the semiconductor memory can be configured reasonably.

[~~00111~~][00112] An embodiment of the disclosure provides another method for density configuration of a bank of a semiconductor memory, which includes the operations 401 to 411 including:

[~~00112~~][00113] In 401, determining a target bank to be configured of the memory, the target bank including at least two logic storage regions, each of the at least two logic

storage regions includes at least two consecutive physical storage regions, and a storage region to be trimmed in the target bank including at least two consecutive physical storage regions to be trimmed.

[~~00113~~][00114] In a possible implementation, a density of the target bank is 1G, and the target bank may include 6 regions, e.g., Region<5:0>, where Region<1:0> may be a logic storage region 1, Region<3:2> may be a logic storage region 2, and Region<5:4> may be a logic storage region 3, i.e., the target bank includes three logic storage regions. Region<0> to Region<5> may include physical storage regions 1 to 6, where the logic storage region 1 may include consecutive Region<0> and Region<1>, the logic storage region 2 may include consecutive Region<2> and Region<3>, and the logic storage region 3 may include consecutive Region<4> and Region<5>. It can be seen that each logic storage region includes two consecutive physical storage regions.

[~~00114~~][00115] In 403, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank.

[~~00115~~][00116] In 405, determining, when the density configuration parameter of the target bank includes the physical storage regions to be trimmed in the target bank, a logic storage region to be trimmed from the at least two logic storage regions in the target bank based on the at least two consecutive physical storage regions to be trimmed in the target bank.

[~~00116~~][00117] It should be understood that according to the embodiment of the disclosure, the trimming is performed in a unit of a logic storage region, i.e., as long as any physical storage region in the logic storage region is damaged, the logic storage region in which the physical storage region is located is required to be trimmed. For example, for the logic storage region Region<1:0>, when the physical storage region Region<1> is damaged, the logic storage region Region<1:0> in which Region<1> is located is required to be trimmed.

[~~00117~~][00118] In some possible implementations, determining, when the density configuration parameter of the target bank includes the physical storage regions to be trimmed in the target bank, a logic storage region to be trimmed from the at least two logic storage regions in the target bank based on the physical storage regions to be trimmed in the target bank may include: determining, as the logic storage region to be trimmed, a logic storage region including the physical storage regions to be trimmed among the at least two logic storage regions in the target bank, when the density configuration parameter of the target bank includes the physical storage regions to be trimmed in the target bank.

[~~00118~~][00119] In 407, determining a target code from a set of codes of the target bank based on the logic storage region to be trimmed, the target code corresponding to the storage region to be trimmed in the target bank.

[~~00119~~][00120] It should be understood that the logic storage region to be trimmed may be an implementation of the storage region to be trimmed.

[00120][00121] In 409, generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank.

[00121][00122] In 411, trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

[00122][00123] According to the embodiment of the disclosure, the minimum unit of the trimming for the target bank is determined as a logic storage region, and if the physical storage region belonging to the logic storage region is damaged, the logic storage region in which the physical storage region is located is required to be trimmed, so that the possibility of missing the trimming for the damaged storage region can be reduced.

[00123][00124] An embodiment of the disclosure provides another method for density configuration of a bank of a semiconductor memory, which includes the operations 501 to 521 including:

[00124][00125] In 501, determining a target bank to be configured of the memory, the target bank including at least two logic storage regions, each of the at least two logic storage regions including at least two consecutive physical storage regions.

[00125][00126] In 503, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank, and the density configuration parameter of the target bank including a target density of the target bank.

[00126][00127] In 505, determining a density of each physical storage region in the target bank.

[00127][00128] It should be understood that the density of each physical storage region is equal to a ratio of a total density of the target bank to the number of the physical storage regions in the target bank. For example, if the total density of the target bank is 1Gb and the number of the physical storage regions is 6, the density of each physical storage region is (1/6)Gb.

[00128][00129] In 507, determining the number of the consecutive physical storage regions in each logic storage region.

[00129][00130] In an example, the number of the consecutive physical storage regions in each logic storage region may be 2, or may be an integer larger than 2.

[00130][00131] In a possible implementation, the number of the consecutive physical storage regions in each logic storage region is determined according to the number of bits of each code among of the set of codes of the target bank and the number of the physical storage regions in the target bank.

[00131][00132] In 509, determining, based on the number of the consecutive physical storage regions in each logic storage region and the density of each physical storage region, a density of the logic storage region.

[~~00132~~][00133] In some possible implementations, determining, based on the number of the consecutive physical storage regions in each logic storage region and the density of each physical storage region, the density of the logic storage region may include: determining a product of the number of the consecutive physical storage regions in each logic storage region and the density of each physical storage region as the density of the logic storage region. For example, if the number of the consecutive physical storage regions in each logic storage region is 2 and the density of each physical storage region is (1/3)Gb, the density of each logic storage region is (2/3)Gb.

[~~00133~~][00134] In 511, determining a maximum density of the target bank.

[~~00134~~][00135] It should be understood that the maximum density of the target bank may be the density of the target bank without being damaged or trimmed. Determining the maximum density of the target bank may include obtaining the maximum density from factory test data of the semiconductor memory.

[~~00135~~][00136] In a possible implementation, the maximum density of the target bank Bank8 is 1Gb and Bank8 includes 6 physical storage regions, e.g., Region<5:0>, where every two consecutive physical storage regions are determined as a logic storage region, so that a logic storage region 1 (e.g., Region<1:0>), a logic storage region 2 (e.g., Region<3:2>) and a logic storage region 3 (e.g., Region<5:4>) are formed. It can be seen that the density of each physical storage region is (1/6)Gb and the density of each logic storage region is (1/3)Gb.

[~~00136~~][00137] In 513, determining at least one configurable density of the target bank based on the density of each logic storage region and the maximum density of the target bank, the density of each logic storage region being a sum of densities of respective physical storage regions in the logic storage region.

[~~00137~~][00138] According to an embodiment, if the logic storage region includes two physical storage regions and the density of each physical storage region is (1/6)Gb, the density of the logic storage region is (1/3)Gb.

[~~00138~~][00139] According to an embodiment, determining the at least one configurable density of the target bank based on the density of each logic storage region and the maximum density of the target bank may include: determining a difference between the maximum density of the target bank and an integer multiple of the density of each logic storage region as the at least one configurable density of the target bank. For example, if the maximum density of the target bank is 1Gb and the density of the logic storage region is (1/3)Gb, the at least one configurable density of the target bank may include (1/3)Gb, (2/3)Gb and 1Gb, each of which is an integer multiple of (1/3)Gb.

[~~00139~~][00140] In 515, determining an actual density to be configured based on the at least one configurable density and the target density.

[~~00140~~][00141] In a possible implementation, determining the actual density to be configured based on the at least one configurable density and the target density may include: comparing the at least one configurable density and the target density, and determining, as the actual density to be configured, a configurable density among the at

least one configurable density that is closest to and less than the target density.

[~~00141~~][00142] It should be understood that when the maximum density of the target bank is 1Gb, and when the density of the logic storage region is (1/3)Gb and the target density is (5/6)Gb, the at least one configurable density may include at least (1/3)Gb and (2/3)Gb. Since (2/3)Gb is the configurable density closest to (5/6)Gb ((5/6)Gb is not an integer multiple of the density of the logic storage region), the actual density to be configured may be determined to be (2/3)Gb.

[~~00142~~][00143] In 517, determining, when the actual density is inconsistent with the target density, a target code from a set of codes of the target bank based on the actual density, the target code corresponding to a storage region to be trimmed in the target bank.

[~~00143~~][00144] It should be understood that because the configurable density may be actually implemented or obtained, when the actual density is inconsistent with the target density, the target code may be determined from the set of codes of the target bank according to the actual density.

[~~00144~~][00145] In 519, generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank.

[~~00145~~][00146] In 521, trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

[~~00146~~][00147] According to the embodiment of the disclosure, the density of each logic storage region may be determined according to the density of each physical storage region and the number of the consecutive physical storage regions in the logic storage region; the at least one configurable density of the target bank may be determined according to the density of each logic storage region and the maximum density of the target bank; and the actual density to be configured may be determined according to the at least one configurable density and the target density of the target bank; and the target code may be determined based on the actual density, when the actual density is inconsistent with the target density.

[~~00147~~][00148] An embodiment of the disclosure provides another method for density configuration of a bank of a semiconductor memory, which includes the operations 601 to 623 including:

[~~00148~~][00149] In 601, determining a target bank to be configured of the memory, the target bank including at least two logic storage regions, each of the at least two logic storage regions including at least two consecutive physical storage regions.

[~~00149~~][00150] In 603, determining a density configuration parameter of the target bank, the density configuration parameter being configured to represent a density to be configured for the target bank, and the density configuration parameter of the target bank including a target density of the target bank.

[~~00150~~][00151] In 605, determining a density of each physical storage region in the

target bank.

[00151][00152] In 607, determining the number of bits of each code among a set of codes of the target bank.

[00152][00153] It should be understood that the number of bits of each code among the set of codes of the target bank is determined according to the number of logic storage regions in the target bank. For example, if the number of bits of each code among the set of codes of the target bank is 2, the number of the logic storage regions cannot be larger than the power of 2.

[00153][00154] In 609, determining the number of physical storage regions in each logic storage region based on the number of physical storage regions in the target bank and the number of bits of each code.

[00154][00155] In some possible implementations, determining the number of physical storage regions in each logic storage region based on the number of physical storage regions in the target bank and the number of bits of each code may include: determining, according to the number of bits of each code, the maximum number of logic storage regions capable of being distinguished by the set of codes of the target bank; and determining the number of consecutive physical storage regions in each logic storage region according to the determined maximum number of the logic storage regions and the number of physical storage regions.

[00155][00156] According to an embodiment, determining the number of consecutive physical storage regions in each logic storage region according to the determined maximum number of logic storage regions and the number of physical storage regions may include: determining the number of the consecutive physical storage region in each logic storage region to be 1, when the maximum number of the logic storage regions is greater than or equal to the number of the physical storage regions; determining the number of the consecutive physical storage regions in each logic storage region to be 2, when the maximum number of the logic storage regions is less than the number of the physical storage regions and twice the maximum number of the logic storage regions is greater than the number of the physical storage regions.

[00156][00157] For example, if the number of bits of each code among the set of codes of the target bank is 2, and the number of the physical storage regions is 6, the maximum number of the logic storage regions (which is determined based on the number of bits of each code among the set of codes of the target bank being 2) may be determined to be 4. It is clear that the maximum number 4 of the logic storage regions is less than the number 6 of the physical storage regions, but twice the maximum number of the logic storage regions (i.e., 8) is greater than the number 6 of the physical storage regions, and thus the number of the consecutive physical storage regions in each logic storage region may be determined to be 2.

[00157][00158] For another example, if the number of bits of each code among the set of codes of the target bank is 3, and the number of the physical storage regions is 6, the maximum number of the logic storage regions (which is determined based on the number of bits of each code among the set of codes of the target bank being 3) may be

determined to be 8. It is clear that the maximum number 8 of the logic storage regions is greater than the number 6 of the physical storage regions, and thus the number of the consecutive physical storage region in each logic storage region may be determined to be 1.

[~~00158~~][00159] In 611, determining, based on the number of consecutive physical storage regions in each logic storage region and the density of each physical storage region, a density of the logic storage region.

[~~00159~~][00160] In a possible implementation, determining, based on the number of consecutive physical storage regions in each logic storage region and the density of each physical storage region, the density of the logic storage region may include: determining a product of the number of the consecutive physical storage regions in each logic storage region and the density of each physical storage region to be the density of the logic storage region. For example, if the number of the consecutive physical storage regions in each logic storage region is 2 and the density of each physical storage region is (1/6)Gb, the density of each logic storage region may be determined to be (1/3)Gb.

[~~00160~~][00161] In 613, determining a maximum density of the target bank.

[~~00161~~][00162] In 615, determining at least one configurable density of the target bank based on the density of each logic storage region and the maximum density of the target bank, the density of each logic storage region being a sum of densities of respective physical storage regions in the logic storage region.

[~~00162~~][00163] In 617, determining an actual density to be configured based on the at least one configurable density and the target density.

[~~00163~~][00164] In 619, determining, when the actual density is inconsistent with the target density, a target code from the set of codes of the target bank based on the actual density, the target code corresponding to a storage region to be trimmed in the target bank.

[~~00164~~][00165] In 621, generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank.

[~~00165~~][00166] In 623, trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

[~~00166~~][00167] According to the embodiment of the disclosure, the number of the consecutive physical storage regions in each logic storage region may be accurately determined according to the number of bits of each code among the set of codes of the target bank and the number of the physical storage regions in the target bank.

[~~00167~~][00168] According to the embodiment of the disclosure, if the maximum density of the target bank without being damaged or trimmed is 1Gb, the density of (2/3)Gb may be implemented by trim. The target bank is divided into 6 regions, e.g., Region<5:0>, if the density of the target bank is 1G, all the 6 regions including Region<5:0> are utilized; if the density of the target bank is (2/3)G, 4 regions are

selected from the 6 regions including Region<5:0>. For example, a die of a DRAM may include 16 banks, and the density of each bank may be 1Gb (which means that the bank includes at least 2^30 storage capacitors; in fact, the DRAM further includes redundant storage capacitors, and if the density of the bank is 1Gb, the bank includes more than 2^30 storage capacitors), thus the density of the full die may reach 16Gb. If partial storage capacitors of a die cannot work due to manufacturing process or other reasons, the density of the die may be configured to 12Gb, 8Gb, 4Gb or 2Gb through trim, so that the DRAM die may be utilized as much as possible, when the partial storage capacitors cannot work.

Table 1

trim_halfGoodBnk<1:0>				Density
00	Region<0,1>	Region<2,3>	Region<4,5>	1G
01	Region<0,1>	Region<2,3>		(2/3)G
10	Region<0,1>		Region<4,5>	(2/3)G
11		Region<2,3>	Region<4,5>	(2/3)G

~~[00168]~~[00169] With reference to Table 1, it can be seen that when trim_halfGoodBnk<1:0>=01, 4 regions including Region<3:0> are selected and Region<4,5> is trimmed to implement the density of (2/3)G; when trim_halfGoodBnk<1:0>=10, 4 regions including Region<1:0> and Region<5:4> are selected and Region<3,2> is trimmed to implement the density of (2/3)G; when trim_halfGoodBnk<1:0>=11, 4 regions including Region<5:2> are selected and Region<1:0> is trimmed to implement the density of (2/3)G.

~~[00169]~~[00170] FIG. 3a is a structural diagram of storage regions and addresses of a full-chip according to an embodiment of the disclosure. As shown in FIG. 3a, the full-chip includes 16 banks, where the number of bits of a row control line guided by the row control 301 is 16; Bank4, Bank6, Bank5, Bank7, Bank0, Bank2, Bank1 and Bank3 are distributed on the left side; and Bank8, Bank10, Bank9, Bank11, Bank 12, Bank 14, Bank 13 and Bank 15 are distributed on the right side.

~~[00170]~~[00171] FIG. 3b is an enlarged structural diagram of Bank8 of FIG. 3a according to an embodiment of the disclosure. As shown in FIG. 3b, Bank 8 includes 6 physical storage regions from Region<0> to Region<5>, where the 6 regions from Region<0> to Region<5> are encoded by Ra<15>, Ra<14> and Ra<13> in a row address Ra<15:0>. It can be seen that a code corresponding to Region<0> is 000; a code corresponding to Region<1> is 001; a code corresponding to Region<2> is 010; a code corresponding to Region<3> is 011; a code corresponding to Region<4> is 100; and a code corresponding to Region<5> is 101.

~~[00171]~~[00172] FIG. 3c is a structural diagram of Bank8 after trimming according to an embodiment of the disclosure. As shown in FIG. 3c, two consecutive physical storage regions (i.e., Region<4> and Region<5>) of Bank8 are trimmed to change the density of Bank8 from 1Gb to (2/3)Gb. For example, Region<4> and Region<5> may be the

damaged physical storage regions, or may be any two consecutive physical storage regions randomly selected when each physical storage region from Region<0> to Region<5> is not damaged.

[~~00172~~][00173] According to the embodiment of the disclosure, in the process of generating, based on the target code, the region selection signal configured to select the storage region to be trimmed in the target bank, the target code is required to be decoded. Herein, three region selection signals (e.g., Ra1514<0>, Ra1514<1> and Ra1514<2>) are defined. The relations between (Ra1514<0>, Ra1514<1>, and Ra1514<2>) and each storage region may be understood with reference to Table 2.

Table 2

Ra1514<0>		Ra1514<1>		Ra1514<2>	
Ra13=0	Ra13=1	Ra13=0	Ra13=1	Ra13=0	Ra13=1
Region<0>	Region<1>	Region<2>	Region<3>	Region<4>	Region<5>

[~~00173~~][00174] As shown in Table 2, Ra1514<0> represents 2 regions including Region<0,1>; Ra1514<1> represents 2 regions including Region<2,3>; and Ra1514<2> represents 2 regions including Region<4,5>.

[~~00174~~][00175] The region selection signal (e.g., Ra1514<0>, Ra1514<1>, Ra1514<2>) may be obtained by performing logic processing on a target code and a high 2-bit address (Ra<15> and Ra<14>) of Bank8 through a logic circuit.

[~~00175~~][00176] Before obtaining the region selection signal (e.g., Ra1514<0>, Ra1514<1>, Ra1514<2>), some intermediate signals may be determined, such as a signal obtained by performing logic NOT operation on the target code, a signal obtained by performing logic NOT operation on Ra<15:14>, and the like.

[~~00176~~][00177] FIG. 3d is a logic circuit diagram of performing logic NOT operation on a target code according to an embodiment of the disclosure. As shown in FIG. 3d, DensityTrim<1:0> represents the target code, and DensityTrimB<1:0> may be obtained by performing logic NOT operation on DensityTrim<1:0>.

[~~00177~~][00178] FIG. 3e is a logic circuit diagram of performing logic NOT operation on a high 2-bit address according to an embodiment of the disclosure. As shown in FIG. 3e, Ra<15:14> is the high 2-bit address, and RaB<15:14> may be obtained by performing logic NOT operation on Ra<15:14>.

[~~00178~~][00179] FIG. 3f is a logic circuit diagram of performing logic operation on DensityTrim<0> and DensityTrim<1> according to an embodiment of the disclosure. As shown in FIG. 3f, S11N may be obtained by performing logic NAND operation on DensityTrim<0> and DensityTrim<1>, and S11 may be obtained by performing logic NOT operation on S11N.

[~~00179~~][00180] FIG. 3g is a logic circuit diagram of performing logic operation on

DensityTrimB<0> and DensityTrimB<1> according to an embodiment of the disclosure. As shown in FIG. 3g, S00N may be obtained by performing logic NAND operation on DensityTrimB<0> and DensityTrimB<1>, and S00 may be obtained by performing logic NOT operation on S00N.

[~~00180~~][00181] FIG. 3h is a logic circuit diagram of obtaining the region selection signal Ra1514<0> based on a target code and a high 2-bit address according to an embodiment of the disclosure. As shown in FIG. 3h, Ra1514<0> may be obtained by performing logic NOT operation on a logic result which is obtained by performing logic NAND operation on RaB<15>, RaB<14> and S11N.

[~~00181~~][00182] FIG. 3i is a logic circuit diagram of obtaining the region selection signal Ra1514<1> based on a target code and a high 2-bit address according to an embodiment of the disclosure. As shown in FIG. 3i, logic NAND operation is performed on RaB<15>, RaB<14> and S11 to obtain a first logic result; and logic NAND operation is performed on RaB<15>, Ra<14> and DensityTrimB<1> to obtain a second logic result; and logic NAND operation is performed on the first logic result and the second logic result to obtain Ra1514<1>.

[~~00182~~][00183] FIG. 3j is a logic circuit diagram of obtaining the region selection signal Ra1514<2> based on a target code and a high 2-bit address according to an embodiment of the disclosure. As shown in FIG. 3j, logic NAND operation is performed on Ra<15>, RaB<14> and S00 to obtain a third logic result; logic NAND operation is performed on RaB<15>, Ra<14> and DensityTrim<1> to obtain a fourth logic result; and logic NAND operation is performed on the third logic result and the fourth logic result to obtain Ra1514<2>.

[~~00183~~][00184] According to the embodiments of the disclosure, there are multiple options for density configuration of a target bank, which may be understood with reference to Table 3.

Table 3

Density<1:0>			
00 (1G)	Ra1514<0>	Ra1514<1>	Ra1514<2>
01 ((2/3) G)	Ra1514<0>	Ra1514<2>	Ra1514<2>=0
10 ((2/3) G)	Ra1514<0>	Ra1514<1>=0	Ra1514<2>
11 ((2/3) G)	Ra1514<0>=0	Ra1514<1>	Ra1514<2>

[~~00184~~][00185] As shown in Table 3, Density<1:0> may represent different densities. Density<1:0> is 00 which represents that the density of the target bank is 1G, and Ra1514<0> to Ra1514<2> are all 1 which represents that Region<0> to Region<5> are all 1 (because Ra1514<0> represents Region<0,1>, Ra1514<1> represents Region<2,3>, and Ra1514<2> represents Region<4,5>), i.e., available.

[~~00185~~][00186] Density<1:0> is 01 which represents that the density of the target bank

is (2/3)G, and Ra1514<0> and Ra1514<1> are 1 and Ra1514<2> is 0 which represent that Region<0> to Region<3> are all 1 (available) and Region<4> and Region<5> are 0 (unavailable) (because Ra1514<0> represents Region<0,1>, Ra1514<1> represents Region<2,3>, and Ra1514<2> represents Region<4,5>).

[~~00186~~][00187] Density<1:0> is 10 which represents that the density of the target bank is (2/3)G, and Ra1514<0> and Ra1514<2> are 1 and Ra1514<1> is 0 which represent that Region<0>, Region<1>, Region<4> and Region<5> are all 1 (available) and Region<2> and Region<3> are 0 (unavailable) (because Ra1514<0> represents Region<0,1>, Ra1514<1> represents Region<2,3>, and Ra1514<2> represents Region<4,5>).

[~~00187~~][00188] Density<1:0> is 11 which represents that the density of the target bank is (2/3)G, and Ra1514<0> is 0 and Ra1514<1> and Ra1514<2> are ~~0~~ 1 which represent that Region<0> and Region<1> are 0 (unavailable) and Region<2> to Region<5> are all 1 (available) (because Ra1514<0> represents Region<0:1>, Ra1514<1> represents Region<2:3>, and Ra1514<2> represents Region<4:5>).

[~~00188~~][00189] FIG. 4 illustrates a structural diagram of a system for density configuration of a bank of a semiconductor memory according to an embodiment of the disclosure. As shown in FIG. 4, the system structure includes a read-write system 401, a control unit 402, a decoding unit 403 and a bank 404. Ra<12:0> in a row address line Ra<15:0> guided by the read-write system 401 is directly connected to the bank 404, and Ra<15:13> is connected to the control unit 402. The control unit 402 is configured to input Ra<15:13> and the generated DensityTrim<1:0> into the decoding unit 403. The decoding unit 403 is connected to the bank 404, and the decoding unit 403 is configured to perform logic operation on Ra<15:13> and DensityTrim<1:0> to obtain a region selection signal, and transmit the obtained region selection signal to the bank 404. The bank 404 is configured to trim a corresponding region to be trimmed according to the region selection signal to configure the density of the bank.

[~~00189~~][00190] It should be understood that the decoding unit 403 may be implemented by the circuits shown in FIG. 3h to FIG. 3j. The reference may be made in the foregoing description.

[~~00190~~][00191] According to the embodiment of the disclosure, different encoding states of Ra1514<2:0> correspond to different regions of the bank 404, for example, the region corresponding to Ra1514<2:0>=100 is Region<0:1>.

[~~00191~~][00192] Furthermore, an embodiment of the disclosure further provides a semiconductor memory, which supports the methods for density configuration of the bank of the semiconductor memory according the foregoing embodiments. FIG. 5 is a structural diagram of the semiconductor memory according to the embodiment of the disclosure. As shown in FIG. 5, the semiconductor memory includes a target bank 501, an address processing unit 502, a code obtaining unit 503 and a region selection signal generation unit 504 and a trim unit 505.

[~~00192~~][00193] The target bank 501 includes at least two storage regions.

[~~00193~~][00194] The address processing unit 502 is configured to output an address of the target bank 501, here, an output terminal of the address processing unit 502 is connected to the target bank 501.

[~~00194~~][00195] The code obtaining unit 503 is configured to receive a target code, here, the target code corresponds to at least one storage region to be trimmed in the target bank 501.

[~~00195~~][00196] The region selection signal generation unit 504 is configured to generate, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank 501, here, an output terminal of the region selection signal generation unit ~~503~~ 504 is connected to an input terminal of a trim unit 505.

[~~00196~~][00197] The trim unit 505 is configured to trim the storage region to be trimmed based on the region selection signal to configure a density of the target bank 501, here, an output terminal of the trim unit 505 is connected to the target bank 501.

[~~00197~~][00198] According to some embodiments, the semiconductor memory further includes: a control unit, configured to determine the target bank 501 to be configured of the semiconductor memory; to determine a density configuration parameter of the target bank 501, here, the density configuration parameter is configured to represent the density to be configured for the target bank 501; and to determine the target code from a set of codes of the target bank 501 based on the density configuration parameter of the target bank 501, here, the target code corresponds to the storage region to be trimmed in the target bank 501. An output terminal of the control unit is connected to the code obtaining unit.

[~~00198~~][00199] According to some embodiments, the address processing unit 502 includes: a row address processing unit, configured to output a row address of the target bank 501, here, an output terminal of the row address processing unit is connected to an input terminal of the region selection signal generation unit and the target bank 501; a column address processing unit, configured to output a column address of the target bank 501, here, an output terminal of the column address processing unit is connected to the target bank 501; and a bank address processing unit, configured to output a bank address of the target bank 501, here, an output terminal of the bank address processing unit is connected to the target bank 501. The region selection signal generation unit 503 is configured to perform logic processing on the target code and a row address of the storage region to be trimmed corresponding to the target code to obtain a target level, and take the target level as the region selection signal.

[~~00199~~][00200] According to some embodiments, an output terminal of a high-bit address in the row address processing unit is connected to the input terminal of the region selection signal generation unit; here, the high-bit address is configured to distinguish different storage regions in the target bank 501.

[~~00200~~][00201] According to some embodiments, the region selection signal generation unit 503 includes a logic gate circuit including a NAND gate and a NOT gate, here, an input terminal of the logic gate circuit includes a signal line corresponding to the target

code and a signal line corresponding to the row address of the storage region to be trimmed; and the logic gate circuit is configured to perform logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code to obtain the target level, and to take the target level as the region selection signal.

[~~00201~~][00202] According to some embodiments, the region selection signal generation unit 503 includes a decoder. Here, an input terminal of the decoder is a signal line corresponding to the target code; and each level output by the decoder is taken as the region selection signal when the level is valid, and each output terminal of the decoder is connected to the input terminal of the trim unit.

[~~00202~~][00203] The semiconductor memory according to the embodiments of the disclosure is similar to the methods for density configuration of the bank of the semiconductor memory according to the foregoing embodiments. The technical features not disclosed in detail according to the embodiments of the disclosure can be understood with reference to the foregoing embodiments, which will not be repeated herein.

[~~00203~~][00204] The embodiments of the disclosure provide the semiconductor memory. Considering that the density configuration parameters of different target banks to be configured of the semiconductor memory may be different, the target codes determined based on the different density configuration parameters may further be different, and the region selection signals generated based on the different target codes may further be different. Therefore, different storage regions to be trimmed of different target banks to be configured can be trimmed through different region selection signals, so that the storage region(s) to be trimmed can be flexibly selected, and the effective utilization rate of the density configuration of the banks of the semiconductor memory is improved.

[~~00204~~][00205] It should be understood that in the embodiments of the disclosure, the disclosed devices and methods may be implemented in a non-targeted manner. The foregoing device embodiments are merely illustrative. For example, the division of the units is only a logical function division. In actual implementation, there may be other division methods. For example, a plurality of units or components may be combined, or may be integrated into another system, or some features may be ignored or not implemented.

[~~00205~~][00206] The features disclosed in the method or device embodiments of the disclosure may be combined arbitrarily without conflict to obtain new method or device embodiments.

[~~00206~~][00207] The foregoing description is merely for the illustration of specific embodiments of the disclosure. The scope of protection of the disclosure is not limited thereto. Those skilled in the art may make modifications or substitutions within the technical scope of the disclosure, which shall fall within the scope of the disclosure. Therefore, the scope of protection of the disclosure shall be defined by the scope of the claims.

INDUSTRIAL APPLICABILITY

[~~00207~~][00208] In the embodiments of the disclosure, since the density configuration parameters of different target banks to be configured may be different, the target codes determined based on the different density configuration parameters may be different, and the region selection signals generated based on the different target codes may further be different. Therefore, different storage regions to be trimmed of different target banks to be configured can be trimmed through different region selection signals, so that the storage region to be trimmed can be flexibly selected, thereby improving the effective utilization rate of the density configuration of the banks of the semiconductor memory.

CLAIMS

1. A method for density configuration of a bank of a semiconductor memory, comprising:

determining a target bank to be configured of the memory;

determining a density configuration parameter of the target bank, wherein the density configuration parameter is configured to represent a density to be configured for the target bank;

determining, based on the density configuration parameter of the target bank, a target code from a set of codes of the target bank, wherein the target code corresponds to a storage region to be trimmed in the target bank;

generating, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank; and

trimming the storage region to be trimmed based on the region selection signal to configure the density of the target bank.

2. The method of claim 1, wherein the density configuration parameter of the target bank comprises at least one of:

a target density of the target bank,
the storage region to be trimmed in the target bank, or
an available storage region in the target bank.

3. The method of claim 2, wherein in response to determining that the density configuration parameter of the target bank comprises the storage region to be trimmed in the target bank or the available storage region in the target bank,

determining, based on the density configuration parameter of the target bank, the target code from the set of codes of the target bank comprises:

determining the storage region to be trimmed based on the storage region to be trimmed or the available storage region; and

determining, based on the storage region to be trimmed, the target code from the set of codes of the target bank, wherein each code among the set of codes of the target bank corresponds to at least one storage region to be trimmed in the target bank.

4. The method of claim 2 or 3, wherein in response to determining that the density configuration parameter of the target bank comprises the target density of the target bank,

determining, based on the density configuration parameter of the target bank, the target code from the set of codes of the target bank comprises:

determining, from the set of codes of the target bank, a plurality of codes corresponding to the density configuration parameter of the target bank; and

randomly selecting, from the plurality of codes corresponding to the density configuration parameter of the target bank, a code as the target code.

5. The method of any of claims 1 to 4, wherein generating, based on the target code, the region selection signal configured to select the storage region to be trimmed in the target bank comprises:

determining, based on the target code, a row address of the storage region to be trimmed in the target bank; and

generating, based on the target code and the row address of the storage region to be trimmed, the region selection signal configured to select the storage region to be trimmed in the target bank.

6. The method of claim 5, wherein generating, based on the target code and the row address of the storage region to be trimmed, the region selection signal configured to select the storage region to be trimmed in the target bank comprises:

performing logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code, to obtain a target level; and

taking the target level as the region selection signal.

7. The method of claim 6, wherein performing logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code, to obtain the target level comprising:

performing the logical processing on the target code and a high-bit address of the row address of the storage region to be trimmed, to obtain the target level~~the row address of the storage region to be trimmed is a high-bit address of the row address of the storage region to be trimmed~~, the high-bit address being configured to distinguish different storage regions in the target bank.

8. The method of any of claims ~~4~~ 2 to 7, wherein in response to determining that the density configuration parameter of the target bank comprises the target density of the target bank,

determining, based on the density configuration parameter of the target bank, the target code from the set of codes of the target bank comprises:

determining a maximum density of the target bank; and

determining, based on the target density, the target code from the set of codes of the target bank, in response to the target density being less than the maximum density.

9. The method of any of claims ~~5~~ 2 to ~~7~~8, wherein the target bank comprises at least two logic storage regions, and each of the at least two logic storage regions comprises at least two consecutive physical storage regions; wherein the storage region to be trimmed in the target bank comprises at least two consecutive physical storage regions to be trimmed; and

wherein in response to determining that the density configuration parameter of the target bank comprises the physical storage regions to be trimmed in the target bank,

determining, based on the density configuration parameter of the target bank, the target code from the set of codes of the target bank comprises:

determining, based on the at least two consecutive physical storage regions to be trimmed in the target bank, a logic storage region to be trimmed from the at least two logic storage regions in the target bank; and

determining, based on the logic storage region to be trimmed, the target code from the set of codes of the target bank.

10. The method of any of claims 1 to 7, wherein the density configuration parameter of the target banks comprises a target density of the target bank; wherein the target bank comprises at least two logic storage regions, and each of the at least two logic storage regions comprises at least two consecutive physical storage regions; and

wherein determining, based on the density configuration parameter of the target bank, the target code from the set of codes of the target bank comprises:

determining a density of each logic storage region and a maximum density of the target bank;

determining at least one configurable density of the target bank based on the density of each logic storage region and the maximum density of the target bank, wherein the density of each logic storage region is a sum of densities of respective physical storage regions in the logic storage region;

determining, based on the at least one configurable density and the target density, an actual density to be configured; and

determining, based on the actual density, the target code from the set of codes of the target bank, in response to the actual density being inconsistent with the target density.

11. The method of claim 10, further comprising:

determining a density of each physical storage region in the target bank;

determining a number of the consecutive physical storage regions in each logic storage region; and

determining, based on the number of the consecutive physical storage regions in each logic storage region and the density of each physical storage region, the density of the logic storage region.

12. The method of claim 11, wherein determining the number of the consecutive physical storage regions in each logic storage region comprises:

determining a number of bits of each code among the set of codes of the target bank; and

determining the number of the physical storage regions in each logic storage region based on a number of the physical storage regions in the target bank and the number of bits of each code.

13. A semiconductor memory, comprising:

a target bank, comprising at least two storage regions;

an address processing unit, configured to output an address of the target bank, wherein an output terminal of the address processing unit is connected to the target bank;

a code obtaining unit, configured to receive a target code, wherein the target code corresponds to at least one storage region to be trimmed in the target bank;

a region selection signal generation unit, configured to generate, based on the target code, a region selection signal configured to select the storage region to be trimmed in the target bank, wherein an output terminal of the region selection signal generation unit is connected to an input terminal of a trim unit; and

the trim unit, configured to trim the storage region to be trimmed based on the region selection signal to configure a density of the target bank, wherein an output terminal of the trim unit is connected to the target bank.

14. The semiconductor memory of claim 13, further comprising:

a control unit, configured to:

determine the target bank to be configured of the semiconductor memory;

determine a density configuration parameter of the target bank, wherein the density configuration parameter is configured to represent the density to be configured for the target bank; and

determine, based on the density configuration parameter of the target bank, the target code from a set of codes of the target bank, wherein the target code corresponds to the storage region to be trimmed in the target bank,

wherein an output terminal of the control unit is connected to the code obtaining unit.

15. The semiconductor memory of claim 13 or 14, wherein the address processing unit comprises:

a row address processing unit, configured to output a row address of the target bank, wherein an output terminal of the row address processing unit is connected to an input terminal of the region selection signal generation unit and the target bank;

a column address processing unit, configured to output a column address of the target bank, wherein an output terminal of the column address processing unit is connected to the target bank; and

a bank address processing unit, configured to output a bank address of the target bank, wherein an output terminal of the bank address processing unit is connected to the target bank;

wherein the region selection signal generation unit is configured to perform logic processing on the target code and a row address of the storage region to be trimmed corresponding to the target code to obtain a target level, and take the target level as the region selection signal.

16. The semiconductor memory of claim 15, wherein an output terminal of a high-bit address in the row address processing unit is connected to the input terminal of the region selection

signal generation unit; and

wherein the high-bit address is configured to distinguish different storage regions in the target bank.

17. The semiconductor memory of claim 15 or 16, wherein the region selection signal generation unit comprises: a logic gate circuit comprising a NAND gate and a NOT gate;

an input terminal of the logic gate circuit comprises a signal line corresponding to the target code and a signal line corresponding to the row address of the storage region to be trimmed; and

the logic gate circuit is configured to perform logic processing on the target code and the row address of the storage region to be trimmed corresponding to the target code to obtain the target level, and take the target level as the region selection signal.

18. The semiconductor memory of claim 15 or 16, wherein the region selection signal generation unit comprises a decoder;

wherein an input terminal of the decoder is a signal line corresponding to the target code; and

each level output by the decoder is taken as a region selection signal when the level is valid, and each output terminal of the decoder is connected to the input terminal of the trim unit.