

Description

The invention relates to a switch mode power supply (SMPS). In particular, the invention relates to a SMPS that derives a rectified input supply voltage from an AC, mains supply voltage to produce an output supply voltage.

Typically, such SMPS employs a full wave rectifier bridge that rectifies a sinusoidal mains supply voltage and charges an input filter capacitor to produce the rectified input supply voltage. The filter capacitor has a sufficiently large value for reducing, in the input supply voltage, the magnitude of a ripple at the fundamental frequency and at the harmonics of the mains supply voltage. In this way, ripple voltage is prevented from occurring in the output supply voltage.

The filter capacitor draws narrow pulses of input current having a high peak value from the mains supply voltage source. The current pulses occur only at the peaks of the sinusoidal mains supply voltage. Therefore, the waveform of the input current contains undesirable low frequency harmonics of the mains supply voltage frequency. The result is an undesirable decrease in the power factor to about 0.65 and an undesirable increase in distortions of the waveform of the mains supply voltage. Recently, an interest has evolved for revising European Standard EN60555-2 for the purpose of reducing the permissible low frequency harmonic content of the waveform of the input current. It may be desirable to reduce the low frequency harmonic content of the waveform of the input current without significantly increasing a ripple voltage in the output supply voltage.

In an SMPS, embodying an aspect of the invention, an AC mains supply voltage produced in a mains supply voltage source is rectified to form a rectified mains supply voltage. The rectification operation occurs without low-pass filtering with respect to low frequency voltage components. A winding of a flyback transformer is coupled to the rectified, mains supply voltage, and to a switching transistor. Pulses of current at high frequency that are produced in the transformer by switching operation of the transistor produce an output supply voltage that is applied to a load. The peak amplitudes of the current pulses have an envelope that is similar to a waveform of the rectified voltage. Consequently, a ratio between the mains supply voltage and a mains supply current remains constant, during at least a substantial portion of the mains supply voltage. Pulses of current that are produced in the transformer are stored in a capacitor. Pulses of current are produced from the stored charge in the capacitor and re-circulated through the transformer in subsequent cycles, during a portion of the period of the mains supply voltage when the mains supply voltage is low. The re-circulated current is applied to the load so as to reduce a ripple voltage

in the output supply voltage.

A switch mode power supply, embodying a further aspect of the invention, includes a source of an AC, mains supply voltage, an inductance and a first switching arrangement coupled to the mains source and responsive to a switching signal. A first plurality of current pulses are generated in the inductance at a frequency that is substantially higher than that of the mains supply voltage. During a first portion of a given period remote from a peak of the mains supply voltage, when the mains supply voltage decreases, the decrease causes a concurrent decrease in amplitudes of the first plurality of current pulses and in a level of a mains supply current supplied from the mains source. Second switching arrangement is coupled to the inductance for generating a second plurality of current pulses in the inductance at a frequency that is substantially higher than that of the mains supply voltage. The second plurality of current pulses are generated at least during the first portion of the given period of the mains supply voltage. An output supply voltage and an output supply current are generated in a load circuit from the first and second pluralities of current pulses.

It is known from JP-A 58 141 680, to eliminate the input filter capacitor of a switching regulator in order to improve its power factor. Such an arrangement as shown in either figure 2 or figure 6 of said reference uses the charge on a load capacitor to supply current to the switching regulator during those periods of the mains cycle when the voltage is too low.

FIGURE 1 illustrates an SMPS, embodying an aspect of the invention, that utilizes a current interleaving technique;

FIGURES 2a-2k illustrate waveforms useful for explaining the operation of the SMPS of FIGURE 1;

FIGURES 3a and 3b illustrate additional waveforms useful for explaining the operation of the SMPS of FIGURE 1;

FIGURE 4 illustrates an SMPS, embodying another aspect of the invention, that utilizes a current superposition technique;

FIGURES 5a-5f illustrate waveforms useful for explaining the operation of the SMPS of FIGURE 4;

FIGURES 6a and 6b illustrate additional waveforms for the SMPS of FIGURE 4;

FIGURE 7 illustrates an SMPS, embodying a further aspect of the invention; and

FIGURES 8a and 8b are waveforms useful for explaining the operation of the SMPS of FIGURE 7.

FIGURE 1 illustrates an SMPS 100, embodying an aspect of the invention, that utilizes a technique, referred to herein as current interleaving technique. A mains supply voltage source 107 that produced an AC voltage VM is coupled to a full-wave bridge rectifier 102 that produces an AC full-wave rectified input sup-

ply voltage V1 in a relatively small filter capacitor C1. AC voltage VM of source 107 is sinusoidal at, for example, a frequency of 50 Hz. Because of the small capacitance of capacitor C1, voltage VM is rectified without significant low-pass filtering with respect to the frequency of voltage VM. Therefore, low frequency harmonics of voltage V1 are not filtered out. Voltage V1, that is a fullwave rectified voltage, is coupled via a switching diode D1 to a primary winding W1 of a flyback transformer T.

A switching signal V0, having a controllable duty cycle, is coupled via an "OR" gate 113 to produce a switching signal V16. Signal V16 is coupled via a conventional driver stage 103 to a base of a switching transistor Q1 to turn on transistor Q1 only when signal V0 is at a HIGH level. The frequency of signal V0 is selected to be within a range of 20-50 KHz, as determined by an oscillator, not shown, of a control circuit 101.

In a given cycle of signal V0, after signal V0 attains the HIGH level, magnetic energy is stored in transformer T and an upramping current i_{p1} or i_p is produced in winding W1. In such given cycle, immediately after signal V0 becomes LOW, transistor Q1 becomes non-conductive and a flyback operation occurs to produce a flyback pulse current i_{s1} in a given secondary winding of transformer T. The collector voltage of transistor Q1 is limited by means of a snubber circuit that includes a capacitor C8, a resistor R6 and a diode D8.

As a result of flyback current pulses i_{s1} that are produced from pulses i_{p1} , an output supply voltage V2 and an output supply voltage V6 are produced in capacitors C2 and C6. Voltages V2 and V6 are produced by rectifying, in diodes D2 and D6, flyback pulse voltages of secondary windings W2 and W6, respectively, of transformer T when transistor Q1 becomes nonconductive. Voltages V2 and V6 may be used for energizing loads such as a horizontal output stage and an audio stage, respectively, of a television receiver, not shown.

Transformer T may be used for isolating, with respect to electrical shock hazard, source 107 and a "hot" ground conductor, H, from a "cold" ground conductor G. Secondary windings W3, W4 and W5 produce flyback pulse voltages that are rectified by diodes D3, D4 and D5 to produce DC, rectified voltages V3, V4 and V5 with low ripple in filter capacitors C3, C4 and C5, respectively. Voltages V3, V4 and V5 are referenced to hot ground conductor H. Whereas, voltages V2 and V6 are referenced to cold ground conductor G.

DC sense voltage V3 that is indicative of voltages V2 and V6 is applied to a differential amplifier, not shown, of a regulator control stage 105 of circuit 101. Voltage V3 is compared with a reference voltage, not shown. An error voltage, not shown, is produced from a difference between voltage V3 and the reference

voltage. The error voltage is used to control, in a conventional manner, a pulse-width or duty cycle of signal V0 to regulate the levels of output voltages V2 and V6. When signal V0 is HIGH, transistor Q1 is conductive, and a pulse of a current i_{p1} flows via diode D1 to provide current i_p in winding W1.

A ratio between the peak amplitudes of the pulses of current i_{p1} and between the instantaneous value of voltage VM or of full-wave rectified voltage V1 is maintained constant throughout the period of voltage VM or V1. Since voltage V1 has a full-wave rectified sinusoidal waveform, the peaks or envelope of current i_{p1} also varies in full-wave rectified sinusoidal manner. Consequently, an AC current i_m that is supplied from source 107 varies, advantageously, in a sinusoidal manner at the frequency and phase of voltage VM, and with relatively small amount of low order harmonics distortion.

The amplitudes of the pulses of current i_{p1} significantly decrease, during a given period of voltage V1, when voltage V1 decreases. Therefore, had only current i_{p1} been produced in winding W1, voltage V2 would tend to have a significant ripple voltage. It may be desirable to reduce the ripple voltage.

FIGURES 2a-2k illustrate waveforms useful for explaining the operation of SMPS 100 of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2k indicate similar items or functions. The falling edge of signal V0 of FIGURE 2b triggers a monostable multivibrator (MMV) 104 of FIGURE 1 that produces a signal V14 at a LOW level with a predetermined pulse width. Signal V14 is coupled to a base of a switching transistor Q4 via a pulse shaping parallel arrangement of a resistor R5 and a capacitor C7. As a result of the falling edge of signal V0, signal V14 of MMV 104 attains the LOW level and transistor Q4 becomes nonconductive. The collector of transistor Q4 is coupled to a base of a series pass switching transistor Q2 to control the switching operation of transistor Q2.

Transistor Q2 is switched on by a drive current that is supplied via an arrangement formed by a transistor Q3 and resistors R1, R2, R3 and R4. Transistors Q3 and Q2 are turned on when transistor Q4 becomes nonconductive, immediately following the falling edge of signal V0. Forward-biased transistor Q2 couples DC voltage V4 to an anode of a switching diode D7 having a cathode that is coupled to a junction terminal Ta, between a cathode of diode D1 and winding W1. As long as transistor Q1 is nonconductive, following the falling edge of signal V0, no current is supplied to winding W1 via diode D7 and transistor Q2.

The falling edge of signal V0 of FIGURE 2b also triggers a sawtooth generator, not shown, in stage 105 that produces a sawtooth signal V13 of FIGURE 2e. Sawtooth signal V13 is compared in a comparator COMP2 with a controllable slicing voltage V10. Voltage V10 has a level that is shown as a broken line in FIGURE 2e. For a given cycle of voltage VM or V1 of

FIGURE 1, voltage V10 is constant. Immediately after the falling edge of signal V0, when signal V13 is smaller than voltage V10, an output signal V11 of comparator COMP2 is at a LOW level. Signal V11 is applied to a reset input of a flip-flop (F-F) 106. F-F 106 is not affected by signal V11, as long as signal V11 is at the LOW level. Prior to the falling edge of signal V0, signal V11 is at the HIGH level. Consequently, signal V11 maintains an output signal V7 of F-F 106 at the LOW level.

An unrectified, flyback voltage V15, across winding W3, is indicative of an instant when the magnetic energy in transformer T, or a secondary current is, becomes zero. Current i_s or i_{s1} becomes zero following the falling edge of signal V0. Circuit 105 generates a narrow pulse signal V12 of FIGURE 2d when current i_s of FIGURE 2c becomes zero. The leading edge of pulse signal V12 of FIGURE 2d triggers F-F 106 of FIGURE 1 to a "set" state. As a result, output signal V7 of FIGURE 2g of F-F 106 of FIGURE 1 attains a HIGH level immediately after the magnetic energy has decayed in transformer T.

Transistor Q1 is also controlled by signal V7 that is coupled via "OR" gate 113. Signals V0 and V7 cannot occur simultaneously at the active HIGH levels. When, in a given cycle, signal V7 attains the HIGH level, transistor Q1 begins conducting. In accordance with an inventive feature, transistor Q2, that is already forward biased, as explained before, begins conducting a pulse of a current i_{p2} in winding W1, and diode D1 becomes back-biased. In a given cycle of signal V0, for example, primary current i_{p2} increases in an upramping manner until F-F 106 is reset by signal V11. As a result, a pulse of current i_{s2} is produced in a given secondary winding of transformer T in a flyback mode of operation. The pulses of currents i_{p2} and i_{s2} are shown in broken lines in FIGURES 2a and 2c. When current i_{s2} ceases, the pulse of signal V12 of FIGURE 2d is produced but has no effect on F-F 106 since F-F 106 is already reset.

Signal V14 of FIGURE 2i, at the LOW level, changes to the HIGH level, prior to the occurrence of a rising edge of signal V0 of FIGURE 2b, in accordance with pulse-width determining parameters of MMV 104. When signal V14 becomes HIGH, transistor Q4 becomes conductive that causes transistor Q2 to become nonconductive. A new cycle begins at the rising edge of the following pulse of signal V0 of FIGURE 2b. Signal V14 remains at the HIGH level until signal V0 attains the LOW level, so as to maintain transistor Q2 nonconductive.

The time difference between the falling edge of signal V0 and the leading edge of signal V12 or V7 varies as a function of the instantaneous value of voltage V1 or VM or the peak of current i_{p1} or i_{s1} within a given period of voltage V1 or VM. The smaller is voltage V1, the earlier is the occurrence of the leading edge of signal V7. Voltage V10 is constant for a given

period of voltage V1. Therefore, signal V11 attains the HIGH level and signal V7 attains the LOW level at the same time, with respect to signal V0, in each cycle throughout the period voltage V1. Thus, the pulse-width of signal V7 is modulated or varies during the period of voltage V1. The pulse-width of signal V7 decreases when voltage V1 or current i_{p1} increases, and vice versa. When, for example, voltage V1 is zero, the pulse-width of signal V7 is at a maximum. During the given period of voltage V1 of FIGURE 1, as voltage V1, for example, decreases, the peaks of the pulses of current i_{p1} or current i_{s1} of FIGURE 2a and FIGURE 2c, respectively, also decrease, as shown in solid lines.

In accordance with an aspect of the invention, during a portion of the period of voltage V1 of FIGURE 1, when the peaks of the pulses of current i_{p1} of FIGURE 2a or current i_{s1} of FIGURE 2c, for example, decrease, the peak and pulse-width of each of the pulses of current i_{p2} or i_{s2} increase, as shown in broken lines in FIGURES 2a and 2c. When the pulse-width and amplitude of the pulses of, for example, current i_{s2} of FIGURE 2c increase, additional energy is supplied to the load. The additional energy is supplied to the load via current i_{s2} of FIGURE 1 when the energy that is supplied to the load by the pulses of current i_{p1} or i_{s1} is diminished. Therefore, the reduction in the amplitude of the pulses of current i_{p1} or i_{s1} that tends to produce the ripple voltage in, for example, voltage V2 is, advantageously, reduced by the current pulses of current i_{p2} or i_{s2} .

It may be desirable to, for example, increase the pulse-width of the pulses of signal V7 in each cycle of signal V7 when the loading of capacitor C2 increases so as to control current i_{p2} . To that end, current i_{p2} is controlled by controlling the pulse-width of signal V7 in a close loop manner. The pulse-width of signal V7 is determined by set and reset signals V12 and V11, as explained before. Signal V12 ensures that the pulse of current i_{p2} starts to flow after the pulse of secondary current i_{s1} has decayed to zero. Signal V11 determines the amplitude of current i_{p2} .

In the closed-loop operation, signal V7 is demodulated by applying signal V7 via a low pass filter LPF1. A resulting low-pass filtered signal V8 has a waveform that is illustrated in FIGURE 2j. During a first portion of the cycle of voltage VM, signal V8 varies as a function of $\cos \omega t$, where "t" denotes time and " ω " denotes the radian velocity; whereas, voltage VM of FIGURE 1 varies as a function of $\sin \omega t$. Thus, pulse-width modulated signal V7 is transformed to an equivalent signal, signal V8, having an amplitude and a DC, average level that are determined in accordance with the pulse-width of signal V7. Signal V8 provides a relative measure for the power required to compensate for a reduction in the input power derived from mains supply voltage source 107, during a given period of voltage V1. For example, at mains voltage

VM zero crossing, the input power from source 107 is zero. When the input power from source 107 is zero, a maximum pulse-width of signal V7 and a peak of signal V8 occur, indicating that SMPS 100 requires maximum power compensation via the pulses of current ip2. On the other hand, in a second portion of the cycle of voltage V1 or VM, in the vicinity of an instant when the input power is at a maximum, signal V8 is a minimum, as shown in broken lines, and no power compensation is required.

Signal V8 is compared with a reference voltage VR in a comparator COMP1. The level of voltage VR is shown in FIGURE 2j as a broken line. An output signal V9 of comparator COMP1 is produced when signal V8 is smaller than voltage VR. Signal V9 is applied to an input of a second low pass filter LPF2. Low pass filter LPF2 produces slicing voltage V10 that is used as a slicing level for comparator COMP2.

Assume, for example, that an increase in loading of capacitor C2 occurs. Therefore the pulse of signal V12 and the leading edge of signal V7 occur later in a given cycle of signal V0. Therefore, the pulse-width of each of the pulses of signal V7 tends to decrease, throughout the period of voltage VM. The result is that the average value of signal V8 becomes less positive. The decrease in the average value of signal V8 of FIGURE 2j tends to increase the pulse-width of signal V9 of FIGURE 2k. As a result, the level of voltage V10 becomes more positive. Consequently, the leading edges of the pulses of signal V11 of FIGURE 2f are more delayed or occur later within a given period of, for example, signal V0. Therefore, advantageously, the pulse-width of signal V7 in each cycle, when signal V7 occurs, increases. The increase in the pulse-width of signal V7 causes the average value of signal V8 to increase in a manner to attain steady state operation. In this way, steady-state operation is maintained when a change in loading occurs in a manner to vary the amplitude of current is2 as a function of loading.

Signal V11 of FIGURE 2f causes FF 106 to be at the "reset" state throughout an interval, T1, of FIGURE 2g of voltage VM of FIGURE 1. The value of voltage VR of FIGURE 1 determines the length of interval T1 of FIGURE 2g. Throughout interval T1, signal V7 is maintained continuously at the LOW level. Thus, signal V11 prevents the generation of the pulses of current ip2 or is2, throughout interval T1 of FIGURE 2g. Interval T1 occurs in the vicinity of the peak of voltage V1 or VM, when the pulses of current ip1 or is1 are sufficiently large to energize the load. Maintaining interval T1 for an entire range of loading and input voltage VM conditions provides protection feature against an undesirable mode of operation of SMPS 100 of FIGURE 1. For example, had interval T1 not been maintained, capacitor C4 might have been overloaded.

FIGURE 3b illustrates schematically the peaks or

envelope of the pulses of currents ip1 and ip2 in a given period of voltage V1 of FIGURE 2a. Similar symbols and numerals in FIGURES 1, 2a-2k and 3a-3b indicate similar items or functions. During interval T1 of FIGURE 3b that occurs in the vicinity of the peak of voltage V1 of FIGURE 3a, the pulses of current ip2 are disabled. Whereas, during the rest of the period, an interval T2, they are enabled. During interval T2, voltage V4 is larger than voltage V1, for proper operation.

FIGURE 4 illustrates an SMPS 100', embodying another aspect of the invention, that utilizes a technique referred to herein as a current superposition technique. FIGURES 5a-5f illustrate waveforms useful for explaining the operation of SMPS 100' of FIGURE 4. Similar symbols and numerals in FIGURES 1, 4 and 5a-5f indicate similar items or functions, except that in FIGURES 4 and 5a-5f the symbol (') is added.

In FIGURE 4, transistors Q1' and Q2' are, illustratively, MOS transistors. Transistor Q2' is turned on by a voltage V5' that is more positive by about 15V than voltage V4'. Transistor Q2' is turned off by a transistor Q4'. A signal V14' at a HIGH level that is produced in an inverting output $\bar{Q}$ of a flip-flop (FF) 200 causes transistor Q4' to turn on and transistor Q2' to turn off. A protection zener diode D9 limits a gate-source voltage excursions of transistor Q2'. Transistor Q1' is controlled by signals V0' and V7'. Only one of signals V0' and V7' can be at a HIGH level at any one time. Signal V0' controls a primary current component ip1' and signal V7' controls a primary current ip2'. A primary current ip' in a winding W1' is sampled by means of a very low value resistor R31 coupled between the source electrode of transistor Q1' and ground H'. A voltage V31, developed across resistor R31, is proportional to current ip1. Voltage V31 is applied via a low pass filter 202 to remove any existing spikes. A resulting low-pass filtered signal V91 is shown in FIGURE 5a. Signal V91 is compared with a slicing voltage V10' that varies in a closed-loop manner in a comparator 201. Voltage V10' is indicated in FIGURE 5a as a broken line. The slicing level of voltage V10' relative to signal V91 determines the lengths of intervals T1' and T2'. A resulting signal V11' at an output of comparator 201 is illustrated in FIGURE 5c.

A flip-flop (F-F) 200 is set by the falling edge of signal V0' that is coupled via an inverter 200a and reset by the HIGH level of signal V11'. Output signal V7' developed in a non-inverting output Q of F-F 200 is applied to an input of an OR-gate 113'. Signal V14' developed at inverting output $\bar{Q}$ of F-F 200 is coupled to a resistor R5' and to a capacitor C7'. The parallel combination of resistor R5' and capacitor C7' improves the switching characteristics of transistor Q4'. Control signal V0' is applied to the other input OR-gate 113'.

During a portion of a given cycle of, for example, signal V0', F-F 200 is reset, non-inverting output sig-

nal V7' is at the LOW level and inverting output signal V14' is HIGH. Therefore, transistors Q1' and Q2' are turned off and transistor Q4' is turned on. Signal V0' changes, during its cycle, from the LOW to the HIGH level. The change in signal V0' causes transistor Q1' to conduct and each of primary current i_{p1}' and signal V91 to increase in an upramping manner. Should signal V91 reach the level of voltage V10' when signal V0' is at the HIGH level, comparator 201 output signal V11' would attain the HIGH level.

After a predetermined conduction time of transistor Q1', signal V0' changes again to the LOW level that causes signal V91 to be zero. Since signal V91 is also zero, comparator 201 output signal V11' is at the LOW level.

Throughout an interval T1', in the vicinity of the peak of voltage VM', signal V11' attains the HIGH level prior to the instant when signal V0' changes to the LOW level. As a result, F-F 200 cannot be set. Thus, throughout interval T1', control signal V7' remains at the LOW level. Throughout interval T1', after signal V0' changes to the LOW level, primary current i_{p1}' becomes zero. The result is that current i_{p2}' is disabled, throughout interval T1'.

In contrast to the situation during interval T1', during an interval T2' of voltage VM', signal V91 does not reach the level of voltage V10' during the period of signal V0' in which both signal V0' is at the HIGH level and transistor Q1' is conductive. This is so because, during interval T2', the rate of change of current i_{p1}' is smaller than during interval T1' due to the decrease in input voltage VM' or V1'. During interval T2', when signal V0' attains the LOW level, the reset signal V11' is still at the LOW level. Therefore, F-F 200 is set by the falling edge of signal V0'. Thus, when signal V0' becomes LOW, signal V7' changes to the HIGH level.

Transistor Q1' conduction time is now determined by signal V7' which keeps transistor Q1' conducting after signal V0' becomes LOW. The current in transistor Q1' is not disturbed by the fast transition from being controlled by signal V0' to being controlled by signal V7'. Simultaneously, transistor Q4' is turned off by signal V14' which attains the LOW level. Transistor Q2 immediately conducts, a diode D1' becomes nonconductive and a diode D7' becomes conductive. Input supply voltage V1' is decoupled from a winding W1' and a voltage V4' in a capacitor C4' is coupled to winding W1' via transistor Q2'. In cycles that occur during interval T2', primary current i_{p2}' continues to flow without a gap of time relative to current i_{p1}' , as shown in broken lines in FIGURE 5a. Voltage V91 also increases until voltage V91 becomes equal to voltage V10'. Then, comparator 201 output signal V11' becomes HIGH that causes F-F 200 to reset. Transistor Q1' is turned off, transistor Q4' is turned on and transistor Q2' is turned off. Thereafter, a new cycle begins. The result is that the current pulses

of current i_{p2}' are generated from the charge stored in capacitor C4' and are re-circulated via winding W1', during interval T2'.

FIGURE 6b illustrates schematically the peaks or envelope of the pulses of currents i_{p1}' and i_{p2}' in a given period of voltage V1' of FIGURE 5a. Similar symbols and numerals in FIGURES 4, 5a-5f and 6a-6b indicate similar items or functions. During interval T1' of FIGURE 6b, that occurs in the vicinity of the peak of voltage V1' of FIGURE 5a, the pulses of current i_{p2}' are disabled. Whereas, during the rest of the period, interval T2', they are enabled.

It may be desirable to vary current i_{p2}' or i_{s2}' as a function of current loading of, for example, capacitor C2'. This is achieved by controlling signal V11' in a closed-loop manner. To that end, signal V11' is coupled via a low pass filter 203 to an inverting input terminal of a comparator 205. A reference voltage 204 is developed at a noninverting input terminal of comparator 205. An output signal 205a of comparator 205 is coupled via a resistor R9 to a base of a current sinking switching transistor Q5. A collector of transistor Q5 is coupled to a junction terminal between a resistor R6 and a resistor R7. Resistor R6 and R7 are coupled in series between a voltage V3' and a capacitor C9 to generate a current that charges capacitor C9. The average value of a collector current of transistor Q5 determines the level of voltage V10' that is developed in capacitor C9. Thus, capacitor C9 is discharged via transistor Q5 and is charged via resistor R6. In steady state operation, voltage V10' is constant.

Assume that an increase in current loading in capacitor C2' occurs. Therefore, the peak amplitude of current i_{p1}' and of voltage V31 in resistor R31 increase. Therefore, the pulse-width of signal V11' increases. When the pulse-width of signal V11' increases, an output voltage 203a of low-pass filter 203 becomes larger. When voltage 203a exceeds voltage 204 output signal 205a of comparator 205 attains the LOW level. The result is that transistor Q5 is turned off for a longer interval during a given period of, for example, signal V0'. Thus, the average current in transistor Q5 decreases. Therefore, the level of voltage V10' increases. In this way, the peak level of each pulse of current i_{p2}' increases in a manner to transfer more energy to the load.

Upon turning on the SMPS 100' and prior to steady state operation, voltage V10' is undefined and could be 2 or 3 volts higher than in steady state which might allow excessive current to flow. Therefore capacitor C9 is coupled to a voltage divider that includes a resistor R1 and a resistor R2 through a diode D10. Upon switching on the power supply voltage V4' is zero and diode D10 is coupled to ground potential. As a result, voltage V10' can not be greater than 0.6V. As the power supply starts to operate, voltage V4' increases. The voltage level across resistor R2 also increases, thereby allowing voltage V10' to increase.

The voltage divider that includes resistors R1 and R2 causes diode D10 to be in cut off when voltage V4' reaches its nominal value.

FIGURE 7 illustrates an SMPS 100", embodying another aspect of the invention, that utilizes a compromise technique. FIGURES 8a-8b illustrate waveforms useful for explaining the operation of SMPS 100" of FIGURE 7. Similar symbols and numerals in FIGURES 1, 4, 7 and 8a-8b indicate similar items or functions, except that in FIGURES 7 and 8a-8b the symbol ("") is added. In FIGURE 7, switch S1 performs the function of transistors Q1 of FIGURE 1, for example, and switch S2 of FIGURE 7 performs the function of transistor Q2 of FIGURE 1.

Capacitor C4" of FIGURE 7 is charged directly from mains supply voltage VM", and not via the transformer, as in FIGURE 1 or 4. Therefore, a mains current iM" of FIGURE 7 is equal to the sum of the two currents, ip1" and i4. Current ip1" is sinusoidal at the fundamental frequency. Capacitor C4" is charged only during the peaks of mains voltage VM". Thus, current i4 includes narrow, non-sinusoidal current pulses.

The peak value of current i4 is low, because the energy stored in capacitor C4" is used to supply only a portion of a primary current ip" of winding W1". About 65% of the power consumption is obtained by means of current ip1" and 35% by means of current ip2". The resultant current waveform of current iM" is shown in FIGURE 8b. Advantageously, the third harmonic of this current waveform is only about 30% of what it would have been had capacitor C1" been a very large capacitor. The fifth harmonic is also reduced. A control circuit 101" in FIGURE 7 could be of the type, "current interleaving" of FIGURE 1 or of the type, "current superposition" of FIGURE 4.

A comparison between the performances of arrangements of FIGURES 1 and 7, when the mains supply voltage is 220 VAC, the input power is 150W and the output voltage, for example, voltage V2 or V2", is 150 VDC, provides the following results. In the arrangement of FIGURE 1, the harmonic content of current iM in A_{rms} is 0.72 at 50 Hz, 0.05 at 150 Hz, 0.038 at 250 Hz and 0.024 at 350 Hz. The power factor is 0.96, the efficiency is 0.72 and the ripple voltage is 1V. In the arrangement of FIGURE 7, the harmonic content of current iM in A_{rms} is 0.72 at 50 Hz, 0.18 at 150 Hz, 0.126 at 250 Hz and 0.09 at 350 Hz. The power factor is 0.92, the efficiency is 0.78 and the ripple voltage is 0.8V.

The current interleaving technique of FIGURE 1 is particularly suitable for an SMPS with a power rating below, for example, 100W. Whereas, the current super-position technique is suitable for an SMPS with a higher power rating.

Claims

1. A switch mode power supply, comprising:
 - a source (107) of an AC, mains supply voltage (VM);
 - an inductance (W1);
 - first switching means (Q1) coupled to said mains source and responsive to a switching signal (V16) for generating a first plurality of current pulses (ip1, is1) in said inductance at a frequency (20-50 KHz) that is substantially higher than that (50 Hz) of said mains supply voltage such that, during a first portion (T2, Fig. 2g) of a given period remote from a peak of said mains supply voltage, when said mains supply voltage decreases, the decrease causes a concurrent decrease in amplitudes of said first plurality of current pulses and in a level of a mains supply current (iM) supplied from said mains source;
 - characterized by
 - second switching means (Q2) synchronized to said first switching means and coupled to said inductance for generating a second plurality of current pulses (ip2, is2) in said inductance at a frequency that is substantially higher than that of said mains supply voltage, said second plurality of current pulses being generated at least during said first portion of said given period of said mains supply voltage;
 - a load circuit (LOAD); and
 - means (W2) responsive to said first and second pluralities of current pulses for developing an output supply voltage (V2) and an output supply current (iL) in said load circuit.
2. A power supply according to claim 1 further comprising, a rectifier (D2) for rectifying said first (iL1) and second (iL2) pluralities of current pulses to develop said output supply voltage (V2) and said output supply current (iL), such that said second plurality of current pulses compensate for the decrease in said amplitudes of said first plurality of current pulses in a manner to reduce a ripple component at a frequency (100 Hz) that is related to that (50 Hz) of said mains supply voltage.
3. A power supply according to claim 1 wherein said second plurality of current pulses (ip2) are generated in said inductance (W1) and wherein said output supply voltage (V2) is produced in a fly-back manner from said first (ip1) and second (ip2) pluralities of current pulses.
4. A power supply according to claim 1 wherein said current pulses of said first (ip1) and second (ip2) pluralities of current pulses occur in mutually exclusive intervals within a given period of said switching signal (V16).

The voltage divider that includes resistors R1 and R2 causes diode D10 to be in cut off when voltage V4' reaches its nominal value.

FIGURE 7 illustrates an SMPS 100", embodying another aspect of the invention, that utilizes a compromise technique. FIGURES 8a-8b illustrate waveforms useful for explaining the operation of SMPS 100" of FIGURE 7. Similar symbols and numerals in FIGURES 1, 4, 7 and 8a-8b indicate similar items or functions, except that in FIGURES 7 and 8a-8b the symbol (") is added. In FIGURE 7, switch S1 performs the function of transistors Q1 of FIGURE 1, for example, and switch S2 of FIGURE 7 performs the function of transistor Q2 of FIGURE 1.

Capacitor C4" of FIGURE 7 is charged directly from mains supply voltage VM", and not via the transformer, as in FIGURE 1 or 4. Therefore, a mains current iM" of FIGURE 7 is equal to the sum of the two currents, ip1" and i4. Current ip1" is sinusoidal at the fundamental frequency. Capacitor C4" is charged only during the peaks of mains voltage VM". Thus, current i4 includes narrow, non-sinusoidal current pulses.

The peak value of current i4 is low, because the energy stored in capacitor C4" is used to supply only a portion of a primary current ip" of winding W1". About 65% of the power consumption is obtained by means of current ip1" and 35% by means of current ip2". The resultant current waveform of current iM" is shown in FIGURE 8b. Advantageously, the third harmonic of this current waveform is only about 30% of what it would have been had capacitor C1" been a very large capacitor. The fifth harmonic is also reduced. A control circuit 101" in FIGURE 7 could be of the type, "current interleaving" of FIGURE 1 or of the type, "current superposition" of FIGURE 4.

A comparison between the performances of arrangements of FIGURES 1 and 7, when the mains supply voltage is 220 VAC, the input power is 150W and the output voltage, for example, voltage V2 or V2", is 150 VDC, provides the following results. In the arrangement of FIGURE 1, the harmonic content of current iM in A_{rms} is 0.72 at 50 Hz, 0.05 at 150 Hz, 0.038 at 250 Hz and 0.024 at 350 Hz. The power factor is 0.96, the efficiency is 0.72 and the ripple voltage is 1V. In the arrangement of FIGURE 7, the harmonic content of current iM in A_{rms} is 0.72 at 50 Hz, 0.18 at 150 Hz, 0.126 at 250 Hz and 0.09 at 350 Hz. The power factor is 0.92, the efficiency is 0.78 and the ripple voltage is 0.8V.

The current interleaving technique of FIGURE 1 is particularly suitable for an SMPS with a power rating below, for example, 100W. Whereas, the current super-position technique is suitable for an SMPS with a higher power rating.

Claims

1. A switch mode power supply, comprising:
 - a source (107) of an AC, mains supply voltage (VM);
 - an inductance (W1);
 - first switching means (Q1) coupled to said mains source and responsive to a switching signal (V16) for generating a first plurality of current pulses (ip1, is1) in said inductance at a frequency (20-50 KHz) that is substantially higher than that (50 Hz) of said mains supply voltage such that, during a first portion (T2, Fig. 2g) of a given period remote from a peak of said mains supply voltage, when said mains supply voltage decreases, the decrease causes a concurrent decrease in amplitudes of said first plurality of current pulses and in a level of a mains supply current (iM) supplied from said mains source;
 - characterized by
 - second switching means (Q2) synchronized to said first switching means and coupled to said inductance for generating a second plurality of current pulses (ip2, is2) in said inductance at a frequency that is substantially higher than that of said mains supply voltage, said second plurality of current pulses being generated at least during said first portion of said given period of said mains supply voltage;
 - a load circuit (LOAD); and
 - means (W2) responsive to said first and second pluralities of current pulses for developing an output supply voltage (V2) and an output supply current (iL) in said load circuit.
2. A power supply according to claim 1 further comprising, a rectifier (D2) for rectifying said first (iL1) and second (iL2) pluralities of current pulses to develop said output supply voltage (V2) and said output supply current (iL), such that said second plurality of current pulses compensate for the decrease in said amplitudes of said first plurality of current pulses in a manner to reduce a ripple component at a frequency (100 Hz) that is related to that (50 Hz) of said mains supply voltage.
3. A power supply according to claim 1 wherein said second plurality of current pulses (ip2) are generated in said inductance (W1) and wherein said output supply voltage (V2) is produced in a fly-back manner from said first (ip1) and second (ip2) pluralities of current pulses.
4. A power supply according to claim 1 wherein said current pulses of said first (ip1) and second (ip2) pluralities of current pulses occur in mutually exclusive intervals within a given period of said switching signal (V16).



5. A power supply according to claim 1 wherein said second plurality of current pulses (ip2) are generated in said inductance (W1) and wherein a given current pulse of one of said first plurality of current pulses (ip1) occurs adjacent to a given current pulse of said second plurality of current pulses such that there is no time gap between the adjacent pulses. 5
6. A power supply according to claim 1 further comprising, means (COMP 1, COMP 2) for disabling the generation of said second plurality of current pulses (ip2) throughout a second portion (T1, Fig. 2g) of said period of said mains supply voltage (VM), in a vicinity of said peak voltage of said mains supply voltage. 10 15
7. A power supply according to claim 1 further comprising, a pulse-width modulator (101) for pulse-width modulating the current pulses of at least one (ip1, ip2) of said first (ip1) and said second (ip2) plurality of current pulses in accordance with said one of said output supply voltage (V2) and current (IL) in a manner to provide regulation. 20 25
8. A power supply according to claim 7 wherein said pulse-width modulator (101) modulates each of said first (ip1) and second (ip2) pluralities of current pulses in a manner to provide the regulation. 30
9. A power supply according to claim 1 wherein said second plurality of current pulses (ip2) are generated in said inductance and wherein said second plurality of current pulses comprise re-circulated current pulses with respect to said inductance (W1). 35
10. A power supply according to claim 1 wherein said second plurality of current pulses (ip2) are generated in said inductance (W1) and wherein said inductance is included in a first winding (W1) of a transformer (T). 40
11. A power supply according to claim 10 further comprising, a second rectifier (D4) and a capacitor (C4) for rectifying current pulses in a second winding (W4) of said transformer (T) that are produced from said first plurality of current pulses (ip1) to develop a second supply voltage (V4) in said capacitor, said second supply voltage being coupled to said second switching means (Q2) for generating said second plurality of current pulses (ip2) from said second supply voltage. 45 50
12. A power supply according to claim 10 wherein said second switching means (Q2) couples a second supply voltage (V4) to said first winding (W1) of said transformer (T) to generate a given pulse of said second plurality of current pulses (ip2) and wherein said source (107) of mains supply voltage (VM) is simultaneously decoupled from said first winding, during a portion of a given period of said switching signal. 55
13. A power supply according to claim 10 wherein said second plurality of current pulses (ip2) are produced in a current inter-leaving manner (Fig. 1) with respect to said first plurality of current pulses (ip1).
14. A power supply according to claim 10 wherein said second plurality of current pulses (ip2) are produced in a current super-position manner (Fig. 4) with respect to said first plurality of current pulses (ip1).
15. A power supply according to claim 10 further comprising, means (D4", Fig. 7) for generating a second supply voltage (in C4") from said mains supply voltage (VM") via a current path (D4") that excludes said transformer (W1", W2") wherein said second supply voltage is coupled via said second switching means (Q2") to said transformer (W1", W2") for generating said second plurality of current pulses (ip2").
16. A power supply according to claim 10 further comprising, a rectifier (102) coupled to said mains source (107) for rectifying said mains supply voltage (VM) to generate a rectified supply voltage (V1) that is coupled to said transformer (T) wherein said rectified supply voltage is developed from said mains supply voltage without significant low-pass filtering with respect to a frequency (50 Hz) of said mains supply.
17. A power supply according to claim 10 wherein, during said given period of said mains supply voltage (VM), a ratio between an amplitude of a given current pulse of said first plurality of current pulses (ip1) and a level of said mains supply voltage (VM) that prevails during said given current pulse of said first plurality of current pulses is substantially constant for each current pulse.
18. A switch mode power supply, comprising:
a source (107) of an AC, mains supply voltage (VM);
a flyback transformer (T);
a rectifier (102) coupled to said mains source for rectifying said mains supply voltage to develop in a first winding (W1) of said transformer a first rectified supply voltage (V1) such that said rectified supply voltage is developed without low-pass filtering with respect to a frequency (50 Hz) and low order harmonics of said mains supply voltage;



first switching means (Q1) responsive to a switching signal (V16) at a frequency (20-50 KHz) that is substantially higher than a frequency (50 Hz) of said mains supply voltage for generating a first plurality of current pulses (ip1) in said first winding; and

means (W4, D4) generating a second supply voltage (V4);

characterized by

second switching means (Q2) coupled to said transformer and synchronized to said first switching means for coupling said second rectified supply voltage to said transformer and for decoupling said first rectified supply voltage from said transformer to generate in said transformer from said second rectified supply voltage a second plurality of current pulses (ip2), such that a given current pulse of said first plurality of current pulses and a given current pulse of said second plurality of current pulses occur, during a given period of said switching signal, said first and second pluralities of current pulses being transformer-coupled via said transformer to a load circuit (LOAD) to develop in said load circuit an output supply voltage (V2) and an output supply current (IL).

19. A power supply according to claim 18 further comprising, means (COMP 1, COMP 2) for disabling the generation of said second plurality of current pulses (ip2) throughout a portion (T1) of a period of said mains supply voltage (VM), in a vicinity of a peak voltage of said mains supply voltage.

20. A power supply according to claim 18 wherein said second plurality of current pulses (ip2) are generated during a portion (T2) of a period of said main supply voltage (VM) when amplitudes of said first plurality of current pulses substantially decrease.

21. A power supply according to claim 18 wherein said second plurality of current pulses (ip2) are produced in a current inter-leaving manner (Fig. 1) with respect to said first plurality of current pulses (ip1).

22. A power supply according to claim 18 wherein said second plurality of current pulses (ip2) are produced in a current super-position manner (Fig. 4) with respect to said first plurality of current pulses (ip1).

Patentansprüche

1. Schaltnetzteil, enthaltend:

- eine Quelle (107) einer AC-Netzversorgungs-Spannung (VM);
- eine Induktivität (W1);
- ein erstes Schaltmittel (Q1), das mit der Netz-Versorgungs-Quelle gekoppelt ist und auf ein Schaltsignal (V16) anspricht, zum Erzeugen einer ersten Mehrzahl von Stromimpulsen (ip1, is1) in der Induktivität bei einer Frequenz (20-50 kHz), die wesentlich höher als die (50 Hz) der Netz-Versorgungs-Spannung ist, so daß während eines ersten Zeitabschnitts (T2, Fig. 2g) einer gegebenen Periode, entfernt von einer Spitze oder einem Scheitelpunkt der Netz-Versorgungs-Spannung, wenn sich die Netz-Versorgungs-Spannung verringert, die Abnahme eine gleichzeitige Abnahme der Amplituden der ersten Mehrzahl von Stromimpulsen und eines Pegels eines Netz-Versorgungsstroms (IM) bewirkt, der von der ersten Netzquelle zugeführt wird, dadurch gekennzeichnet,
- daß ein zweites Schaltmittel (Q2) mit dem ersten Schaltmittel synchronisiert und mit der Induktivität gekoppelt ist zum Erzeugen einer zweiten Mehrzahl von Stromimpulsen (ip2, is2) in der Induktivität bei einer Frequenz, die wesentlich höher ist als die der Netz-Versorgungs-Spannung, wobei die zweite Mehrzahl der Stromimpulse zumindest während des ersten Abschnitts der gegebenen Periode der Netz-Versorgungs-Spannung erzeugt wird;
- daß eine Lastschaltung (LOAD) vorgesehen ist; und
- daß ein Mittel (W2) vorgesehen ist, das auf die erste und zweite Mehrzahl der Stromimpulse anspricht, zum Bilden einer Ausgangs-Versorgungsspannung (V2) und eines Ausgangs-Versorgungsstroms (IL) in der Lastschaltung.

2. Schaltnetzteil nach Anspruch 1, enthaltend einen Gleichrichter (D2) zum Gleichrichten der ersten (IL1) und zweiten (IL2) Mehrzahl von Stromimpulsen, um die Ausgangs-Versorgungsspannung (V2) und den Ausgangsstrom (IL) so zu bilden, daß die zweite Mehrzahl von Stromimpulsen die Abnahme der Amplituden der ersten Mehrzahl von Stromimpulsen derart kompensiert, daß eine Wellen-Komponente (Ripple) bei einer Frequenz (100 Hz), die zu der (50 Hz) der Netz-Versorgungs-Spannung Bezug hat, reduziert wird.

3. Schaltnetzteil nach Anspruch 1, wobei die zweite Mehrzahl von Stromimpulsen (ip2) in der Induktanz (W1) erzeugt wird und wobei die Ausgangs-



Versorgungsspannung (V2) in Sperrwandler-Weise (Flyback-manner) von der ersten (ip1) und zweiten (ip2) Mehrzahl von Stromimpulsen erzeugt wird.

4. Schaltnetzteil nach Anspruch 1, bei dem die Stromimpulse der ersten (ip1) und zweiten (ip2) Mehrzahl von Stromimpulsen in sich gegenseitig ausschließenden Intervallen innerhalb eines gegebenen Zeitabschnitts des Schaltsignals (V16) auftreten.

5. Schaltnetzteil nach Anspruch 1, wobei die zweite Mehrzahl von Stromimpulsen (ip2) in der Induktanz (W1) erzeugt wird und wobei ein gegebener Stromimpuls von einer der ersten Mehrzahl von Stromimpulsen (ip1) benachbart zu einem gegebenen Stromimpuls der zweiten Mehrzahl von Stromimpulsen auftritt, so daß keine Zeitlücke zwischen den benachbarten Stromimpulsen entsteht.

6. Schaltnetzteil nach Anspruch 1, enthaltend ein Mittel (COMP 1, COMP 2) zum Abschalten der Erzeugung der zweiten Mehrzahl von Stromimpulsen (ip2) während eines zweiten Teils (T1, Fig. 2g) der Periode der Netz-Versorgungs-Spannung (VM), in der Nähe des Scheitelpunktes oder der Spitze der Spannung der Netz-Versorgungs-Spannung.

7. Schaltnetzteil nach Anspruch 1, enthaltend einen Pulsbreiten-Modulator (101) zum Steuern der Impulsbreite der Stromimpulse mindestens einer (Mehrzahl) (ip1, ip2) der ersten (ip1) und zweiten (ip2) Mehrzahl von Stromimpulsen in Übereinstimmung mit dem einen der Ausgangsspannung (V2) oder Strom (IL), um die Regulierung bereitzustellen.

8. Schaltnetzteil nach Anspruch 7, wobei der Pulsbreiten-Modulator (101) jede der ersten (ip1) und zweiten (ip2) Mehrzahl von Stromimpulsen steuert, um eine Regulierung/Regelung zu bewirken.

9. Schaltnetzteil nach Anspruch 1, wobei die zweite Mehrzahl der Stromimpulse (ip2) in der Induktanz erzeugt wird und wobei die zweite Mehrzahl der Stromimpulse umlaufende (re-circulated) Stromimpulse bezüglich der Induktanz (W1) beinhaltet.

10. Schaltnetzteil nach Anspruch 1, wobei die zweite Mehrzahl der Stromimpulse (ip2) in der Induktanz (W1) erzeugt wird und wobei die Induktanz in einer ersten Wicklung (W1) eines Transformators/Übertragers (T) beinhaltet ist.

11. Schaltnetzteil nach Anspruch 10, enthaltend ei-

nen zweiten Gleichrichter (D4) und einen Kondensator (C4) zum Gleichrichten von Stromimpulsen in einer zweiten Wicklung (W4) des Transformators/Übertragers (T), die von der ersten Mehrzahl von Stromimpulsen (ip1) erzeugt werden, zum Bilden einer zweiten Versorgungsspannung (V4) am Kondensator, wobei die zweite Versorgungs-Spannung mit dem zweiten Schaltmittel (Q2) zum Erzeugen der zweiten Mehrzahl von Stromimpulsen (ip2) aus der zweiten Versorgungs-Spannung gekoppelt ist.

12. Schaltnetzteil nach Anspruch 10, wobei das zweite Schaltmittel (Q2) eine zweite Versorgungs-Spannung (V4) mit der ersten Wicklung (W1) des Transformators (T) koppelt, um einen gegebenen Impuls der zweiten Mehrzahl von Stromimpulsen (ip2) zu erzeugen, und wobei die Quelle (107) der Netz-Versorgungs-Spannung (VM) gleichzeitig von der ersten Wicklung während eines Teils der gegebenen Periode oder des gegebenen Zeitabschnitts des Schaltsignals entkoppelt wird.

13. Schaltnetzteil nach Anspruch 10, wobei die zweite Mehrzahl von Stromimpulsen (ip2) in einer hinsichtlich der ersten Mehrzahl von Stromimpulsen (ip1) stromverschachtelten Weise (Figur 1) erzeugt wird.

14. Schaltnetzteil nach Anspruch 10, wobei die zweite Mehrzahl von Stromimpulsen (ip2) in einer stromüberlagerten Weise (Figur 4) hinsichtlich der ersten Mehrzahl von Stromimpulsen (ip1) erzeugt wird.

15. Schaltnetzteil nach Anspruch 10, umfassend ein Mittel (D4", Fig. 7) zum Erzeugen einer zweiten Versorgungs-Spannung (an C4") aus der Netz-Versorgungs-Spannung (VM") über einen Strompfad (D4"), der den Transformator (W1", W2") ausschließt oder umgeht, wobei die zweite Versorgungs-Spannung durch ein zweites Schaltmittel (Q2") an den Transformator (W1", W2") zum Erzeugen einer zweiten Mehrzahl von Stromimpulsen (ip2") gekoppelt ist.

16. Schaltnetzteil nach Anspruch 10, umfassend einen Gleichrichter (102), der an die Netzquelle (107) zum Gleichrichten der Netz-Versorgungs-Spannung (VM) gekoppelt ist, zum Erzeugen einer gleichgerichteten Versorgungs-Spannung (V1), die an den Transformator (T) gekoppelt ist, wobei die gleichgerichtete Versorgungs-Spannung von der Netzspannung ohne signifikantes Tiefpaß-Filtern hinsichtlich einer Frequenz (50 Hz) der Netzspannung gebildet wird.

17. Schaltnetzteil nach Anspruch 10, bei dem wäh-



rend der gegebenen Periode der Netzspannung (VM) ein Verhältnis zwischen einer Amplitude eines gegebenen Stromimpulses der ersten Mehrzahl der Stromimpulse (ip1) und einem Pegel der Netzspannung (VM), der während des gegebenen Stromimpulses der ersten Mehrzahl der Stromimpulse vorherrscht oder überwiegt, im wesentlichen konstant für jeden Stromimpuls ist.

18. Schaltnetzteil enthaltend:

- eine Quelle (107) einer AC-Netz-Versorgungs-Spannung (VM) ;
- einen Sperrwandler-Transformator (T);
- einen Gleichrichter (102), der an die Netzquelle gekoppelt ist, zum Gleichrichten der Netz-Versorgungs-Spannung, um in einer ersten Wicklung (W1) des Transformators eine erste gleichgerichtete Versorgungs-Spannung (V1) zu bilden, so daß die gleichgerichtete Versorgungs-Spannung ohne Tiefpaß-Filtern hinsichtlich einer Frequenz (50 Hz) und niedrigen Harmonischen der Netz-Versorgungs-Spannung gebildet wird;
- ein erstes Schaltmittel (Q1), ansprechend auf ein Schaltsignal (V16) bei einer Frequenz (20-50 kHz), die wesentlich höher als die Frequenz (50 Hz) der Netz-Versorgungs-Spannung ist, zum Erzeugen einer ersten Mehrzahl von Stromimpulsen (ip1) in der ersten Wicklung; und
- ein Mittel (W4,D4), das eine zweite Versorgungs-Spannung (V4) erzeugt; dadurch gekennzeichnet, daß ein zweites Schaltmittel (Q2) mit dem Transformator gekoppelt ist und mit dem ersten Schaltmittel zum Koppeln der zweiten gleichgerichteten Versorgungs-Spannung an den Transformator und zum Abkoppeln oder Entkoppeln der ersten gleichgerichteten Versorgungs-Spannung von dem Transformator synchronisiert ist, zum Erzeugen einer zweiten Mehrzahl von Stromimpulsen (ip2) in dem Transformator aus der zweiten gleichgerichteten Versorgungs-Spannung, so daß ein gegebener Stromimpuls der ersten Mehrzahl von Stromimpulsen und ein gegebener Stromimpuls der zweiten Mehrzahl von Stromimpulsen während einer bestimmten Periode oder Zeitabschnitts des Schaltsignals auftreten, wobei die erste und zweite Mehrzahl der Stromimpulse durch den Transformator zu einer Lastschaltung (LOAD) transformatorisch gekoppelt wird, um an der Lastschaltung eine Ausgangsspannung (V2) und einen Ausgangsstrom (IL) zu erzeugen.

19. Schaltnetzteil nach Anspruch 18, enthaltend ein

Mittel (COMP 1, COMP 2) zum Abschalten der Erzeugung der zweiten Mehrzahl von Stromimpulsen (ip2) während eines Teils (T1) einer Periode oder eines Zeitabschnitts der Netz-Versorgungs-Spannung (VM) in einer Nähe oder Umgebung der Scheitelpunkt-Spannung der Netz-Versorgungs-Spannung.

20. Schaltnetzteil nach Anspruch 18, wobei die zweite Mehrzahl von Stromimpulsen (ip2) während eines Teils (T2) eines Zeitabschnitts oder Periode der Netz-Versorgungs-Spannung (VM) erzeugt wird, wo oder wenn die Amplituden der ersten Mehrzahl von Stromimpulsen sich wesentlich verringern.

21. Schaltnetzteil nach Anspruch 18, wobei die zweite Mehrzahl von Stromimpulsen (ip2) in einer mit der ersten Mehrzahl von Stromimpulsen (ip1) strom-verschachtelten Weise (Figur 1) erzeugt wird.

22. Schaltnetzteil nach Anspruch 18, wobei die zweite Mehrzahl von Stromimpulsen (ip2) in einer Strom-Überlagerungsweise (Fig. 4) hinsichtlich der ersten Mehrzahl von Stromimpulsen erzeugt wird.

Revendications

1. Une alimentation en mode commuté intégrant :
une source (107) de tension d'alimentation CA (VM) ;
une inductance (W1) ;
un premier moyen de commutation (Q1) couplé à ladite source d'alimentation et sensible à un signal de commutation (V16) destiné à générer un premier ensemble d'impulsions d'intensité (ip1, is1) dans ladite inductance à une fréquence (20-50 KHz) largement supérieure à celle de ladite tension d'alimentation (50 Hz) de sorte que pendant une première partie (T2, Fig. 2g) d'une période définie, éloignée d'une crête de ladite tension d'alimentation, lorsque ladite tension d'alimentation diminue, la baisse occasionne une diminution simultanée des amplitudes dudit premier ensemble d'impulsions d'intensité et du niveau d'intensité d'alimentation (IM) délivré par ladite source d'alimentation ;
caractérisé par
un second moyen de commutation (Q2) synchronisé audit premier moyen de commutation et couplé à ladite inductance afin de générer un second ensemble d'impulsions d'intensité (ip2, is2) dans ladite inductance à une fréquence nettement supérieure à celle de ladite tension d'alimentation, ledit second ensemble d'impulsions d'intensité



étant généré au moins pendant ladite première partie de ladite période définie de ladite tension d'alimentation ;
un circuit de charge (LOAD) ; et
un moyen (W2) sensible auxdits premier et second ensembles d'impulsions d'intensité destiné à générer une tension d'alimentation de sortie (V2) et une intensité d'alimentation de sortie (IL) dans ledit circuit de charge.

2. Une alimentation conforme à la Revendication 1 intégrant également un redresseur (D2) destiné à redresser lesdits premier (IL1) et second (IL2) ensembles d'impulsions d'intensité afin de générer ladite tension d'alimentation de sortie (V2) et ladite intensité d'alimentation de sortie (IL), de sorte que ledit second ensemble d'impulsions d'intensité compense la diminution desdites amplitudes dudit premier ensemble d'impulsions d'intensité de manière à réduire une composante d'ondulation à une fréquence (100 Hz) apparentée à celle de ladite tension d'alimentation (50 Hz).
3. Une alimentation conforme à la Revendication 1 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré dans ladite inductance (W1) et en ce que ladite tension d'alimentation de sortie (V2) est générée par retour desdits premier (ip1) et second (ip2) ensembles d'impulsions d'intensité.
4. Une alimentation conforme à la Revendication 1 caractérisée en ce que lesdites impulsions d'intensité desdits premier (ip1) et second (ip2) ensembles d'impulsions d'intensité surviennent à des intervalles mutuellement exclusifs pendant une période donnée dudit signal de commutation (V16).
5. Une alimentation conforme à la Revendication 1 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré dans ladite inductance (W1) et en ce qu'une impulsion d'intensité donnée d'un desdits premiers ensembles d'impulsions d'intensité (ip1) est générée à proximité d'une impulsion d'intensité donnée dudit second ensemble d'impulsions d'intensité de sorte qu'il n'existe aucun décalage temporel entre les impulsions adjacentes.
6. Une alimentation conforme à la Revendication 1 intégrant également un moyen (COMP 1, COMP 2) destiné à désactiver le processus de génération dudit second ensemble d'impulsions d'intensité (ip2) lors d'une seconde partie (T1, Fig. 2g) de ladite période de ladite tension d'alimentation (VM), aux alentours de ladite tension crête de ladite tension d'alimentation.

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7. Une alimentation conforme à la Revendication 1 intégrant également un modulateur d'impulsions en largeur (101) en vue de la modulation d'impulsions en largeur des impulsions d'intensité d'au moins l'un (ip1, ip2) dudit premier (ip1) et dudit second (ip2) ensemble d'impulsions d'intensité conformément à une valeur prise parmi ladite intensité (IL) et ladite tension d'alimentation de sortie (V2) de manière à assurer la régulation.
8. Une alimentation conforme à la Revendication 7 caractérisée en ce que ledit modulateur d'impulsions en largeur (101) module chacun desdits premier (ip1) et second (ip2) ensembles d'impulsions d'intensité de manière à assurer la régulation.
9. Une alimentation conforme à la Revendication 1 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré dans ladite inductance et en ce que ledit second ensemble d'impulsions d'intensité est composé d'impulsions d'intensité retransmises par rapport à ladite inductance (W1).
10. Une alimentation conforme à la Revendication 1 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré dans ladite inductance (W1) et en ce que ladite inductance est incluse dans le premier enroulement (W1) d'un transformateur (T).
11. Une alimentation conforme à la Revendication 10 comprenant également, un second redresseur (D4) et un condensateur (C4) destinés à redresser les impulsions d'intensité dans un second enroulement (W4) dudit transformateur (T), qui sont générées à partir dudit premier ensemble d'impulsions d'intensité (ip1) afin de délivrer une seconde tension d'alimentation (V4) dans ledit condensateur, ladite seconde tension d'alimentation étant couplée audit second moyen de commutation (Q2) afin de générer le second ensemble d'impulsions d'intensité (ip2) à partir de ladite seconde tension d'alimentation.
12. Une alimentation conforme à la Revendication 10 caractérisée en ce que ledit second moyen de commutation (Q2) couple une seconde tension d'alimentation (V4) audit premier enroulement (W1) dudit transformateur afin de générer une impulsion donnée dudit second ensemble d'impulsions d'intensité (ip2), et en ce que ladite source (107) de tension d'alimentation (VM) est simultanément découplée dudit premier enroulement, pendant une partie d'une période donnée dudit signal de commutation.



13. Une alimentation conforme à la Revendication 10 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré par entrelacement des intensités (Fig. 1) par rapport audit premier ensemble d'impulsions d'intensité (ip1). 5
14. Une alimentation conforme à la Revendication 10 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est générée par superposition des intensités (Fig. 4) par rapport audit premier ensemble d'impulsions d'intensité (ip1). 10
15. Une alimentation conforme à la Revendication 10 comprenant également, un moyen (D4", Fig. 7) destiné à générer une seconde tension d'alimentation (dans C4") à partir de ladite tension d'alimentation (VM") via un chemin d'intensité (D4") qui exclut ledit transformateur (W1", W2"), caractérisé en ce que ladite seconde tension d'alimentation est couplée via ledit second moyen de commutation (Q2") audit transformateur (W1", W2") afin de générer ledit second ensemble d'impulsions d'intensité (ip2"). 15 20 25
16. Une alimentation conforme à la Revendication 10 comprenant également, un redresseur (102) couplé à ladite source d'alimentation (107) afin de redresser ladite tension d'alimentation (VM) pour générer une tension d'alimentation redressée (V1) qui est couplée audit transformateur (T), caractérisée en ce que ladite tension d'alimentation redressée est produite à partir de ladite tension d'alimentation sans filtrage passe-bas par rapport à une fréquence (50 Hz) de ladite alimentation. 30 35
17. Une alimentation conforme à la Revendication 10 caractérisée en ce que, pendant ladite période donnée de ladite tension d'alimentation (VM), le rapport entre l'amplitude d'une impulsion d'intensité dudit premier ensemble d'impulsions d'intensité (ip1) et le niveau de ladite tension d'alimentation (VM) qui prévaut pendant ladite impulsion d'intensité donnée dudit premier ensemble d'impulsions d'intensité, est largement constant à chaque impulsion d'intensité. 40 45
18. Une alimentation en mode commuté comprenant :
une source (107) de tension d'alimentation CA (VM) ;
un transformateur de retour (T) ;
un redresseur (102) couplé à ladite source d'alimentation afin de redresser ladite tension d'alimentation pour générer, dans un premier enroulement (W1) dudit transformateur, une première 50 55
- tension d'alimentation redressée (V1) de sorte que ladite tension d'alimentation redressée soit générée sans filtrage passe-bas par rapport à une fréquence (50 Hz) et d'harmoniques de poids faible de ladite tension d'alimentation ;
un premier moyen de commutation (Q1) sensible à un signal de commutation (V16) à une fréquence (20-50 KHz) largement supérieure à une fréquence (50 Hz) de ladite tension d'alimentation afin de générer un premier ensemble d'impulsions d'intensité (ip1) dans ledit premier enroulement ; et
un moyen (W4, D4) délivrant une seconde tension d'alimentation (V4) ;
caractérisé par
un second moyen d'alimentation (Q2) couplé audit transformateur et synchronisé avec ledit premier moyen de commutation afin de connecter ladite seconde tension d'alimentation redressée audit transformateur et de déconnecter ladite première tension d'alimentation redressée dudit transformateur pour générer, dans ledit transformateur, à partir de ladite seconde tension d'alimentation redressée, un second ensemble d'impulsions d'intensité (ip2), de sorte qu'une impulsion d'intensité donnée dudit premier ensemble d'impulsions d'intensité et une impulsion d'intensité donnée dudit second ensemble d'impulsions d'intensité surviennent, pendant une période définie dudit signal de commutation, lesdits premier et second ensembles d'impulsions d'intensité étant couplés par transformateur, par l'intermédiaire dudit transformateur à circuit de charge (LOAD) pour générer dans ledit circuit de charge, une tension d'alimentation de sortie (V2) et une intensité d'alimentation de sortie (iL)
19. Une alimentation conforme à la Revendication 18 comprenant également, un moyen (COMP 1, COMP 2) destiné à désactiver la génération dudit second ensemble d'impulsions d'intensité (ip2) lors d'une partie (T1) d'une période de ladite tension d'alimentation (VM), aux alentours d'une tension crête de ladite tension d'alimentation.
20. Une alimentation conforme à la Revendication 18 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré pendant une partie (T2) d'une période de ladite tension d'alimentation (VM) lorsque les amplitudes dudit premier ensemble d'impulsions d'intensité diminuent fortement.
21. Une alimentation conforme à la Revendication 18 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré par entrelacement des intensités (Fig. 1) par rapport audit premier ensemble d'impulsions d'intensité



(ip1).

- 22.** Une alimentation conforme à la Revendication 18 caractérisée en ce que ledit second ensemble d'impulsions d'intensité (ip2) est généré par superposition des intensités (Fig. 4) par rapport audit premier ensemble d'impulsions d'intensité (ip1).

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