Claims

What is claimed is:

1. An apparatus with an ultra low power architecture, comprising:
a first power supply rail, wherein a plurality of subsystems are to be powered by the first power supply rail; and
a second power supply rail, wherein a plurality of autonomous subsystems are to be powered by the power supply rail, wherein the second power supply rail is to be always on, always available, and low power.

2. The apparatus of claim 1, wherein the apparatus is a system on chip.

3. The apparatus of claim 1, wherein the autonomous subsystems directly access a memory of the apparatus.

4. The apparatus of claim 1, wherein a memory access by the plurality of autonomous subsystems does not exit an S0ix system state.

5. The apparatus of claim 1, wherein an autonomous subsystem is active during a deep S0ix sleep state.

6. A power management integrated circuit (PMIC) operable to provide a plurality of power states, wherein the power management integrated circuit is to transition an autonomous subsystem from a sleep state to an active state, and wherein the autonomous subsystem is active and powered by a low power always on power supply while a second subsystem is to remain in the sleep state.

7. The power management integrated circuit of claim 6, wherein the low power always on power supply is to power a non-coherent data path to memory.

8. The power management integrated circuit of claim 6, wherein the autonomous subsystem uses a non-coherent data path to access memory during a low power use case.

9. The power management integrated circuit of claim 6, wherein the power management integrated circuit is to remove the second subsystem from the sleep state when the autonomous subsystem is to provide coherent data on a coherent data path to memory.

10. The power management integrated circuit of claim 6, wherein the power management integrated circuit does not toggle a main power rail in response to a non-coherent memory access by the autonomous subsystem.

11. A method for providing an ultra low power architecture, comprising:
enabling a first path to memory on a mobile system on chip, wherein the first path to memory is powered by a main power rail; and
enabling a second path to memory on the mobile system on chip, wherein the path to memory is powered by a second low power, always on power rail.

12. The method of claim 11, wherein the first path to memory is a high bandwidth, high latency data path.

13. The method of claim 11, wherein second path to memory is a low bandwidth, low latency data path.

14. The method of claim 11, wherein an autonomous subsystem accesses the memory using the second path to memory, without a second subsystem exiting an S0ix system state.

15. An apparatus with an ultra low power architecture, comprising:
a first means to supply power to a memory device of the apparatus; and
a second means to supply power to the memory device of the apparatus, wherein the second means is to be always on and low power.

16. The apparatus of claim 15, wherein a plurality of autonomous subsystems are to be powered by the second means to supply power.

17. The apparatus of claims 15, wherein the second means to supply power is to power an always on, always available, low bandwidth and low latency data path to memory.

18. The apparatus of claims 15, wherein a memory access by the plurality of autonomous subsystems does not exit an S0ix system state

19. The apparatus of claims 15, wherein an autonomous subsystem is active during a deep S0ix sleep state.

20. The apparatus of claims 15, comprising:
a coherent data path to a memory subsystem from the plurality of autonomous subsystems; and
a non-coherent data path to a memory subsystem from the plurality of autonomous subsystems.

21. A system with an ultra low power architecture, comprising:
a display;
a radio;
a memory that is to store instructions and that is communicatively coupled to the display;
a processor communicatively coupled to the radio and the memory;

a first power supply rail, wherein a plurality of subsystems are to be powered by the first power supply rail; and

a second power supply rail, wherein a plurality of autonomous subsystems are to be powered by the second power supply rail, wherein the second power supply rail is to be always on and always available.

22. The system of claim 21, wherein the autonomous subsystems directly access the memory via a low latency, low bandwidth path to memory.

23. The system of claim 21, wherein a memory access by the plurality of autonomous subsystems does not exit an S0ix system state.

24. The system of claim 21, wherein an autonomous subsystem powered by the second power supply rail is active during a deep S0ix sleep state in which the first power supply rail is powered down.

25. The system of claim 21, comprising:

a coherent data path to a memory subsystem from the plurality of autonomous subsystems that is powered by the first power supply rail; and

a non-coherent data path to a memory subsystem from the plurality of autonomous subsystems that is powered by the second power supply rail.

Claims

What is claimed is:

1. An apparatus with an ultra low power architecture, comprising:
   a first power supply rail, wherein a plurality of subsystems are to be powered by the first power supply rail; and
   a second power supply rail, wherein a plurality of autonomous subsystems are to be powered by the power supply rail, wherein the second power supply rail is to be always on, always available, and low power.

2. The apparatus of claim 1, wherein the apparatus is a system on chip.

3. The apparatus of claim 1, wherein the autonomous subsystems directly access a memory of the apparatus.

4. The apparatus of claim 1, wherein a memory access by the plurality of autonomous subsystems does not exit an S0ix system state.

5. The apparatus of claim 1, wherein an autonomous subsystem is active during a deep S0ix sleep state.

6. The apparatus of claim 1, comprising:
   a coherent data path to a memory subsystem from the plurality of autonomous subsystems; and
   a non-coherent data path to a memory subsystem from the plurality of autonomous subsystems.

7. The apparatus of claim 1, wherein the plurality of autonomous subsystems are placed on a same fabric of the apparatus.

8. The apparatus of claim 1, wherein the plurality of autonomous subsystems are moved to a separate companion die of the apparatus.

9. The apparatus of claim 1, wherein the plurality of autonomous subsystems include sensor hub, modem, audio, any subsystem that can access memory independently, or any combination thereof.

10. The apparatus of claim 1, wherein the apparatus is a mobile device.

11. The apparatus of claim 1, wherein a high bandwidth path to memory is enabled by first power supply rail.

12. The apparatus of claim 1, wherein a low bandwidth path to memory is enabled using the always on, always available second power supply rail.

13. A power management integrated circuit (PMIC) operable to provide a plurality of power states, wherein the power management integrated circuit is to transition an autonomous subsystem from a sleep state to an active state, and wherein the autonomous subsystem is active and powered by a low power always on power supply while a second subsystem is to remain in the sleep state.

14. The power management integrated circuit of claim 13, wherein the low power always on power supply is to power a non-coherent data path to memory.

15. The power management integrated circuit of claim 13, wherein the autonomous subsystem uses a non-coherent data path to access memory during a low power use case.

16. The power management integrated circuit of claim 13, wherein the power management integrated circuit is to remove the second subsystem from the sleep state when the autonomous subsystem is to provide coherent data on a coherent data path to memory.

17. The power management integrated circuit of claim 13, wherein the power management integrated circuit does not toggle a main power rail in response to a non-coherent memory access by the autonomous subsystem.

18. The power management integrated circuit of claim 13, wherein the power management integrated circuit manages a plurality of autonomous subsystems.

19. A method for providing an ultra low power architecture, comprising:

enabling a first path to memory on a mobile system on chip, wherein the first path to memory is powered by a main power rail; and

enabling a second path to memory on the mobile system on chip, wherein the path to memory is powered by a second low power, always on power rail.

20. The method of claim 19, wherein the first path to memory is a high bandwidth, high latency data path.

21. The method of claim 19, wherein second path to memory is a low bandwidth, low latency data path.

22. The method of claim 19, wherein an autonomous subsystem accesses the memory using the second path to memory, without a second subsystem exiting an S0ix system state.

23. The method of claim 19, wherein the first path to memory is a coherent data path to the memory subsystem from a plurality of autonomous subsystems.

24. The method of claim 19, wherein the second path to memory is a non-coherent data path to a memory subsystem from a plurality of autonomous subsystems.

25. The method of claim 19, wherein the second path to memory is accessed by a plurality of autonomous subsystems that are placed on a same fabric of the mobile system on chip.