

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor memory device, comprising:
a semiconductor layer including a first region and a second region;
a plurality of first vertical structures on the first region and extending in a first direction perpendicular to a top surface of the semiconductor layer; and
a plurality of second vertical structures on the second region and extending in the first direction,

wherein each of the first vertical structures comprises:

a vertical semiconductor pattern extending in the first direction and contacting the semiconductor layer; and

a first data storage pattern surrounding a periphery of the vertical semiconductor pattern, and

wherein each of the second vertical structures comprises:

an insulation structure extending in the first direction and contacting the semiconductor layer; and

a second data storage pattern surrounding a periphery of the insulation structure, the second data storage pattern directly contacting a sidewall of the insulation structure.

2. The device of claim 1, wherein
each first vertical structure comprises a first width, and
each second vertical structure comprises a second width that is greater than the first width.

3. The device of claim 2, wherein:

each first data storage pattern comprises a first thickness, and

each second data storage pattern comprises a second thickness that is substantially equal to or less than the first thickness.

4. The device of any one of claims 1 to 3, wherein each of the first and second data storage patterns comprises a tunnel insulation layer, a charge storage layer, and a blocking insulation layer that are sequentially stacked.

5. The device of any one of claims 1 to 4, wherein a bottom surface of the insulation structure of one of the second vertical structures is lower than the top surface of the semiconductor layer.

6. The device of any one of claims 1 to 5, wherein a bottom surface of the insulation structure of one of the second vertical structures is lower than a bottom surface of the second data storage pattern.

7. The device of any one of claims 1 to 6, wherein the semiconductor layer comprises:

a first epitaxial layer connected to the vertical semiconductor pattern of one of the first vertical structures on the first region; and

a second epitaxial layer contacting the insulation structure of one of the second vertical structures on the second region.

8. The device of claim 7, wherein
the first epitaxial layer comprises a first height, and
the second epitaxial layer comprises a second height that is less than the first height.

9. The device of any one of claims 1 to 8, further comprising an electrode structure including electrodes stacked in the first direction on the semiconductor layer, wherein the electrode structure extends from the first region toward the second region in a second direction, wherein the electrode structure has a stepwise structure on the second region, and wherein the second direction is parallel to the top surface of the semiconductor layer.

10. The device of claim 9, wherein each of the electrodes comprises a pad constituting the stepwise structure on the second region, and wherein one or more of the second vertical structures extend into the pad of each of the electrodes.

11. The device of claim 10, further comprising contact plugs coupled to the pads of the electrodes, wherein the second vertical structures surround each of the contact plugs in a plan view.

12. The device of claim 11, wherein the contact plugs comprise a lower contact plug that is coupled to a lowermost one of the electrodes, and wherein the lower contact plug comprises a width greater than those of ones of the other contact plugs.

13. A three-dimensional semiconductor memory device, comprising:
a substrate including a first region and a second region;
an electrode structure including electrodes vertically stacked on the substrate;
a plurality of first vertical structures extending into the electrode structure on the first region; and
a plurality of second vertical structures extending into the electrode structure on the second region,

wherein each of the first vertical structures comprises:

a vertical semiconductor pattern extending into the electrode structure;

and

a first data storage pattern between the vertical semiconductor pattern and the electrode structure, and

wherein each of the second vertical structures comprises:

an insulation structure extending into the electrode structure; and

a second data storage pattern between the insulation structure and the electrode structure, the second data storage pattern directly contacting a sidewall of the insulation structure,

a bottom surface of the insulation structure being lower than a bottom surface of the vertical semiconductor pattern and a bottom surface of the second data storage pattern.

14. The device of claim 13, wherein the second data storage pattern of one of the second vertical structures surrounds the insulation structure of the one of the second vertical structures.

15. The device of claim 13 or claim 14, wherein each first vertical structure comprises a first width, and each second vertical structure comprises a second width greater than the first width.

16. The device of any one of claims 13 to 15, wherein:

each of the first vertical structures comprises a first epitaxial layer between the substrate and the vertical semiconductor pattern,

each of the second vertical structures comprises a second epitaxial layer between the substrate and the insulation structure, and

the bottom surface of each insulation structure contacts the second epitaxial layer.

17. The device of any one of claims 13 to 16, wherein the second vertical structures partially extend into the electrode structure.

18. The device of any one of claims 13 to 17, wherein the electrode structure comprises a stepwise structure on the second region, wherein each of the electrodes comprises a pad that constitutes the stepwise structure on the second region, and wherein the second vertical structures extend into the pad of each of the electrodes.

19. The device of claim 18, further comprising cell contact plugs coupled to the pads of the electrodes on the second region, wherein each of the cell contact plugs is between adjacent ones of the second vertical structures.

20. The device of claim 19, wherein each of the cell contact plugs is surrounded by the second vertical structures, in a plan view.