Description

The present invention relates to a battery powered key entry device including a microprocessor and a power conservation system.

Currently known self contained battery powered key entry or keyboard devices may be classified into two general groups.

The first group comprises calculators, extending from the simplest four function type through to the considerably more powerful programmable calculators as exemplified by the 600 and 700 series of calculators produced by Casio Corporation. All of these devices are not normally used continuously for any great length of time. The usual operational method is to switch the device on, perform one or more calculations, and then switch off. With such operations, and depending on the form of display employed, the batteries in calculators last from several months to years. In order to conserve the batteries in the event that a calculator is left on after operation, many such devices employ an arrangement in which, some minutes after a key operation, the microprocessor is switched to a standby-mode, and the display is switched off. Thereafter, the microprocessor and display are powered up by depression of a particular key, normally the CLEAR key.

The second group comprises remote control devices, for example television remote control units. In operation, these consume much more power than the average calculator as they employ some form of transmission device, such as an infra-red generator. Such control devices are normally used relatively infrequently and for short periods. Typically, a television remote control unit may generate a sequence of up to about ten control pulses during each of up to ten to twenty times a day. Between operations, these units are switched off completely. Consequently, battery drain offers no significant problem. However, "8029 Electronic Engineering, Vol. 55 (1983) Apr., No. 676, pages 41—43 and 47 mentions, in passing, that it is possible to incorporate a processor standby mode in a remote control device with infrared transmission incorporating a processor which scans the keyboard, but makes no further comment on how this is accomplished.

Processing systems are known in which part of the system can be shutdown under processor control when not required to be active and revived when a key is depressed, see, for example Patents Abstracts of Japan, Volume 6, No. 171, (P-140) (1049), September 4, 1982 and EP—A—8501. However, in the former, the controller with which the keyboard communicates also drives the display and is only partially powered down and, in addition, since powering-up depends on the setting of a flip-flop by the depression of any key via connecting lines and an OR circuit, it implies a keyboard which has all its keys "live" even when the controller is partially powered down. EP—A—8501 discloses a processor which ideally signals power-down sub-circuit when it completes an operation, and includes a power-up circuit which comes into play when a data input circuit is operated, but the data input device is maintained live.

The present invention is concerned with the situation in which it is the data entry device that is powered down since, if it is required to provide a remote self-contained, battery powered keyboard entry device for, for example, a microcomputer, normally independently powered, battery life in the data input device, per se, becomes a significant problem. Such a device may be in substantially continuous use throughout each day of a working week. With such operational conditions, without some form of battery conservation system, battery life may prove insufficient to ensure reliable operation without frequent battery changes and yet must not involve significant cost and time delay overheads.

It is, therefore, an object of the present invention to provide a power conservation system specifically adapted for and in such an independent and remote keyboard entry device.

The present invention provides a battery powered remote key entry device comprising a keyboard and a microprocessor coupled to drive lines of the keyboard and to sense signals on a plurality of sense lines from the keyboard corresponding to key depressions and to generate, in response to the sense line signals coded output signals to drive an infra-red light emitting device, and including a power conservation system comprising a circuit interconnecting a battery between the drive and sense lines, first means responsive to a first level signal on any of the sense lines derived from said circuit by connection of a drive line to a sense line through a depressed key to generate a first signal, and second means responsive to the first signal to power the microprocessor up from its low power standby mode and to a microprocessor output signal indicating completion of processing of all received sense signals to return the microprocessor to its low power standby mode, the microprocessor, when powered-up, energising the drive lines at significantly timed intervals to cause data signals at a second level to be generated on the or those sense lines connected to actuated keys of the keyboard until all the drive lines have been energised. From this it will be appreciated that the only part of the keyboard that remains "live" is the circuit and this, as in the case of the disclosed embodiment of the invention, need be no more than a simple resistor.

With this arrangement, when the microprocessor has processed the received key entry signals, it is set into its low power standby mode and is not powered up until the next keystroke is detected. Accordingly, battery power is conserved as the microprocessor is for the majority of the time in its low power standby mode.

The present invention will be described further by way of example with reference to an embodiment thereof as illustrated in the accompanying drawings, in which:—

Figure 1 is a diagram of the circuit of a battery powered keyboard entry device; and

Figure 2 is a timing diagram of keyboard drive and sense signals therefor.

In Figure 1, a keyboard entry device includes a microprocessor 1 coupled to a matrix keyboard 2. Microprocessor 1 may be the 80C48 microprocessor produced by Nippon Electric Company. For simplicity, only the inputs and outputs particularly relevant to the present invention have been shown. These are, the input data port lines, comprising 8 inputs DB0 through DB7, the first ouput port lines, again 8 lines, P10 through through P17, the address latch enable output ALE, which provides an output once during each processor cycle and is, therefore useful as a clock output, two lines P25 and P27 of the second output port, a NOT RESET input, and the lower power standy input V_{DD}.

The first output port lines P10 through P17 are coupled through eight inverting amplifiers 11—12 and eight diodes 13—14 to drive the matrix keyboard 2. Eight sense lines from the keyboard 2 are fed back to the data input port DB0 through DB7 of microprocessor 1. Each matrix drive line is coupled through an associated one of eight resistors 15—16 to battery positive, and each matrix sense line is similarly coupled to the battery positive through an associated one of eight resistors 17—18.

Keyboard 2 is of the matrix contact type, in which depression of a key connects the single drive and sense lines which cross at the key position. Suitable keyboard technologies for the present system include the full travel contact membrane system or a carbon contact/rubber dome system.

Figure 2 shows the signals on the keyboard drive and sense lines in a typical operation of the Figure 1 system. As an example, let us look at the signals on the drive line from P10 and the resulting sense signals applied to DB0. With none of the eight keys coupled to the sense line depressed, this sense line is held high through resistor 17, as substantially no current flows through the resistor into the sense line. Similarly when none of the keys coupled to the P10 drive line is depressed, the input to inverting amplifiers 11 is high, its output is, therefore, low, but no current flows through diode 13 as the drive line is not connected within matrix 2. When the key coupling these lines is depressed, current flows through resistor 17, the associated keyboard contacts, and then through diode 13, as the output of amplifiers 11 is still low. Thus, the voltage level on the DB0 sense line is lowered. Subsequently, when microprocessor 1 emits a drive pulse on P10, resistor 15 conducts, lowering the input to amplifier 11. The output of this amplifier is thereby raised, cutting off current through diode 13, so, for the period of the P10 pulse, the DB0 line goes high. In a scan cycle the P10 pulse is followed in turn by the P11 through P17 pulses to drive each of the drive lines, and outputs are provided on each sense line corresponding to a depressed key. Figure 2 shows the timing of the arrangement. Lines K1 and K3 show the depression time of two keys corresponding respectively to drive P10/sense DB0 and drive P12/sense DB2. Line K2 shows the depression time of a single key, which is depressed subsequent to the above mentioned pair, and corresponds to drive P11/sense DB1. To give some idea of the actual times involved, each key depression time shown may occupy 60 m secs. of which the useful time is the central 30 m secs, the hatched areas indicating times of possible contact bounce or noise. As shown, the drive pulse at P10 through P17 take a total period of 16 m secs. The arrows indicate that for the K1 and K3 key depressions appropriate sense signals appears on the DB0 and DB2 sense lines and for the K2 key depression, on the DB1 sense line.

In Figure 2, it is assumed that prior to any of the key depressions shown, microprocessor 1 is in its low power standby condition, and therefore no signals are generated on the P10 through P17 lines. Upon depression of a key, the P10 through P17 signals are initiated after a delay D. This is shown in Figure 2 as a delay of 15 m secs, but it may be of any length sufficient to allow the first cycle of the drive signals (15 m secs. in Figure 2) to take place within the 30 m secs. sense time for the first key depression. This delay is to permit the microprocessor to power up from its low power standby condition.

Referring back to the details of Figure 1, an 8 input NOR gate 3 has each of its inputs coupled to an associated one of the DB0 through BD7 sense lines. With no key depressed, all of these lines are high, so the output on line 19 is low. Line 19 is coupled as a set input to a latch circuit comprising three NAND gates 4, 5 and 6, which is reset by a signal on line 20 which will be described later. Assuming, for the present, that the latch circuit has been reset, the signal on line 19 sets it to raise output line 21 from a '0' condition to a '1' condition.

This '1' condition on line 21 is applied directly to the S input of a D flip-flop 9, and after inversion by inverter 22, as a '0' input to a single shot 7 and the R input of a D flip-flop 8. Immediately prior to this time, flip-flop 9 had no input to its clock line, the S input was '0', the D input was '0' and the R input was '0', so the Q output was '0'. This Q output is applied, as shown to the V_{DD} input of microprocessor 1 and when in a '0' state, sets the microprocessor into its low power standby mode. Now, when the S input from line 21 changes to '1', flip-flop 9 switches to provide a '1' output at Q, thereby releasing the microprocessor from the standby mode. As mentioned above, the '0' input from inverter 22 is, at the same time, applied to a 16 m sec. single shot delay circuit 7 and to the R input of flip-flop 8. As can be seen, the D input of this flip-flop is always '1' and the S input is always '0'. Prior to arrival of the '1' signal from inverter 22, the R input is '1' so the Q output is '0' thereby placing microcomputer in a reset state. The '0' signal from inverter 22 to the R input of flip flop 8 does not alter the Q output, but sets the flip flop in

its synchronous mode to respond to a signal at the clock input. This clock input arrives 16 m. secs later from delay circuit 7 as a rising edge which sets flip-flop 8 to provide a '1' output. This takes microprocessor 1 out of its reset condition. It is noted that this output is also applied to the D input of flip-flop 9, but at this time this flip-flop is operating in the asynchronous mode (S=1) so the D input signal has no effect on the Q output.

Thus, what has happened so far is that a key has been depressed, flip-flop 9 has switched microprocessor 1 from its standby to its operating mode and, after a 16 m sec. delay, flip-flop 8 has removed reset from the microprocessor. The microprocessor now responds to keystroke inputs at inputs DB0 through DB7, converts this data to a form suitable for transmission, and after buffering in an internal transmit buffer, sends the data in serial fashion to a line 23 from output P25 of the second output port. Line 23 is connected to a driver amplifier 10 which drives a light-emitting diode 24 to provide infra-red pulses for transmission to a receiver device.

The microprocessor continuously monitors the content of the transmit buffer, and when it empties, generates a signal on output P27 of the second output port. This signal is applied to NAND gate 6 to switch the latch including this NAND gate and thereby return line 21 from the '1' state back to the '0' state. This is transmitted through inverting amplifier 22 to the R input of flip-flop 8 as a '1' signal. This resets this flip-flop to provide a '0' output to the NOT RESET input of the microprocessor, thereby setting it into its reset state. This '0' output is also applied to the D input of flip-flop 9, setting it into the synchronous mode. In this mode, the next rising edge of a clock pulse from the microprocessor ALE output switches the flip flop to provide a '0' output. This is applied to the V_{DD} input of the microprocessor which then reverts to its low power standby mode.

Thus, what has been described above is a keyboard entry device using battery power. The battery life is extended by placing the microprocessor in a standby, low power condition immediately it has processed and passed on the received keystroke data. In all but a very few exceptional cases, this condition is entered between each keystroke.

If we take an example of a system operating at 10000 keystrokes per eight hour day, with the electronics taking 0.1 sec. to process each keystroke and then power down to the standby condition, then the electronics are dynamic for 16.67 minutes, or 3.5% of the day and at standby for the remaining 96.5% of the day. With a 6 m A dynamic current and a 1.5 μ A standby current, this gives a battery drain of $(1.5/10^6 \times 96.5/100 \times 8 + 6/10^3 \times 3.5/100 \times 8) \times 10^3 = 1.6916$ m A—hr. per day. This compares dramatically with the worst case in which the electronics remain in the dynamic state continuously. In this case the battery drain would be $(6/10^3 \times 8) \times 10^3 = 48$ m A—hr per day. With the prior art arrangements in which the standby condition is entered minutes after the last keystroke, it is quite probably that this worst case situation would be the normal situation with, possibly, standby entered only once or twice a day.

Claims

1. A battery powered remote key entry device comprising a keyboard (2) and a microprocessor (1) coupled to drive lines (P10—P17) of the keyboard and to sense signals on a plurality of sense lines (DB0—DB7) from the keyboard corresponding to key depressions and to generate, in response to the sense line signals, coded output signals to drive an infra-red light emitting device (24), and a power conservation system comprising a circuit (15 to 18) interconnecting a battery between the drive and sense lines, first means (3) responsive to a first level signal on any of the sense lines derived from said circuit by connection of a drive line to a sense line through a depressed key on any of the sense lines to generate a first signal (on 19), and second means (4, 5, 6, 7, 8, 9) responsive to the first signal to power the microprocessor up from its low power standby mode and to a microprocessor output signal (on 20) indicating completion of processing of all received sense signals to return the microprocessor to its low power standby mode, the microprocessor, when powered-up, energising the drive lines at significantly timed intervals to cause data signals at a second level to be generated on the or those sense lines connected to actuated keys of the keyboard until all drive lines have been energised.

2. A key entry device according to claim 1 wherein the infra-red light emitting device is capable of producing a single datum output only at a given time, the microprocessor, when powered-up, energising the drive lines in turn and serialising the input to the emitting device.

3. A key entry device according to either preceding claim, in which said first means includes a NOR circuit (3) having an associated input coupled to each of the sense lines.

4. A key entry device according to claim 3, in which the second means includes a first latch circuit (4, 5, 6) coupled to the output of the NOR circuit and to receive said microprocessor output signal for switching respectively between its set and reset states.

5. A key entry device according to claim 4, including a second latch circuit (9) having a first input coupled to the output of the first latch circuit and its output coupled to the microprocessor low power standby mode input.

6. A key entry device according to claim 5 including a delay circuit (7) coupled between the output of said first latch circuit and an input of a third latch circuit (8) having its output coupled to a NOT-resetting input of the microprocessor.

its synchronous mode to respond to a signal at the clock input. This clock input arrives 16 m. secs later from delay circuit 7 as a rising edge which sets flip-flop 8 to provide a '1' output. This takes microprocessor 1 out of its reset condition. It is noted that this output is also applied to the D input of flip-flop 9, but at this time this flip-flop is operating in the asynchronous mode (S=1) so the D input signal has no effect on the Q output.

Thus, what has happened so far is that a key has been depressed, flip-flop 9 has switched microprocessor 1 from its standby to its operating mode and, after a 16 m sec. delay, flip-flop 8 has removed reset from the microprocessor. The microprocessor now responds to keystroke inputs at inputs DB0 through DB7, converts this data to a form suitable for transmission, and after buffering in an internal transmit buffer, sends the data in serial fashion to a line 23 from output P25 of the second output port. Line 23 is connected to a driver amplifier 10 which drives a light-emitting diode 24 to provide infra-red pulses for transmission to a receiver device.

The microprocessor continuously monitors the content of the transmit buffer, and when it empties, generates a signal on output P27 of the second output port. This signal is applied to NAND gate 6 to switch the latch including this NAND gate and thereby return line 21 from the '1' state back to the '0' state. This is transmitted through inverting amplifier 22 to the R input of flip-flop 8 as a '1' signal. This resets this flip-flop to provide a '0' output to the NOT RESET input of the microprocessor, thereby setting it into its reset state. This '0' output is also applied to the D input of flip-flop 9, setting it into the synchronous mode. In this mode, the next rising edge of a clock pulse from the microprocessor ALE output switches the flip flop to provide a '0' output. This is applied to the V_{DD} input of the microprocessor which then reverts to its low power standby mode.

Thus, what has been described above is a keyboard entry device using battery power. The battery life is extended by placing the microprocessor in a standby, low power condition immediately it has processed and passed on the received keystroke data. In all but a very few exceptional cases, this condition is entered between each keystroke.

If we take an example of a system operating at 10000 keystrokes per eight hour day, with the electronics taking 0.1 sec. to process each keystroke and then power down to the standby condition, then the electronics are dynamic for 16.67 minutes, or 3.5% of the day and at standby for the remaining 96.5% of the day. With a 6 m A dynamic current and a 1.5 μ A standby current, this gives a battery drain of $(1.5/10^6 \times 96.5/100 \times 8 + 6/10^3 \times 3.5/100 \times 8) \times 10^3 = 1.6916$ m A—hr. per day. This compares dramatically with the worst case in which the electronics remain in the dynamic state continuously. In this case the battery drain would be $(6/10^3 \times 8) \times 10^3 = 48$ m A—hr per day. With the prior art arrangements in which the standby condition is entered minutes after the last keystroke, it is quite probably that this worst case situation would be the normal situation with, possibly, standby entered only once or twice a day.

Claims

1. A battery powered remote key entry device comprising a keyboard (2) and a microprocessor (1) coupled to drive lines (P10—P17) of the keyboard and to sense signals on a plurality of sense lines (DB0—DB7) from the keyboard corresponding to key depressions and to generate, in response to the sense line signals, coded output signals to drive an infra-red light emitting device (24), and a power conservation system comprising a circuit (15 to 18) interconnecting a battery between the drive and sense lines, first means (3) responsive to a first level signal on any of the sense lines derived from said circuit by connection of a drive line to a sense line through a depressed key on any of the sense lines to generate a first signal (on 19), and second means (4, 5, 6, 7, 8, 9) responsive to the first signal to power the microprocessor up from its low power standby mode and to a microprocessor output signal (on 20) indicating completion of processing of all received sense signals to return the microprocessor to its low power standby mode, the microprocessor, when powered-up, energising the drive lines at significantly timed intervals to cause data signals at a second level to be generated on the or those sense lines connected to actuated keys of the keyboard until all drive lines have been energised.

2. A key entry device according to claim 1 wherein the infra-red light emitting device is capable of producing a single datum output only at a given time, the microprocessor, when powered-up, energising the drive lines in turn and serialising the input to the emitting device.

3. A key entry device according to either preceding claim, in which said first means includes a NOR circuit (3) having an associated input coupled to each of the sense lines.

4. A key entry device according to claim 3, in which the second means includes a first latch circuit (4, 5, 6) coupled to the output of the NOR circuit and to receive said microprocessor output signal for switching respectively between its set and reset states.

5. A key entry device according to claim 4, including a second latch circuit (9) having a first input coupled to the output of the first latch circuit and its output coupled to the microprocessor low power standby mode input.

6. A key entry device according to claim 5 including a delay circuit (7) coupled between the output of said first latch circuit and an input of a third latch circuit (8) having its output coupled to a NOT-resetting input of the microprocessor.

* C L M S *

Patentansprüche

1. Batteriebetriebenes Tastaturferneingabegerät bestehend aus einer Tastatur (2) und einem Mikroprozessor (1) welcher an Treiberleitungen (P10—P17) der Tastatur angeschlossen ist und Signale auf einer Vielzahl von Prüfleitungen (DB0—DB7) prüft, die von der Tastatur kommen und den gedrückten Tasten entsprechen, und welcher als Reaktion auf die geprüften Leitungssignale kodierte Ausgangssignale erzeugt, mit denen ein Infrarotlicht-Emitter (24) getrieben wird, und einer Energiespareinrichtung mit einer Schaltung (15—18), die eine Batterie zwischen Treiber- und Prüfleitungen schaltet, mit ersten Mitteln (2), welche auf ein erstes, von der Schaltung abgeleitetes Pegel-Signal auf einer der Prüfleitungen, das durch Verbindung von einer Treiberleitung mit einer Prüfleitung durch Tastendruck erzeugt wird, reagieren, um ein erstes Signal (auf 19) zu erzeugen, und mit zweiten Mitteln (4, 5, 6, 7, 8, 9), welche auf das erste Signal reagieren, so daß die Leistung des Mikroprozessors von seinem Bereitschaftsmodus niedriger Leistung verstärkt wird und welche auf ein Ausgangssignal (auf 20) des Mikroprozessors reagieren, welches die Beendigung der Verarbeitung aller empfangenen Prüfsignale anzeigt, so daß der Mikroprozessor zu seinem Bereitschaftsmodus niedriger Leistung zurückkehren kann, wobei der Mikroprozessor, sobald er mit höherer Leistung arbeitet, die Treiberleitungen in signifikanten Zeitintervallen anregt, um Datensignale auf einem zweiten Pegel auf der Prüfleitung bzw. auf den Prüfleitungen zu erzeugen, welche mit den gedrückten Tasten der Tastatur verbunden sind, bis alle Treiberleitungen angeregt wurden.

2. Tastatureingabegerät nach Anspruch 1, wobei der Infrarotlicht-Emitter eine einzelne Datenausgabe nur zu einer bestimmten Zeit erzeugen kann, wobei der Mikroprozessor, sobalt er mit höherer Leistung arbeitet, die Treiberleitungen dann wieder der Reihe nach anregt und das Eingangssignal zum Emitter serialisiert.

3. Tastatureingabegerät nach einem der vorhergehenden Ansprüche, wobei die erste Einrichtung eine NOR-Schaltung (3) enthält, welche einen zugehörigen Eingang mit jeder der Prüfleitungen verbunden hat.

4. Tastatureingabegerät nach Anspruch 3, wobei die zweite Einrichtung eine erste Verriegelungsschaltung (4, 5, 6) enthält, welche mit dem Ausgang der NOR-Schaltung verbunden ist und das Ausgangssignal vom Mikroprozessor empfängt, um zwischen seinem gesetzten und rückgesetzten Status umzuschalten.

5. Tastatureingabegerät nach Anspruch 4, wobei eine zweite Verriegelungsschaltung (9) vorgesehen ist, deren erster Eingang mit dem Ausgang der ersten Verriegelungsschaltung verbunden ist und deren Ausgang mit dem Eingang des Bereitschaftsmodus niedriger Leistung des Mikroprozessors verbunden ist.

6. Tastatureingabegerät nach Anspruch 5, wobei eine Verzögerungsschaltung (7) zwischen den Ausgang der ersten Verriegelungsschaltung und einen Eingang einer dritten Verriegelungsschaltung (8) gekoppelt ist, deren Ausgang mit einem NICHT-rücksetzenden Eingang des Mikroprozessors verbunden ist.

Revendications

1. Dispositif d'entrée à distance à touches alimenté par batterie comportant un clavier (2) et un microprocesseur (1) couplé de façon à attaquer les lignes (P10 à P17) du clavier et à détecter des signaux sur une pluralité de lignes de détection (DB0 à DB7) venant du clavier, correspondant à des actionnements de touches, et de façon à générer, en réponse aux signaux des lignes de détection, des signaux de sortie codés afin d'attaquer un dispositif émetteur de lumière infrarouge (24), et un système de conservation de l'alimentation comportant un circuit (15 à 18) interconnectant une batterie entre les lignes d'attaque et de détection, des premiers moyens (3) réagissant à un signal d'un premier niveau sur l'une quelconque des lignes de détection, dérivé dudit circuit par la connexion d'une ligne d'attaque à une ligne de détection par l'intermédiaire d'une touche enfoncée sur l'une quelconque des lignes de détection, de façon à générer un premier signal (sur 19), et des deuxièmes moyens (4, 5, 6, 7, 8, 9) réagissant au premier signal de façon à alimenter le microprocesseur à partir de son mode d'attente en basse puissance et à un signal de sortie de microprocesseur (sur 20) indiquant l'achèvement du traitement de tous les signaux de détection reçus de façon à faire revenir le microprocesseur dans son mode d'attente en basse puissance, le microprocesseur, lorsqu'il est alimenté, mettant sous tension les lignes d'attaque à des intervalles synchronisés de façon significative de façon à provoquer la génération de signaux de données d'un deuxième niveau sur les lignes de détection qui sont connectées aux touches actionnées du clavier jusqu'à ce que toutes les lignes d'attaque aient été mises sous tension.

2. Dispositif d'entrée à touches selon la revendication 1 dans lequel le dispositif émetteur de lumière infrarouge est capable de produire une seule sortie de donnée uniquement à un instant donné, le microprocesseur, lorsqu'il est alimenté, mettant sous tension les lignes d'attaque l'une après l'autre et mettant en série l'entrée du dispositif émetteur.

3. Dispositif d'entrée à touches selon l'une quelconque des revendications précédentes, dans lequel lesdits premiers moyens comportent un circuit NON-OU (3) ayant une entrée associée couplée à chacune des lignes de détection.

4. Dispositif d'entrée à touches selon la revendication 3, dans lequel les deuxièmes moyens comportent un premier circuit de bascule (4, 5, 6) couplé à la sortie du circuit NON-OU pour recevoir ledit signal de sortie du microprocesseur afin de le faire basculer respectivement dans ses états en service et hors service.

5. Dispositif d'entrée à touches selon la revendi-

* C L M S *

cation 4, comportant un deuxième circuit de bascule (9) à verrouillage ayant une première entrée couplée à la sortie du premier circuit de bascule et sa sortie couplée à l'entrée du mode d'attente en basse puissance du microprocesseur.

6. Dispositif d'entrée à touches selon la revendication 5.comportant un circuit de retard (7) couplé entre la sortie dudit premier circuit de bascule et une entrée d'un troisième circuit de bascule (8) ayant sa sortie couplée à une entrée inverseuse de remise à zéro du microprocesseur.

* C L M S *