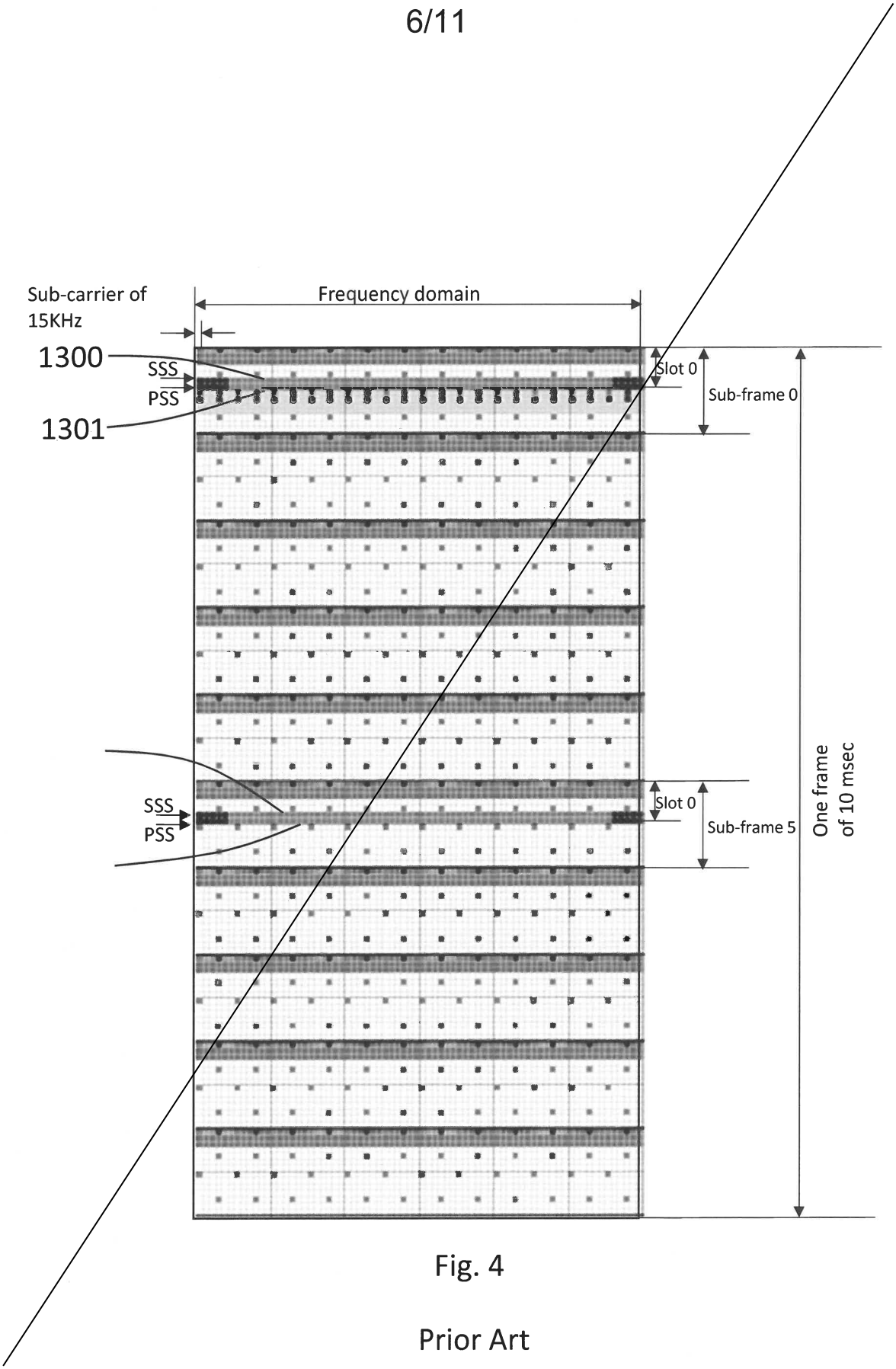



Fig. 4

Prior Art

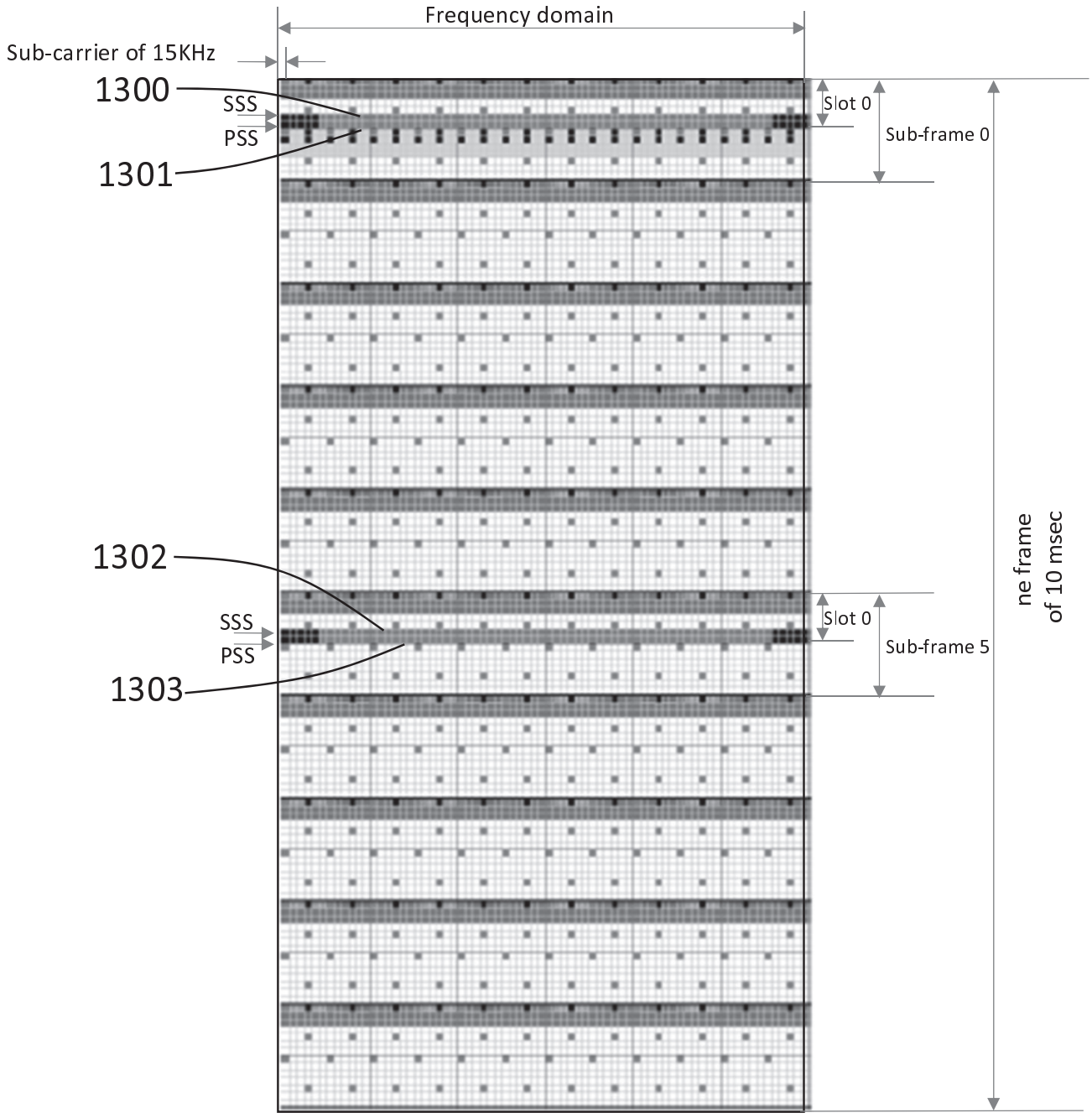



Fig. 4

Prior Art

Fig. 6

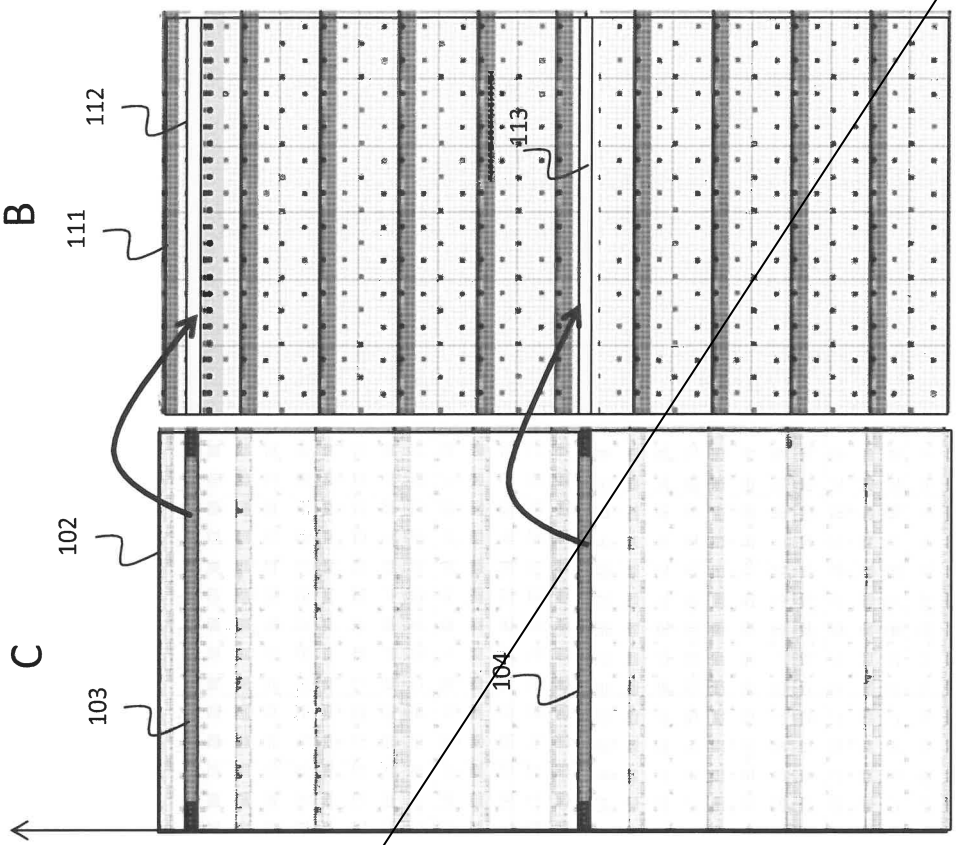



Fig. 5

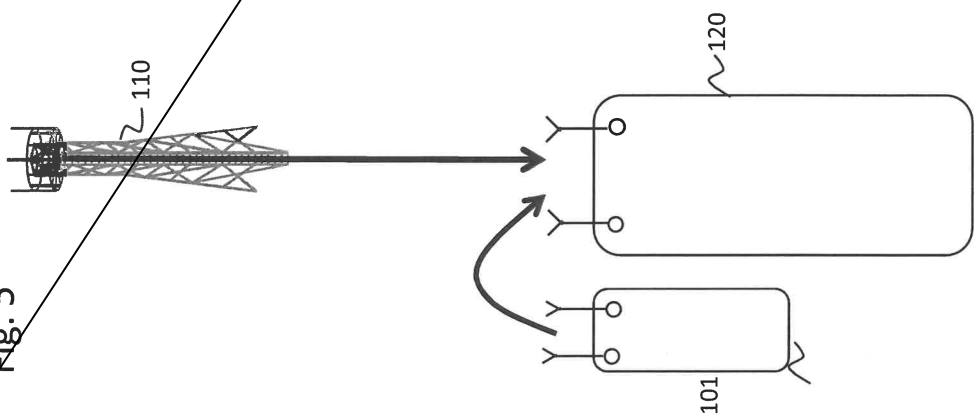


Fig. 6

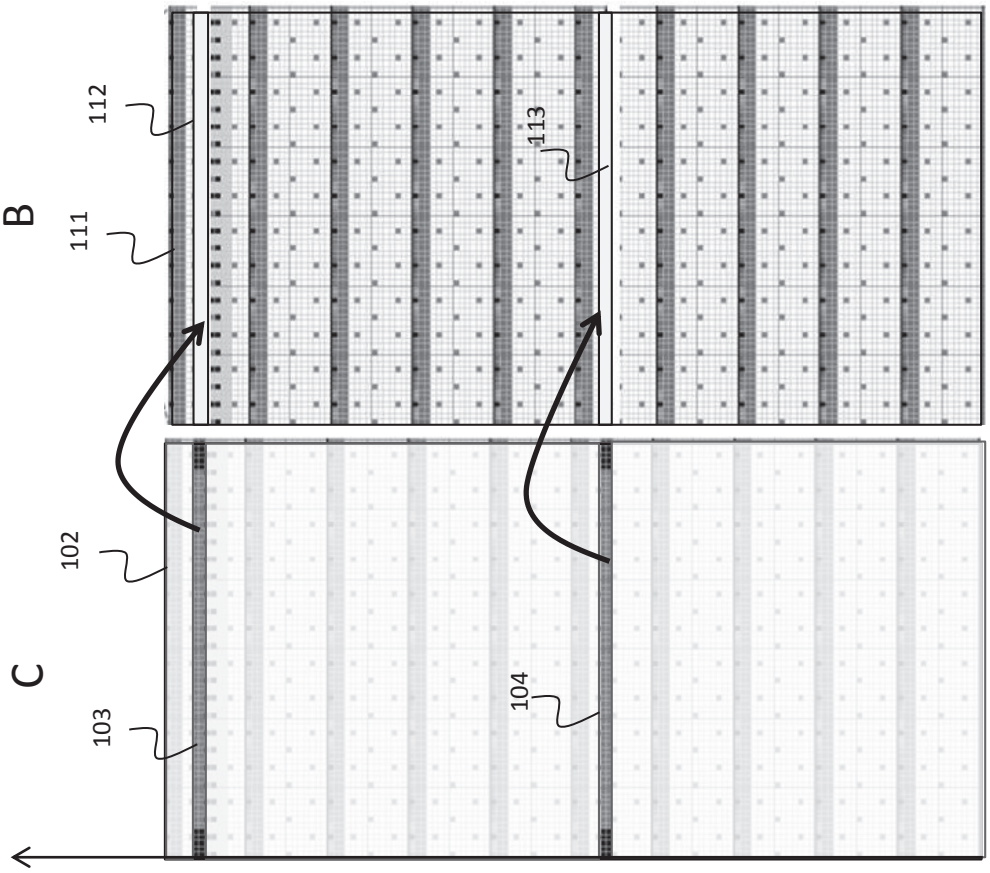



Fig. 5

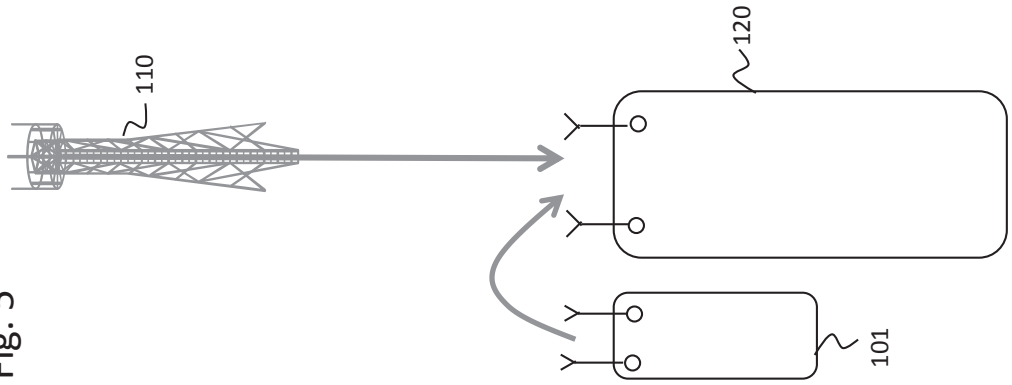


Fig. 8-A

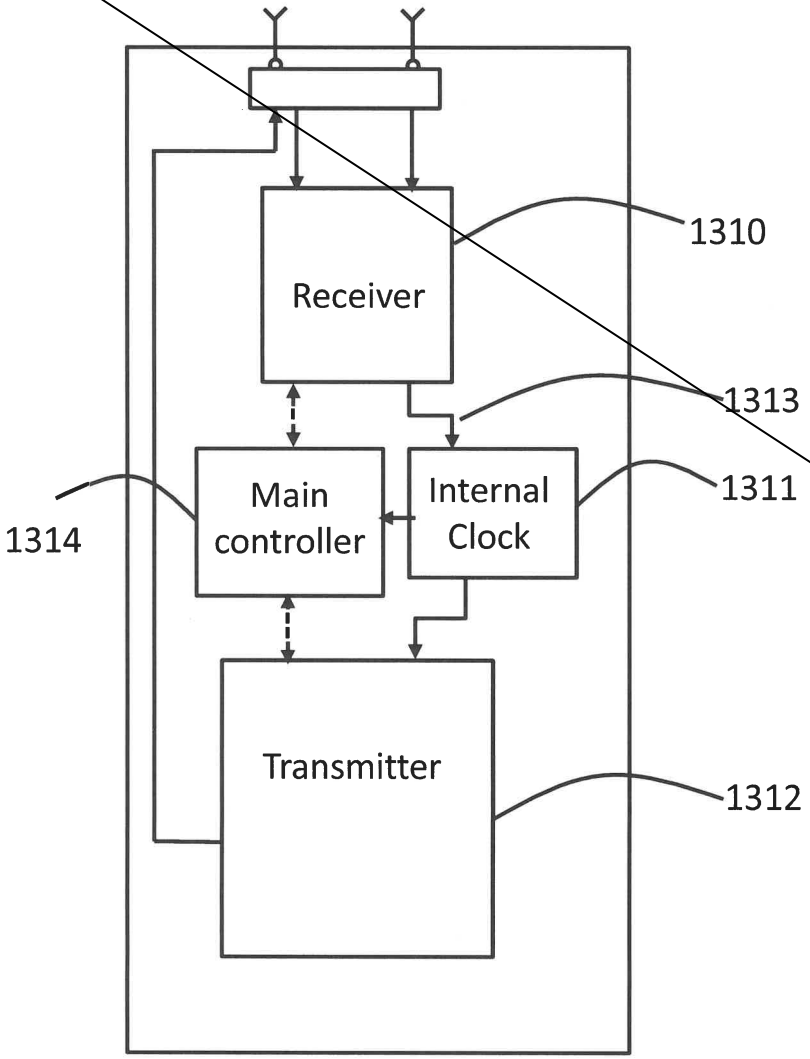

Receiver
1310
1313
Main controller
Internal Clock
1311
1314
Transmitter
1312

Fig. 8-B

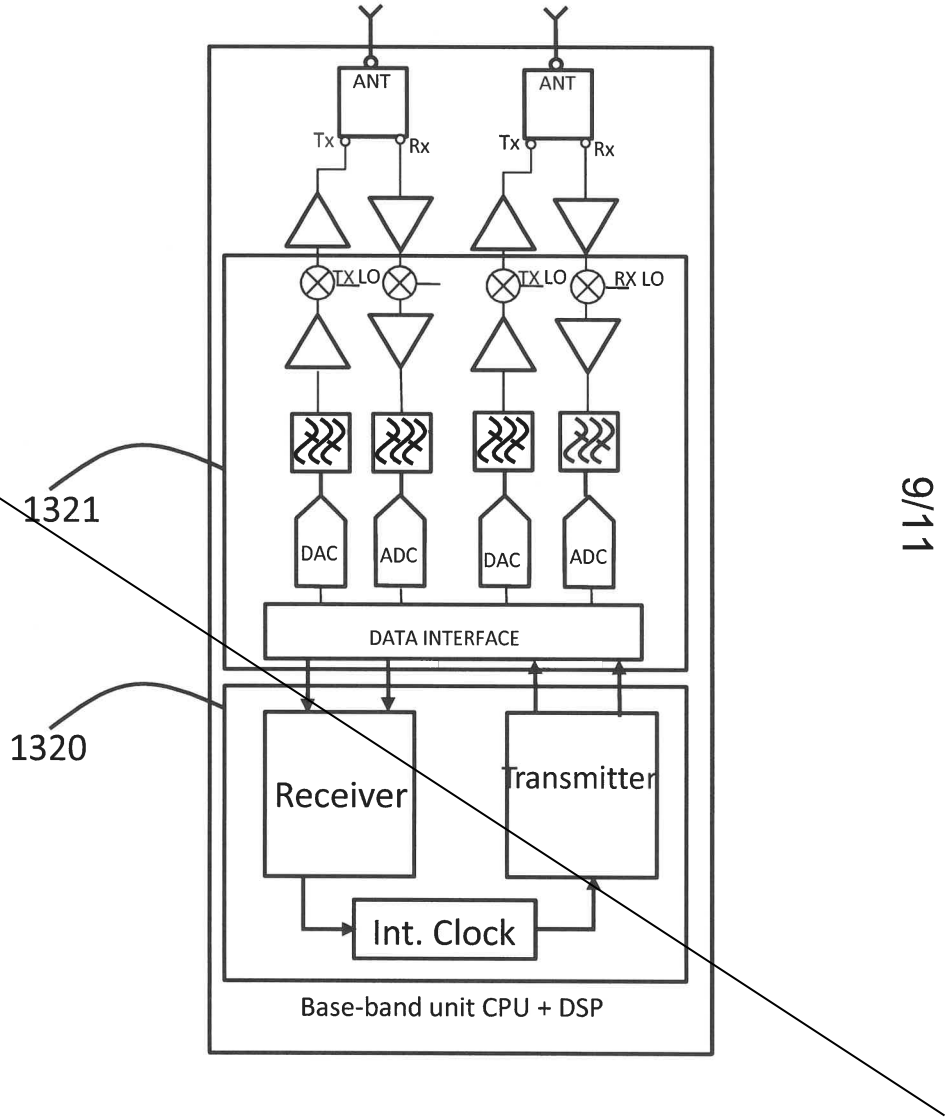

ANT
ANT
Tx
Rx
Tx
Rx
TX LO
TX LO
RX LO
1321
DAC
ADC
DAC
ADC
DATA INTERFACE
1320
Receiver
Transmitter
Int. Clock
Base-band unit CPU + DSP

Fig. 8-A

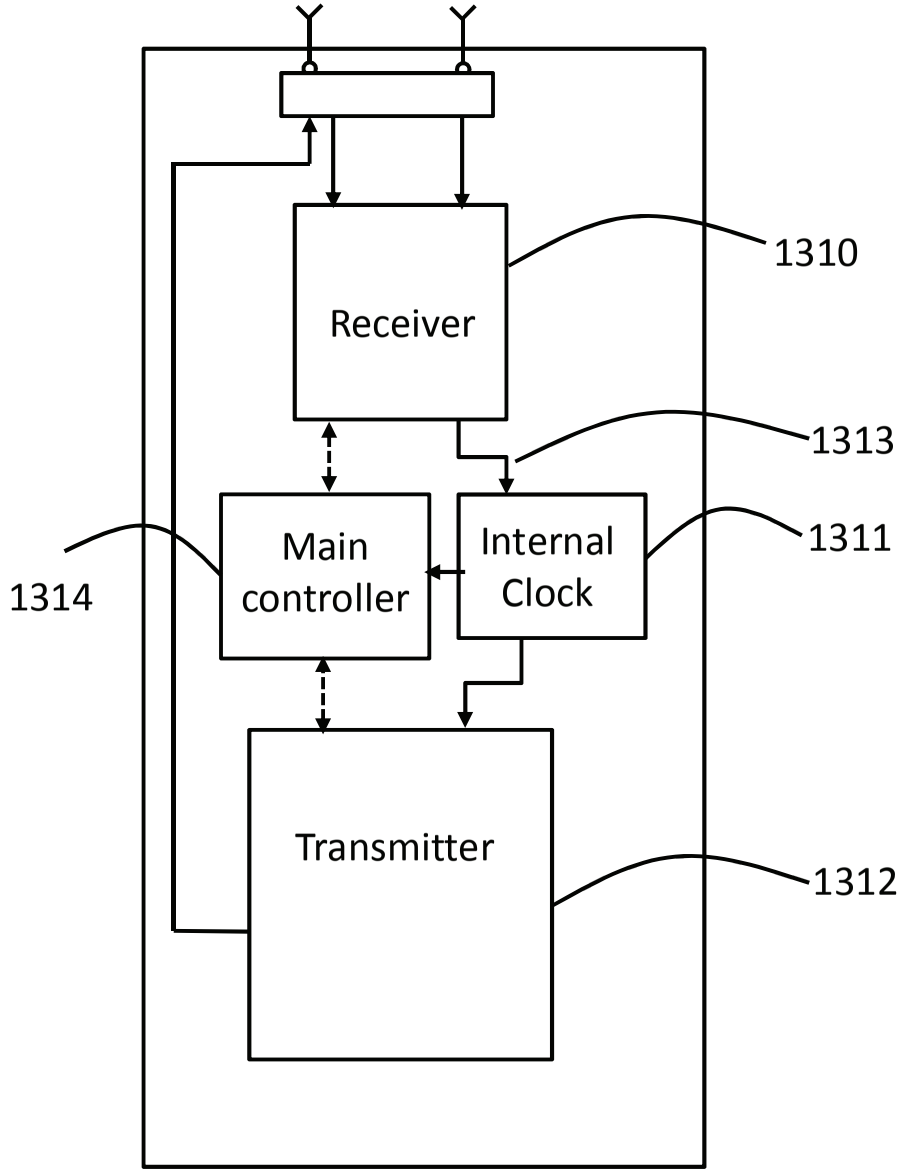

Receiver
1310
1313
Main controller
Internal Clock
1311
1314
Transmitter
1312

Fig. 8-B

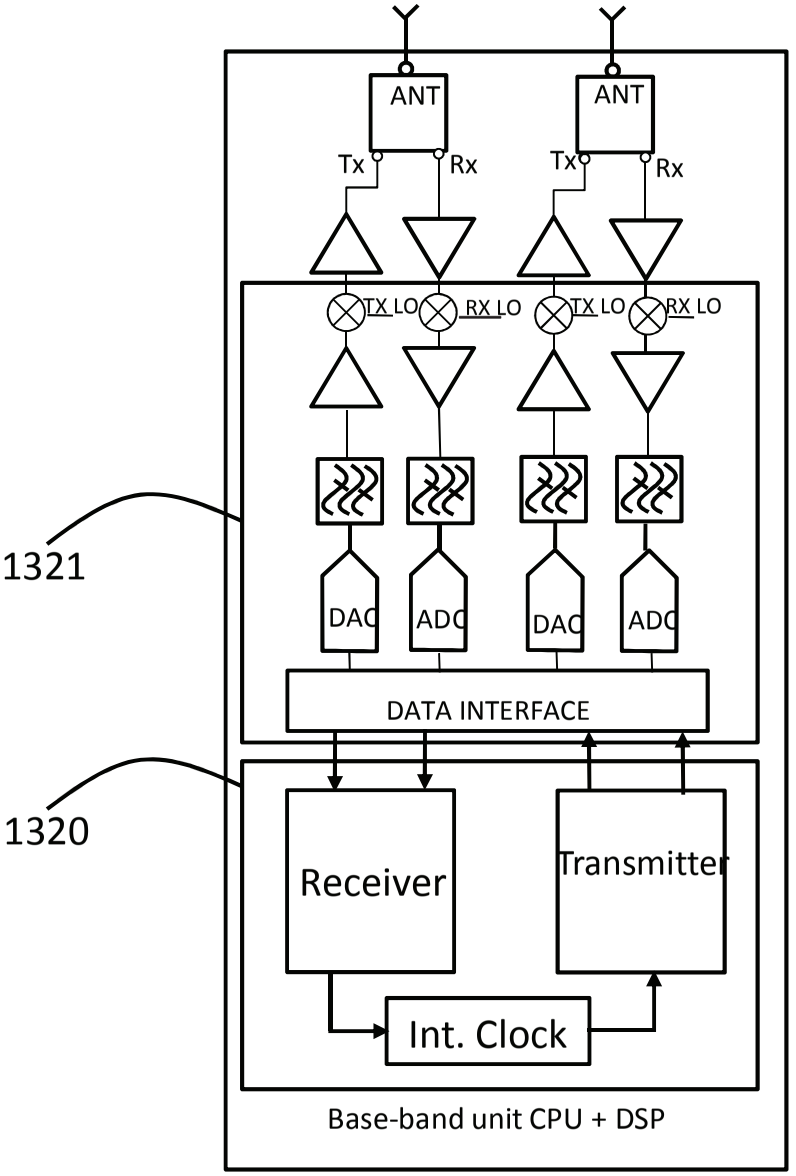

ANT
ANT
Tx
Rx
Tx
Rx
TX LO
RX LO
TX LO
RX LO
DAC
ADC
DAC
ADC
DATA INTERFACE
1321
1320
Receiver
Transmitter
Int. Clock
Base-band unit CPU + DSP

Fig. 10-A

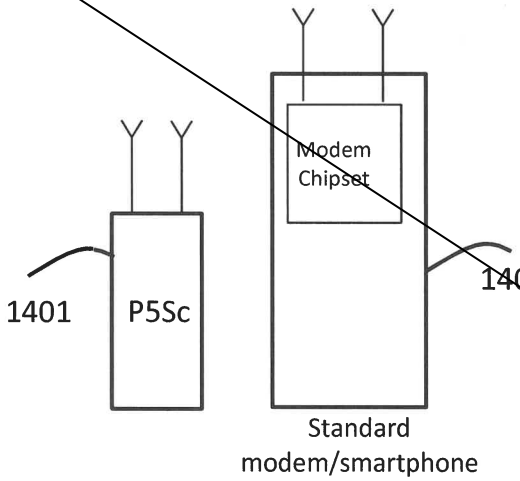



Fig. 10-B

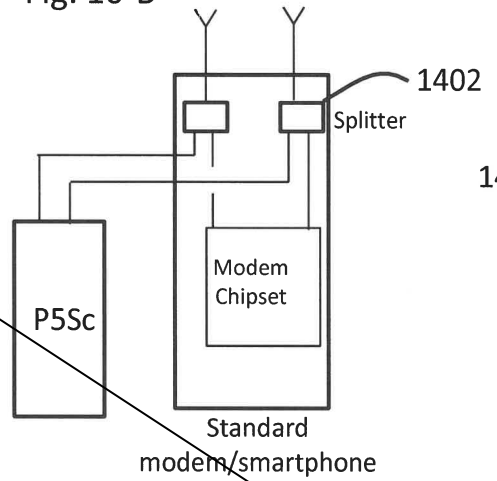



Fig. 10-C

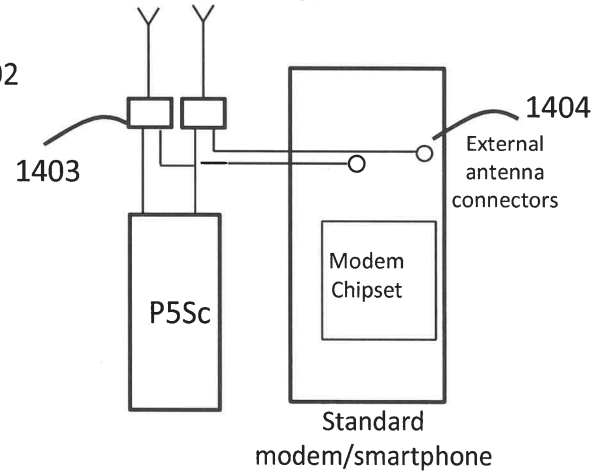



Fig. 11-A

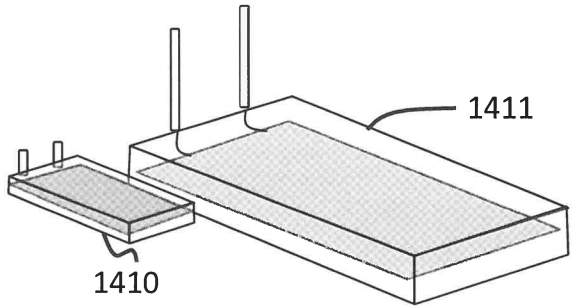



Fig. 11-B

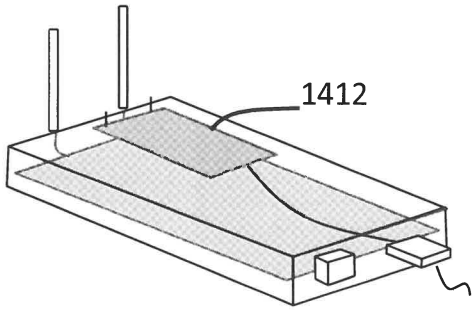



Fig. 11-C

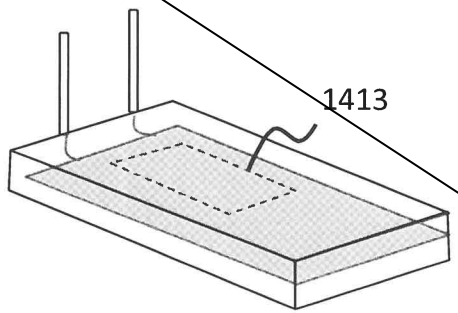


Fig. 10-A

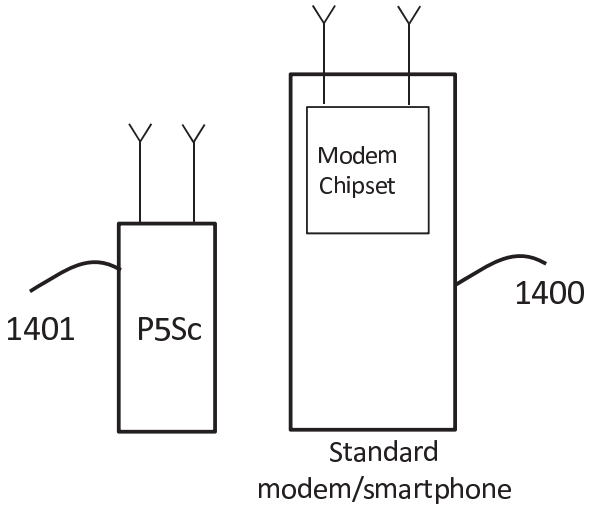



Fig. 10-B

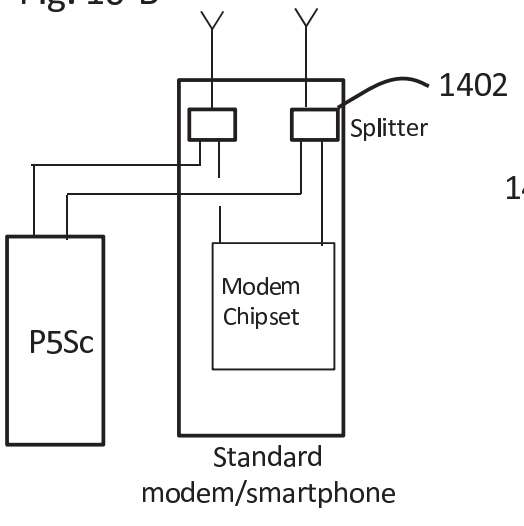



Fig. 10-C

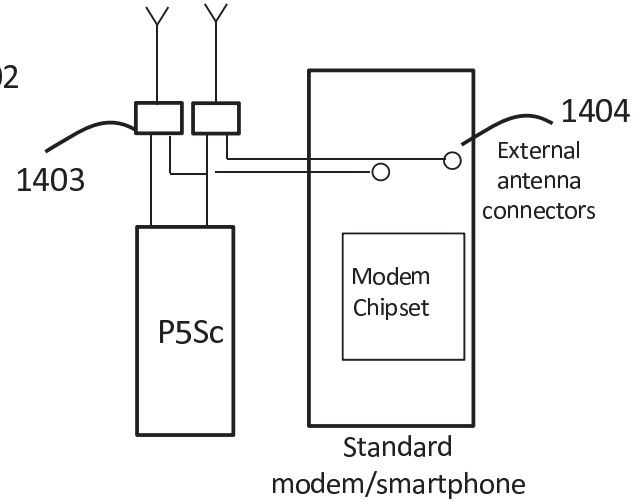





Fig. 11-A

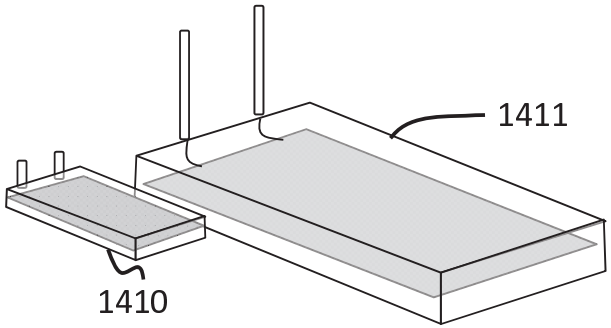



Fig. 11-B

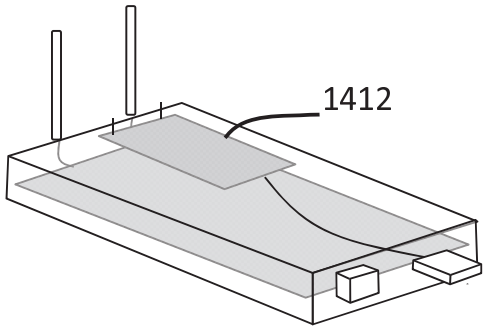



Fig. 11-C

