STEP LDD LDMOSFET

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to lateral double diffused metal oxide semiconductor devices and more particularly to lateral double diffused metal oxide semiconductor devices used in radio frequency power transistors.

Description of the Related Art

Lateral diffused metal oxide semiconductors (LDMOS) and their related radio frequency (RF) LDMOS devices are being utilized in wireless communication applications such as digital audio broadcasting (DAB) and the mobile telephone technologies.

Advances in LDMOS technologies have made LDMOS devices competitive with GaAs devices and are an improvement over SiGe devices when choosing technologies for RF power amplifiers in, for example, wireless telephone base stations.

There is an ongoing effort to improve the performance of LDMOS devices by optimizing silicon circuit layouts and by reducing gate resistance. Furthermore, LDMOS performance continues to be hampered and limited by a large parasitic feedback capacitance between the gate and drain of the device (C_{gd}). Parasitic capacitance reduces the maximum amount of RF output power that the LDMOS device can provide. The RF output power of an LDMOS device decreases drastically as the C_{gd} parasitic capacitance increases.

Thus, what is needed is a new LDMOS structure that reduces parasitic feedback capacitance in order to increase the overall available power output of the LDMOS device without negatively affecting the device's performance.

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SUMMARY OF THE INVENTION

Embodiments of the present invention overcome the above-mentioned drawbacks of previous LDMOS devices by providing a reduced gate-to-drain capacitance and a low drain to source resistance over the operating range of the device.

One embodiment of the present invention is an LDMOS device that includes a gate with an oxide layer. The lightly doped drain has a first and second portion such that the first portion is adjacent to the gate. The second portion is more heavily doped than the first portion and is positioned away from the gate and adjacent to the drain terminal of the device.

BRIEF DESCRIPTION OF THE DRAWINGS

Various objects and advantages of this invention will become apparent and more readily appreciated from the following description of the presently preferred exemplary embodiments, taken in conjunction with the accompanying drawings, of which:

FIGURE 1 depicts a cross-section structure of an RF LDMOS;

FIGURE 2 depicts a cross-section portion of a LDMOS having a deep LDD;

FIGURE 3 depicts a cross-section portion of a LDMOS having a shallow LDD; and

FIGURE 4 depicts an embodiment of the present step LDD LDMOS.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EXEMPLARY EMBODIMENTS OF THE PRESENT INVENTION

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the

embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and will convey the invention to those skilled in the art.

Referring to FIGURE 1, an LDMOS 10 is depicted. A polysilicon gate electrode 12 is on top of an oxide layer (not specifically shown). A gate-drain capacitance C_{gd} 20 is created between the gate 12 and a lightly doped drain (LDD) portion 22, which abuts a n well 24 at the drain region 14.

When used in RF systems, the gate-drain parasitic capacitance C_{gd} 20 of the LDMOS 10 negatively influences the performance of the device. Minimizing the C_{gd} 20 is advantageous to improving device's performance. As shown in FIGURE 2, the C_{gd} is made up of C_{ox} and C_{si} in series. To reduce the C_{gd}, both C_{ox} and C_{si} must be minimized.

A first technique for decreasing the C_{gd} 20 is by increasing the gate oxide thickness 18 (See FIGURES 2 and 3) (D-oxide), this reduces the C_{OX} but an increase of the gate oxide thickness (D-oxide) 18 undesirably reduces the transconductance of the LDMOS 10, resulting in a poor RF performance.

A second technique, which reduces the parasitic capacitance C_{gd} 20, is to reduce the doping concentration in the LDD 22' region (see FIGURE 3). This reduces the C_{si}. A drawback with decreased doping of the LDD 22' region is an increase of LDD resistance. For most applications LDMOS is required to have a breakdown voltage of 75 volts or more. In order to have a breakdown voltage of 75 volts or more, the LDD needs to be as long as about 3um. The light doping and the length of the LDD 22' contributes significantly to the on-state resistance of the device. The LDD resistance can be reduced by increasing the doping of the LDD 22", but it causes the C_{si} to increase (see FIGURE 2).

An exemplary LDMOS design which eliminates the trade-offs of the above two techniques has been established via a stepped LDD structure which reduces the C_{si} without increasing the LDD resistance. In order to take advantage of parasitic capacitance reducing aspect of (1) increasing the gate oxide thickness D-oxide 18 and (2) decreasing the doping amount of the LDD 22, while limiting the drawback of the two changes, it is important to review

the following. FIGURE 2 depicts an enlarged view of a portion of an LDMOS 10". The gate-drain parasitic capacitance C_{gd} is calculated as:

$$C_{gd} = C_{ox}C_{si}/(C_{ox} + C_{si})$$

The (C_{ox}) is a function of the L-overlap area 24 and the oxide thickness 18. The capacitance C_{si} 30 is related to the junction depth and doping concentration of the LDD region 22. As shown in FIGURES 2 and 3, a deep LDD 22" junction depth creates a large L-overlap 24" and a shallow LDD 2' junction depth creates a small L-overlap 2' length. Furthermore, a deep or heavily doped LDD 22" creates a large C_{si} and a shallow or lightly doped LDD 22' created a small C_{si}.

FIGURE 3 depicts the lower C_{gd} of FIGURE 2 and 3 because both the LDD 22' is shallow or lightly doped and the L-overlap area 24" is small.

Referring now to FIGURE 4, a portion of an exemplary step LDD LDMOS 400 is shown. The gate 402 rests on an oxide layer 404 which has a predetermined thickness D-oxide thereby creating a capacitance C_{ox} 406. A stepped LDD 408 is established between the gate 402 and the drain (not specifically shown in this figure). The stepped LDD 408 comprises two portions. First, an LDD1 portion 410 which has a low doping concentration and a shallow junction with the gate oxide region 404. The second portion, the LDD2 portion 412 has a higher dopping concentration than LDD1 410 thereby establishing a deeper doped well than LDD1 410 junction. The stepped LDD 408 technology allows a device designer to choose the LDD1/LDD2 conditions or relationships suitable to create a low C_{gd} and a low on-state resistance at the same time. The light doping in LDD1 410 enables to release the high electric field and then reduce the electron-hole generation at drain bias. This improves the hot-carrier immunity.

The step LDD portion 408 can be made in a two-step process wherein the LDD1 portion 410 doped first and the LDD2 portion 412 is doped using an additional mask. The shallow junction LDD1 410 can be formed by using a low energy implant (such as arsenic), with a low dosage in the area of $-e^{11}/cm^2$. The deeper junction LDD2 412 can be formed using a high energy implant (such as phosphorus), at a higher dosage level of about $-e^{12}/c^2$.

Although various preferred embodiments of the invention have been shown and described, it will be appreciated by those skilled in the art that changes may be made to these embodiments without departing from the principles and the spirit of the invention, the scope of which is defined in the appended claims.

WHAT IS CLAIMED IS:



1. An LDMOS device comprising:

a gate;

an oxide layer below said gate;

a stepped lightly doped drain portion adjoining said oxide layer, said stepped lightly doped drain portion being doped in a stepped manner having a first portion and a second portion such that said first portion is adjacent to said gate and is doped to a lesser degree than said second portion which is distally positioned from said gate.

2. The LDMOS device of claim 1, wherein said first portion is doped with a low energy implant.

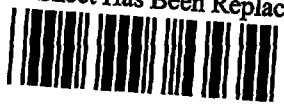
3. The LDMOS device of claim 1, wherein said second portion is doped with a high energy implant.

4. The LDMOS device of claim 1, further comprising a drain portion, said drain portion being adjoining to said second portion of said stepped lightly doped drain portion.

5. The LDMOS device of claim 1, wherein the dopant quantities for doping said first portion and said second portion are selected to minimize the gate to drain capacitance and further to minimize an effective resistance of said stepped lightly doped drain portion.

6. An LDMOS device, comprising:

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a stepped drain portion having a proximate end being overlapped by said gate portion;

a drain terminal portion adjacent to a distal part of said stepped drain portion;

said stepped drain portion being doped in a stepped manner such that said proximate end of said stepped drain portion is doped to a lesser degree than said distal part of said stepped drain portion.

7. The LDMOS device of claim 6, wherein said gate portion further includes a gate terminal and an oxide layer, said oxide layer being a between said gate terminal and said stepped drain portion.

8. The LDMOS device of claim 7, wherein said oxide layer has a predetermined thickness.

9. The LDMOS device of claim 6, wherein said stepped drain portion includes a first LDD portion, and a second LDD portion, said first LDD portion being proximate to said gate portion, said second LDD portion being proximate to said drain terminal portion.

10. The LDMOS device of claim 6, wherein said stepped drain portion includes a shallow LDD portion which extends from said gate portion to said drain terminal portion; and a deep LDD portion which is placed a predetermined distance from said gate and extends toward said drain terminal portion.

11. The LDMOS device of claim 10, wherein said deep LDD portion is more heavily doped than said shallow LDD portion.

12. An LDMOS device comprising;

a gate portion;

a drain terminal portion; and

a stepped drain portion between said gate portion and said drain terminal portion, said stepped drain portion being doped a first amount near said drain terminal portion and doped a second amount near said gate portion.

13. The LDMOS device of claim 12, wherein said stepped drain portion comprises a plurality of separately doped co-mingling portions each having different dopant dosages.

14. The LDMOS device of claim 12, wherein said stepped drain portion comprised, at least, an LDD1 portion and an LDD2 portion such that said LDD1 portion is more lightly doped than said LDD2 portion.

