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(71) Applicant: **FTL SYSTEMS, INC.** [US/US]; 1620 Greenview Drive South West, Rochester, MN 55902 (US).

(72) Inventors: **WILLIS, John, Christopher**; 924 Sierra Lane NE, Rochester, MN 55906 (US). **JOHNSON, Joshua, Alan**; 2252 5th Avenue NE, Rochester, MN 55906 (US). **BETCHER, Ruth, Ann**; 2407 30th Avenue NW, Rochester, MN 55901 (US).

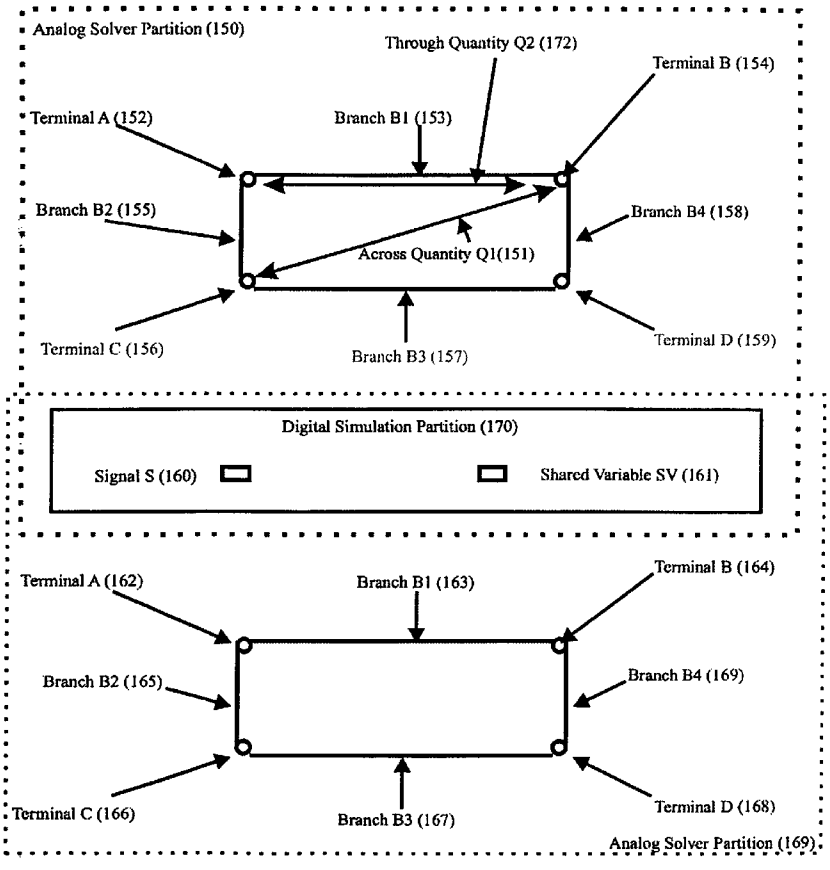
(74) Agent: **LIESKE, Steven, C.**; Oppenheimer Wolff & Donnelly LLP, 45 South Seventh Street, Suite 3300, Minneapolis, MN 55402 (US).

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(54) Title: SIMULATION OF DESIGNS USING RE-CONFIGURABLE LOGIC



(57) Abstract: A means of increasing the steady-state simulation speed of a design comprising digital (Fig. 1-170), analog (Fig. 1-150), mixed-signal and full-wave components is taught using general purpose processors and electronically re-configurable logic. The innovative compilation and execution method disclosed uses either a single compilation step before the onset of simulation or incremental compilation during simulation to yield multiple, optimized processor instructions, logic configurations and interconnect configurations specific to the operating contexts encountered during execution embedded within a pseudo-static execution schedule. Caching provides for rapid re-use of compilation results specific to an operating context. Key innovative steps embodied in the apparatus include representing time-varying changes in design state rather than the actual value of design state at each time point, encapsulation of component model functionality, dynamically varying numerical range in hardware, and integration of a reduced latency interconnect in close proximity to the acceleration resources.

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