CLAIMS

1. A photonic-electronic integrated circuit chip formed on a semiconductor-on-insulator substrate, which semiconductor-on-insulator substrate comprises an embedded dielectric layer and an active layer of semiconductor material, said chip comprising an electronic circuit portion and a photonic interconnection interface of the electronic circuit portion co-integrated in the active layer and being characterized in that the electronic circuit portion is formed in an active layer region, the thickness of which is greater than the thickness of an active layer region in which said photonic interface is formed.

2. The chip according to Claim 1, wherein the active layer region in which said photonic interface is formed is sandwiched between the embedded dielectric layer and a surface dielectric region and the active layer region in which the electronic circuit portion is formed is devoid of a surface dielectric layer.

3. The chip according to any of Claims 1 and 2, wherein the thickness of the active layer region in which the electronic circuit portion is formed is greater than 0.2 μm, preferably greater than 0.5 μm.

4. The chip according to any of Claims 1 to 3, wherein the thickness of the active layer region in which said photonic interface is formed ranges between 0.2 μm and 0.5 μm.

5. The chip according to any of Claims 1 to 4, wherein the thickness of the embedded dielectric layer is greater than 1 μm, preferably greater than 2 μm.

6. The chip according to any of Claims 1 to 5, wherein the photonic interface comprises at least one waveguide and preferably an active photonic circuit portion.

7. The chip according to any of Claims 1 to 6, wherein the electronic circuit portion comprises a transistor logic module, with the transistors being of the FinFET or GAAFET type, for example.

8. A semiconductor-on-insulator substrate comprising a support substrate, an embedded dielectric layer and an active layer of semiconductor material separated from the support substrate by the embedded oxide layer, characterized in that an active layer region intended for forming an electronic circuit portion is thicker than the thickness of an active layer region intended for forming a photonic interconnection interface of the electronic circuit portion.

9. A method for manufacturing a semiconductor-on-insulator substrate according to Claim 8, comprising transferring the active layer from a donor substrate to the support substrate, said transferring comprising bonding the donor substrate and the support substrate with an oxide layer at the bonding interface.

10. The method according to Claim 9, further comprising localized etching of the transferred active layer in order to form the active layer region intended for forming the photonic interconnection interface.

11. The method according to Claim 10, further comprising forming a dielectric layer on the surface of the active layer region intended for forming the photonic interconnection interface.

12. The method according to Claim 9, further comprising forming the active layer region intended for forming the electronic circuit portion by means of localized epitaxial growth.

13. The method according to Claim 12, wherein the formation of the active layer region intended for forming the electronic circuit portion is preceded by steps of oxidizing the transferred active layer in order to form a dielectric layer and localized removal of the

dielectric layer, with the remaining dielectric layer after localized removal acting as a mask for the localized epitaxial growth.

14. The method according to Claim 12, comprising forming a dielectric layer on the surface of an active layer region that has not been subject to localized epitaxial growth.

15. A method for manufacturing a photonic-electronic integrated circuit chip, comprising the following steps:

- manufacturing a semiconductor-on-insulator substrate in accordance with the method according to Claim 9;
- forming an electronic circuit portion in the active layer region intended for forming an electronic circuit portion;
- forming a photonic interconnection interface in the active layer region intended for forming a photonic interconnection interface of the electronic circuit portion.

16. The method according to Claim 15, wherein manufacturing the semiconductor-on-insulator substrate comprises, before or after all or part of the formation of the photonic interconnection interface, forming a dielectric layer on the surface of the active layer region intended for forming the photonic interconnection interface.