METHOD FOR PROVIDING ELECTRICAL CONNECTIONS TO SPACED CONDUCTIVE LINES

FIELD OF THE INVENTION

[0001] Embodiments described herein relate generally to the fabrication of integrated circuits, and more specifically to providing electrical connections to spaced conductive lines, e.g. spaced parallel lines, in integrated circuits.

BACKGROUND OF THE INVENTION

[0002] Electrically conductive lines form many common components of integrated circuits. Dynamic random access memory (DRAM) circuitry, for example, incorporates multiple parallel conductive lines to form wordlines and bitlines. In order to increase capacity and accommodate smaller devices, there is constant pressure to increase the density of components on these and other circuits. The continual reduction in feature sizes places greater demands on the techniques used to form the features.

[0003] Photolithography is a commonly used technique for patterning integrated circuit features. One example of a photolithographic method for forming conductive lines using conventional photolithographic techniques is illustrated in FIGS. 1A through 1D. FIG. 1A shows a substrate 11, such as a semiconductor substrate or an insulating material substrate. For forming word lines on a semiconductor substrate 11, materials are sequentially deposited over a semiconductor substrate 11, including a gate oxide material 31, a polysilicon material 35, a metal silicide material 37, and an oxide top material 41. The last set of materials deposited comprise a photo patterning stack, which may include photoresist anti-reflective coatings and hardmask materials. Any photoresist materials 33 may be used for the photo patterning stack, including positive photoresist materials (such as DNQ-Novolac) and negative photoresist materials (such as SU-8). In this example, a negative photoresist is used, so that when the photoresist material 33 is exposed

to light through a mask (at portions 60, 61) and developed, the area that has not been exposed to light is dissolved.

[0004] FIG. 1B shows the remaining photoresist material 33 after unexposed portions of the material have been removed. The remaining photoresist material 33 is used as an etch mask for an etching process. In the etching process, portions of the of the gate oxide 31, polysilicon 35, metal silicide 37 and oxide top material 41 that are not covered by the photoresist material 31 are removed by, for example, wet or dry chemical etch. After the etch, the remaining photoresist material 33 is dissolved. FIG. 1C illustrates a cross sectional view of the resulting stack. Once the desired layers have been patterned, an encapsulation insulating material 51 can be deposited and etched. Any suitable insulating material 51, such as an oxide, may be used. FIG. 1D shows an insulating material 51 that has been deposited over the materials and etched from the substrate 11. The encapsulation covers the top and both sides of the underlying materials 31, 35, 37, and 41. Other known techniques for forming an encapsulation insulating material 51 over the materials 31, 35, 37 and 41 can also be used.

[0005] There are limitations on how close line features, such as conductive lines, can be patterned using such known photolithographic techniques. The size of line features on an integrated circuit are conventionally described by their "pitch," which is the distance between an identical point on two neighboring features. Features are typically defined by spaces between adjacent features, and so the pitch can be viewed as the sum of the width of a line feature (x in FIG. 1D) and the width of the space separating that line feature from a neighboring line feature (y in FIG. 1D). The "half pitch" is half the sum of the feature width x and the width y of the space between features. Due to factors such as optics and light or radiation wavelength, there is a minimum pitch below which line features cannot be reliably formed using conventional photolithographic techniques. Conventional photolithographic techniques, one example of which is illustrated in FIGS. 1A-1D, can form parallel spaced conductive lines with a half pitch as low as about 45nm. More advanced photolithographic techniques, such as double patterning and spacer pitch doubling, enable the

formation of conductive lines with a half pitch as low as about 20nm. Examples of these techniques can be found in U.S. Patent No. 5,378,649 to Huang (double-patterning), and U.S. Patent No. 5,328,810 to Lowrey et al. (spacer pitch doubling).

[0006] Recently developed non-lithographic techniques, such as polymer self assembly, have also made it possible to form parallel conductive lines with even smaller spacing between adjacent lines. For example, using block copolymer (BCP) self assembly, conductive lines with a half pitch below 20nm are achievable. FIGS. 2A and 2B illustrate patterns formed using BCP self assembly techniques. The process of forming self-assembled patterns involves the deposition of a thin BCP film composed of, for example, polystyrene (PS) and polymethylmethacrylate (PMMA) (referred to as PS-b-PMMA). This is followed by thermal annealing above the glass transition temperature of the BCP. The quality of the resulting pattern depends on process conditions including film thickness, annealing time, and annealing temperature. FIG. 2A illustrates BCP cylinders 80 (comprising, for example, PS) formed in a matrix phase material 82 (comprising, for example PMMA). Notice that the cylinders do not naturally align in a symmetrical pattern. Various methods can be employed in order to control the orientation of the cylinders, including the use of external thermal or electric fields, shear stress or flow, chemical nanopatterning, or graphoepitaxy. FIG. 2B illustrates parallel spaced copolymer cylinders 80 formed using a graphoepitaxy technique, wherein surface relief (in the form of trenches 84) is used to induce orientation.

[0007] Once formed, the BCP cylinders 80 can be used as a sacrificial template for patterning underlying materials, similar to the way photoresist material is used in conventional photolithographic methods. To accomplish this, the PMMA material is chemically removed by exposure to UV light and immersion in a developer, such as an acetic acid developer. The remaining PS cylinders can then be used as a mask to etch underlying materials, such as a conductive material or (more typically) a hardmask. BCP cylinders 80 can also be metalized to function as conductive lines. BCP cylinders 80 can be metalized by, for example, soaking the cylinders in an acidic metal salt solution. For more information on BCP self assembly techniques, see C. T. Black, et al., *Polymer Self Assembly in*

Semiconductor Microelectronics, 51 IBM J. Res. & Dev. 605 (IBM 1997) and J. Chai, et al., *Assembly of Aligned Linear Metallic Patterns on Silicon*, 2 Nature Nanotechnology 500 (Nature Publishing Group 2007).

[0008] As techniques such as double patterning, spacer pitch doubling, and BCP self-assembly enable the creation of more closely spaced conductive lines, it becomes increasingly difficult to make an electrical connection to a particular line without overlapping and shorting between adjacent lines. Using traditional lithographic techniques, electrical connection pad sites also known as contact landing pads are too large to make contact with only a single conductive line in a group of closely spaced conductive lines. Present lithography technology does not have the resolution or alignment capability to print the patterns necessary to make connection sites for these smaller features. Thus, there exists a need for a technique to make electrical connections to closely spaced conductors and which may also be used to make electrical connections to any spaced apart parallel conductors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGS. 1A through 1D illustrate a conventional photolithographic method of forming conductive lines over a substrate.

[0010] FIGS. 2A and 2B illustrate self-assembled block copolymer (BCP) patterns.

[0011] FIGS. 3A and 3B illustrate top down and cross-sectional views of parallel mask lines formed on a substrate.

[0012] FIGS. 4A and 4B illustrate top down and cross-sectional views of parallel mask lines formed on a substrate covered with a photoresist material.

[0013] FIGS. 5A through 5C illustrate top down and cross-sectional views of parallel mask lines partially covered by a cutting mask.

[0014] FIGS. 6A and 6B illustrate top down and cross-sectional views of mask lines after etching angled line ends using the cutting mask illustrated in FIGS. 5A through 5C.

[0015] FIG. 7 illustrates a top down view of an embodiment with parallel mask lines having angled faces and isotropically grown contact landing pad masks.

[0016] FIG. 8 illustrates a top down view of an embodiment with parallel mask lines having angled faces and anisotropically grown contact landing pad masks.

[0017] FIGS. 9A through 9C illustrate perspective and cross-sectional views of an embodiment with parallel conductive lines with electrical contact landing pad areas formed by using mask lines and contact landing pad masks as an etch mask.

[0018] FIGS. 10A and 10B illustrate cross-sectional views of the formation of an electrical connection to a contact landing pad.

[0019] FIGS. 11A through 11C illustrate perspective and cross-sectional views of an embodiment with single-layer conductive lines.

[0020] FIGS. 12A through 12C illustrate perspective and cross-sectional views of an embodiment using a cutting mask as an insulating material to confine growth of mask pads.

[0021] FIG. 13 illustrates a perspective view of an embodiment with parallel BCP cylinders having angled faces and isotropically grown mask pads.

[0022] FIG. 14 illustrates a perspective view of the embodiment of FIG. 13 after the BCP cylinders and respective mask pads have been used as an etch mask to etch underlying conductive materials.

[0023] FIG. 15 illustrates a perspective view of example conductive lines after cutting angled line ends in accordance with another embodiment.

[0024] FIG. 16 illustrates a perspective view of an embodiment with parallel conductive lines having angled faces and isotropically grown electrical contact landing pads.

[0025] FIGS. 17A and 17B illustrate an example technique for forming electrical connections to the electrical contact landing pads formed in FIG. 16.

[0026] FIG. 18 illustrates a perspective view of an embodiment with parallel conductive lines having angled faces and anisotropically grown electrical contact landing pads.

[0027] FIG. 19 illustrates a perspective view of another embodiment with a single metal layer forming conductive lines having angled faces and anisotropically grown electrical contact landing pads.

[0028] FIG. 20 illustrates a perspective view of an embodiment using a cutting mask as an insulating material to confine growth of electrical contact landing pads.

[0029] FIG. 21 illustrates a perspective view of an embodiment with parallel BCP cylinders forming conductive lines with angled faces and isotropically grown electrical contact landing pads.

DETAILED DESCRIPTION OF THE INVENTION

[0030] Embodiments described herein address the problems with current techniques for making electrical connections to closely spaced conductive lines, e.g. parallel lines with spacing of less than 45nm in width, and provide electrical connections to such closely spaced conductive lines. The embodiments described herein can also be used to make electrical connections to any spaced conductive lines including those formed using conventional photolithographic techniques.

[0031] It should be understood that embodiments of the invention are not limited by the example embodiments described herein and that changes can be made thereto. The embodiments described herein can be applied to any integrated circuit that has spaced

lines, and is particularly suitable for making connections to parallel conductive lines including closely spaced parallel conductive lines, for example, parallel conductive lines having a spacing of 45nm or less between them, and more particularly to such conductive lines having a spacing of 20nm or less between them. These embodiments are particularly well suited for application to memory technology such as dynamic random access memory (DRAM) and other memory devices, which contain closely spaced access lines, for example wordlines and data/source lines, for example bitlines, and to other integrated circuit structures having closely spaced parallel conductive lines.

[0032] The term "substrate" in the following description refers to any supporting material suitable for fabricating an integrated circuit, typically a semiconductor material, but not necessarily so. A substrate may be silicon-based, may include epitaxial layers of silicon supported by a base semiconductor foundation, can be sapphire-based, silicon-on-insulator (SOI), metal, polymer, or any other materials suitable for supporting an integrated circuit. When reference is made to a semiconductor substrate in the following description, previous process steps may have been utilized to form regions or junctions in or over a base semiconductor or foundation.

[0033] Example embodiments are now described with reference to the accompanying figures wherein like reference numbers are used consistently for like features throughout the drawings. FIGS. 3A and 3B illustrate top down and cross-sectional views of parallel spaced mask lines 13 formed over blanket deposited gate stack materials 90, for example, gate stack materials 90 comprising a gate oxide 31, a polysilicon 35, a metal silicide 37, and an oxide top material 41 formed over a semiconductor substrate 11. Though shown here over gate stack materials 90 on a semiconductor substrate 11, the mask lines 13 could be formed above any conductive material of an integrated circuit, including a metal layer. The mask lines 13 comprise a layer of mask material 73 encapsulated by an encapsulation insulating material 51, such as an oxide. The mask material 73 may be any material suitable for use as an etch mask, including photoresist, hardmask, and processed BCP materials, as examples. The mask lines 13 can be formed by any now known or later

developed techniques, including photolithographic techniques and BCP techniques and others used to fabricate closely spaced lines. The mask lines 13 are arranged, in this embodiment, in parallel and extend linearly in one extending direction 29, with a width x and a space y between them. For mask lines 13 formed using current double patterning and spacer pitch doubling techniques, the total mask line width x and space y between mask lines may be between 90nm (a half pitch of 45nm) and 40nm (a half pitch of 20nm). Using BCP self assembly techniques, a mask line with a total line width x and space between y of less than 40nm (a half pitch of 20nm) can be patterned.

[0034] Starting with FIGS. 3A and 3B, one example embodiment for forming connections to closely spaced conductive lines is now described. FIGS. 4A and 4B illustrate top down and cross-sectional views of the FIG. 3A, 3B structure covered with a light-sensitive photoresist material 33. Any common photoresist material 33 may be used, including positive photoresist materials (such as DNQ-Novolac) and negative photoresist materials (such as SU-8).

[0035] Using conventional photolithographic techniques, the photoresist material 33 is selectively exposed to radiation through a mask patterned diagonally across the mask lines 13 so that, when exposed to a suitable developer, the exposed (or unexposed – depending on whether the material is a positive or negative photoresist material) areas of the photoresist are removed. As shown in FIGS. 5A, 5B, 5C, the remaining photoresist material 33 provides an angled profile and forms a cutting mask 43, which can be used to remove exposed materials of the mask lines 13. FIG. 5A illustrates a cutting mask 43 that has been formed at an angle, e.g. between about 5 degrees and 30 degrees relative to the linearly extending direction 29, across the mask lines. FIG. 5B shows a cross-section at a location where the photoresist material 33 has been removed, and FIG. 5C shows a cross-section at a location where the photoresist material 33 forming the cutting mask 43 remains, covering the mask lines 13.

[0036] Next, the area not covered by the cutting mask 43 is etched down to oxide top material 41, removing the exposed portions of the mask lines 13. The remaining photoresist 33 is then removed. FIGS. 6A and 6B illustrate top down and cross-sectional views after the photolithographic and etch process has been completed, and the remaining photoresist material 33 forming the cutting mask 43 has been removed. The mask lines 13 have been cut cross-wise at a diagonal to create angled ends 22. Because of the angled profile of cutting mask 43, each mask line 13 is cut at a different linearly extending location along the extending direction 29 of the lines 13. In the embodiment illustrated in FIGS. 6A and 6B, and as one example, the mask lines 13 may have a width of 15nm, and the cut forms an angle of approximately 10 degrees at the angled ends 22. The resulting length of the exposed angled end 22 is about 68nm, presenting a surface significantly longer than the 15nm width of the mask lines 13. This provides a larger surface area for creating a mask extension for use in forming an electrical contact landing pad, as described below, than if the mask lines 13 were cut cross-wise to form square ends. Additionally, the overall layout of the mask lines 13 – wherein the parallel lines are cut at different respective lengths along the extending direction 29 – provides a larger usable area for forming mask extensions.

[0037] Next, extensions of the parallel mask lines 13, here shown as contact landing pad masks 23, are formed at the angled ends 22 of the parallel mask lines 13, as shown in FIGS. 7, 8, and 9A. The contact landing pad masks 23 are formed by using a material 73 exposed at the angled ends 22 of the mask lines 13 as seed to grow a contact landing pad mask 23 next to the exposed angled ends 22 of each mask line 13. Because the material 73 at the exposed angled ends 22 of each mask line 13 is the nucleation seed for subsequent growth of contact landing pad masks 23, the pad masks 23 are self-aligned to the line ends 22. The self-aligned nature avoids overlay and pattern registration errors associated with photolithograpical patterning methods. FIG. 7 shows isotropic growth of contact landing pad masks 23, and FIGS. 8 and 9A show contact landing pad masks 23 grown anisotropically. Various methods can be used to grow self aligned contact landing pad masks 23 from the mask line 13 materials, depending on the composition of the material 73 within mask lines 13.

[0038] For example, the mask material 73 of the mask lines 13 may be a polymer, such as photoresist material or self-assembled BCP cylinders. In this example, a seed material for selective deposition can been blended with the polymer, or a seed species can be included in the molecular structure of the polymer. For example, a metal seed material may be incorporated in the polymer structure as an organometallic material (by blending) or organometallic functional group (by reacting). After forming the polymer mask 13, the organometallic may or may not be reduced (or oxidized) to facilitate its activity as a seed material, via, e.g. thermal baking or irradative exposure). Alternatively, if seed material is not pre-blended with the polymer, a seed layer may be selectively formed at the angled ends 22 of mask lines 13 by functionalizing a seed material to react with and bond to exposed polymer material 73 at the angled ends 22. The seed material may also be selectively formed on the polymer mask material 73 exposed at the angled ends 22 by using conventional staining techniques. If the mask material 73 is a photoresist, the material 73 may or may not be treated to render them insoluble in the solvent from which the photoresist material 33 of the cutting mask 43 is cast. Such treatment may include thermal cross-linking, acid catalyzed cross-linking, or other commercial "freeze" treatments used for double-patterning photolithography.

[0039] In these examples, where the mask material is a seeded polymer material, extension contact landing pad masks 23 are grown via selective deposition of materials onto the seed material at the angled ends 22. Any now known or later developed selective deposition technique can be used to deposit materials on the seed material. For example, if the seed material is a metal material, then selective chemical vapor deposition (CVD) techniques can be used to deposit materials such as tungsten (W) or titanium (Ti), or Atomic layer deposition (ALD) techniques can be used to deposit materials such as platinum (Pt) and rhodium (Rh) on the seeded material 73. Materials can also be deposited on a metal seeded material 73 using electroless plating techniques, including electroless plating of nickel (Ni), nickel alloy (e.g. NiCoW), cobalt (Co), etc.

[0040] The mask material 73 of the mask lines 13 could also be a hardmask material, such as silicon, polysilicon, or metal. In this example, the extension contact landing pad masks 23 can be grown via selective deposition of materials directly on the mask material 73 exposed at the angled ends 22 of the mask lines 13. For a hardmask material 73 that contains metals, electroless plating or selective CVD, or ALD processed can be used. For a silicon or polysilicon hardmask material 73, epitaxial silicon or polysilicon growth may be used.

[0041] In the presented examples, where the mask material 73 of the mask lines 13 is a seeded polymer or other hardmask material, an encapsulation insulating material 51 formed prior to the photoresist deposition and angled cut of FIGS. 5A through 6B confines nucleation and growth of the extension contact landing pad masks 23 to the mask material 73 exposed at the angled ends 22 of the mask lines 13. For BCP cylinders, matrix phase material surrounding the BCP cylinders could also be used to confine growth to the angled ends 22 of the mask lines 13.

[0042] Also, in the presented examples, a trim or etch-back may be applied to the encapsulation insulating material 51, pulling the material 51 back away from the exposed angled ends 22 of the mask lines 13. A trim or etch-back may or may not be applied in order to regulate the amount of exposed surface for the subsequent selective deposition and contact landing pad growth steps. For electroless plating or selective CVD or ALD processes, the contact landing pad masks 23 may be grown isotropically, as shown in FIG. 7, or anisotropically, as shown in FIGS. 8 and 9A. For epitaxial silicon or polysilicon growth, the contact landing pad masks 23 may be grown anisotropically.

[0043] Once the self-aligned contact landing pad mask 23 is grown, using any of the processes described above, the combined mask pattern can be transferred to the underlying materials via etch to form spaced conductive lines having sufficiently large contact landing pads. FIG. 9A illustrates a perspective view of the mask lines 13 with extension contact landing pad masks 23 grown at the angled ends 22. The mask lines 13 and

associated contact landing pad masks 23 are then used as a hard mask for etching through the underlying materials 31, 35, 37, 41. In FIG. 9B, the combined mask pattern has been transferred to the underlying materials via etch, the remaining mask material has been removed, and an insulating material 71, such as a boron phosphorous silicon glass material has been deposited. The resulting conductive lines 50, which may be provided for use as word lines, have a gate oxide 31, a polysilicon 35, a metal silicide 37, and oxide top material 41. The conductive lines 50 each have a contact landing pad area 25 formed at an end. The angled cut of mask lines 13 and selective growth of extension contact landing pad masks 23 at the mask layer enables the patterning of a sufficiently large electrical contact landing pad area 25, even though the conductive lines 50 may be closely spaced. The electrical contact landing pad areas 25 are sufficiently large to provide an electrical connection to the conductive lines 50, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pad areas 25. FIG. 9C shows a cross section view of the electrical contact landing pad areas 25 of the conductive lines 50 of FIG. 9B.

[0044] FIGS. 10A and 10B illustrate a method of forming electrical connections to the electrical contact landing pad area 25 illustrated in FIG. 9C. In FIG. 10A, a via 55 is formed using conventional techniques. The via is formed through the insulating material 71 and the oxide top material 41, down to the metal silicide 37. A conductive material 45, e.g. polysilicon or metal, is deposited over the insulating material 71, forming an electrical connection to the metal silicide material 37. Thus, electrically isolated electrical connections can be made even though the conductive lines 50 are closely spaced. Though this embodiment is described with reference to forming connections to conductive lines 50 on a semiconductor substrate 11, it should be understood that the technique described herein could be applied to form electrical connections to conductive lines 50 in any conductive layer of a semiconductor device.

[0045] FIGS. 11A through 11C illustrate another embodiment wherein the mask lines 13 with extension contact landing pad masks 23 grown at the angled ends 22 are used to etch into an underlying conductive material. In this embodiment, the conductive

material comprises a single metal layer 67 which may, for example, be provided along an upper level of a semiconductor device. The metal layer 67 is here shown above an insulating material 81, but it could be at any layer of the semiconductor structure. The mask lines 13 with extension contact landing pad masks pads 23 are formed using the same growth techniques described above in reference to FIGS. 7, 8 and 9A, including electroless deposition, selective CVD or ALD processes, or epitaxial silicon or polysilicon growth, as examples, depending on the material 73 used for the mask lines 13. An electrical connection can be made to the electrical contact landing pad 25 illustrated in FIG. 11C using the same technique described above in reference to FIGS. 10A and 10B.

[0046] FIGS. 12A through 12C illustrate yet another embodiment wherein the mask lines 13 with extension contact landing pad masks 23 grown at the angled ends 22 are used to etch into an underlying material stack which may be used for wordlines. This embodiment differs from the embodiment illustrated in FIGS. 9A through 9C in that the lines of mask material 73 are not covered with encapsulation insulating material 51. Here, the photoresist material 33 forming the cutting mask 43 is applied directly over material 73 of lines 13 and is not removed after the mask lines 13 are cut. As a result, the cutting mask 43 acts as an encapsulating growth-confining material during the growth of the extension contact landing pad masks 23, so that growth occurs only at the exposed ends 22 of the mask lines 13. A optional trim or etch-back may be applied to the photoresist material 33 in order to regulate the amount of exposed surface of material 73 for the subsequent selective deposition and contact landing pad growth steps. As in the FIG. 7, 8 and 9A embodiments, contact landing pad masks 23 can be grown using any selective deposition technique, including electroless deposition, selective CVD or ALD processes, or epitaxial silicon or polysilicon growth, as examples, depending on the material used for the mask 73. A connection can be made to the electrical contact landing pad 25 illustrated in FIG. 12C using the same technique described above in reference to FIGS. 10A and 10B.

[0047] In another embodiment, BCP cylinders with extension pad masks 85 are used to pattern both the mask lines 13 and the contact landing pad masks 23. FIG. 13

shows a mask material 73 covered by a self-assembled BCP material with BCP cylinders 80 (comprising, for example, PS) formed in a matrix phase material 82 (comprising, for example PMMA). The BCP cylinders can be formed with a half-pitch below 20nm. The matrix phase material 82 has been selectively exposed to light at an angle across the extending direction of the BCP cylinders 80, and placed in a suitable developer to form an angled mask. The mask formed of the matrix phase material 82 is then used as a cutting mask to cut angled ends 22 in the BCP cylinders 80. Alternatively, the mask and cut could be performed using a conventional photoresist material 33 above the BCP material as a cutting mask 43 to cut the BCP cylinders 80 and the matrix phase material 82 at an angle (or to cut only the BCP cylinders 80 at an angle, if the matrix phase material 82 is removed prior to the mask and cut). An optional trim or etch-back may be applied to the matrix phase material 82. The BCP cylinders may be stained with a metal, such as Pt, W, or other similar metal in order to enhance pattern transfer characteristics and provide a seed material for selective deposition. To form extension mask pads 85 (which will be used to pattern contact landing pad masks 23 in the underlying material), a material at the exposed angled ends 22 of the BCP cylinders 80, such as the stained Pt, W, or other similar metal, acts as seed for growth. Selective deposition of materials on this seed can be performed using processes such as electroless plating or selective CVD or ALD processes. In this embodiment, the matrix phase material 82 or cutting mask 43 confines nucleation and growth of the extension mask pads 85 to the angled ends 22. The extension mask pads 85 may be isotropically (shown) or anisotropically grown.

[0048] Once the extension mask pads 85 have been formed, the matrix phase material 82 is removed through appropriate etching or developing techniques known in the art. The remaining BCP cylinders 80 with extension masks pads 85 can be used as a mask to etch a blanket deposited underlying hard mask material 73. FIG. 14 shows the mask lines 13 with the attached contact landing pad masks 23 formed by this etch of material 73. The remaining underlying materials, including materials 41, 37, 35, and 31, can then be etched using mask lines 13 and the contact landing pad masks 23 using the process described above

in reference to FIGS. 9B and 9C. Electrical connections to the resulting contact landing pads 25 can be formed using the process described above in reference to FIGS. 10A and 10B.

[0049] In another embodiment, line extensions forming electrical contact landing pads 25 can be grown directly on the conductive lines 50. FIG. 15 illustrates a perspective view of example conductive lines 50, such as a wordlines. As an example, these conductive lines 50 have been formed with, an oxide top material 41, a metal silicide 37, and a polysilicon 35 over a gate oxide 31 and a semiconductor substrate 11. The gate oxide 31 is not etched into the conductive line patterns, so that the later formed contact landing pads 25 will be electrically isolated from the semiconductor substrate 11. An insulating material 51, such as an oxide, encapsulates the material stack 35, 37, 41. If the conductive lines 50 are patterned using current double patterning and spacer pitch doubling techniques, the half pitch of the lines may be between about 45nm and about 20nm. Using self-assembled BCP mask and etch techniques, the half pitch of the patterned conductive lines 50 may be from about 20nm and below.

[0050] The conductive lines 50 of FIG. 15 have all been cut at an angle, i.e. an angle of between 5 degrees and 30 degrees relative to the linearly extending direction to form angled ends 22, using the angled cutting mask technique illustrated in FIGS. 4A through 6B to cut the conductive lines 50 and form angled ends 22. In FIG. 15, a trim or etch-back has been performed on the encapsulation insulating material 51, removing material 51 away from the exposed face of materials 31, 35, 37, and 41. A trim or etch-back may or may not be performed in order to regulate the amount of exposed surface for the subsequent electrical contact landing pad 25 growth step. The conductive lines 50 illustrated in FIG. 15 are an example of one conductive line configuration, but the technique described herein can be applied to conductive lines having other configurations and with other conductive materials, for example, a metal line.

[0051] FIG. 16 illustrates isotropic growth of an electrical contact landing pad 25 from an embodiment with parallel conductive lines 50 having angled ends 22 with no

trim or etch back. In this embodiment, like that of FIG. 15, a encapsulation insulating material 51 is formed over conductive lines 50. The extension electrical contact landing pads 25 are formed by using materials exposed at the angled ends 22, such as the polysilicon 35 and/or the metal silicide 37, as examples, as a seed to isotropically grow an electrical contact landing pad 25 at the exposed ends of the conductive line 50. Selective deposition of conductive materials on this seed can be performed using processes such as electroless plating or selective CVD or ALD. The encapsulation insulating material 51 confines nucleation and growth to the angled ends 22. The electrical contact landing pads 25 are self-aligned to the angled end 22, the latter of which forms the seed layer for electrical contact landing pad 25 growth. FIG. 16 shows the electrical contact landing pad 25 as an isotropic growth, however, an anisotropic growth may also be performed.

[0052] FIG. 17A shows in top view and 17B shows in cross sectional view a method of making an electrical connection to a conductive line 50 having an electrical contact landing pad 25, such as the conductive line of FIG. 16. The conductive line 50 has been cut at an angle, and an electrical contact landing pad 25 has been isotropically grown from the angled end 22. Using conventional techniques, a via 55 is formed through an insulating material 71 above the electrical contact landing pad 25. A connecting metal material 45 is deposited over the insulating layer and the via 55 so that it forms a connection to the electrical contact landing pad 25.

[0053] FIG. 18 illustrates a perspective view of another embodiment with conductive lines 50 having the construction of FIG. 15 and having angled ends 22 and here showing anisotropically grown electrical contact landing pads 25. In this embodiment, like that of FIG. 16, an encapsulation insulating material 51 is formed over the conductive lines 50, and no etch-back has been applied at the angled ends 22. The extension electrical contact landing pads 25 are formed using the same growth techniques described above in reference to FIG. 16, including electroless deposition or selective CVD or ALD on the polysilicon 35 and/or the metal silicide 37 materials. An electrical connection can be made to the electrical

contact landing pad 25 illustrated in FIG. 18C using the same technique described above in reference to FIGS. 17A and 17B.

[0054] FIG. 19 illustrates another embodiment with conductive lines 50 having angled ends 22 and anisotropically grown electrical contact landing pads 25. The embodiment of FIG. 19 differs from the embodiment of FIG. 18 in that the conductive line 50 comprises a single metal layer 67 encapsulated by insulating material 51. As in the FIG. 18 embodiment, extension electrical contact landing pads 25 are formed by using material exposed at the angled ends 22, here the metal layer 67, as a seed to anisotropically grow an electrical contact landing pad 25 at the exposed ends of the conductive line 50. Selective deposition of materials on this seed can be performed using processes such as electroless plating, or selective CVD or ALD processes. FIG. 19, like FIG. 18, shows the electrical contact landing pad 25 as an anisotropic growth. Connections can be made to the electrical contact landing pads 25 using the process described above in reference to FIGS. 17A and 17B.

[0055] FIG. 20 illustrates a perspective view of another embodiment with conductive lines 50 having angled ends 22 with anisotropically grown electrical contact landing pads 25. The embodiment of FIG. 20 differs from the embodiments of FIGS. 15 through 18 in that the conductive lines 50 are not individually covered by a respective insulating material 51. In this embodiment, the photoresist material 33 forming the cutting mask 43 is not removed after the conductive lines 50 are cut, and the cutting mask 43 acts as an encapsulating growth-confining material during the growth of the electrical contact landing pads 25, so that growth occurs only at the exposed ends 22 of the conductive lines 50. As in other embodiments, an etch back may or may not be performed on to the photoresist material 33 at the angled ends 22 of the conductive lines 50. Extension electrical contact landing pads 25 are formed using the same growth techniques described above in reference to FIG. 16, including electroless deposition or selective CVD or ALD on polysilicon 35 and/or metal silicide 37, as examples. Connections can be made to the

electrical contact landing pads 25 using the process described above in reference to FIGS. 17A and 17B.

[0056] FIG. 21 illustrates an embodiment with metalized BCP cylinders 80 forming conductive lines 50 with extension contact landing pads 25. A self-assembled BCP material with BCP cylinders 80 (comprising, for example, PS) formed in a matrix phase material 82 (comprising, for example PMMA) is formed over a gate oxide material 31. The matrix phase material 82 has been selectively exposed to light at an angle across the extending direction of the BCP cylinders 80, and placed in a suitable developer to form an angled mask. The mask formed of the matrix phase material 82 is then used as a cutting mask to cut angled ends 22 in the BCP cylinders 80. Alternatively, the mask and cut could be performed using a conventional photoresist material 33 above the BCP material as a cutting mask 43 to cut the BCP cylinders 80 and the matrix phase material 82 at an angle (or to cut only the BCP cylinders 80 at an angle, if the matrix phase material 82 is removed prior to the mask and cut). An optional trim or etch-back may be applied to the matrix phase material 82 (or a cutting mask 43), pulling the material 82 back away from the exposed angled ends 22 of the BCP cylinders 80. The BCP cylinders may be stained with a metal, such as Pt, W, or other similar metal in order to functionalize them as a conductive line and to provide a seed material for selective deposition. To form extension electrical contact landing pads 25, a material at the exposed angled ends 22 of the BCP cylinders 80, such as the stained Pt, W, or other similar metal, acts as seed for growth. Selective deposition of materials on this seed can be performed using processes such as electroless plating or selective CVD or ALD processes. In this embodiment, the matrix phase material 82 confines nucleation and growth of the electrical contact landing pads to the angled ends 22. A photoresist material 33 could perform the same function as the matrix phase material 82 in this embodiment. The contact landing pads 25 may be isotropically (shown) or anisotropically grown.

[0057] The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described

herein. Modifications and substitutions for specific conditions and materials can be made. Accordingly, the embodiments are not considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating an integrated circuit structure on a support structure, the method comprising:

forming a plurality of linearly extending lines of at least one material;

cutting said material lines at an angle relative a linearly extending direction to form respective angled end faces at each of the material lines, said respective angled end faces being spaced in the linearly extending direction; and

forming an extension of each of said material lines at each respective angled end face.

2. The method of claim 1, wherein said material lines are parallel material lines.

3. The method of claim 2, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the parallel material lines simultaneously.

4. The method of claim 2, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

5. The method of claim 2, wherein said parallel material lines have a half pitch of 45nm or less.

6. The method of claim 2, wherein said parallel material lines have a half pitch of 20nm or less.

7. The method of claim 2, wherein said parallel material lines are formed using a self-assembled block copolymer mask.

8. The method of claim 2, further comprising covering said parallel material lines with an encapsulation insulating material prior to cutting said parallel material lines.

9. The method of claim 1, wherein said extensions are grown via selective deposition of a pad material at said respective angled end faces.

10. The method of claim 1, further comprising etching a conductive material provided below said parallel material lines and respective extensions using said parallel material lines and respective extensions as an etch mask to form conductive lines having respective electrical contact landing pad areas.

11. The method of claim 10, wherein said at least one material is one of a photoresist, a block copolymer, a silicon, a polysilicon, and a metal.

12. The method of claim 1, wherein said at least one material is a processed block copolymer and further comprising:

etching a mask material provided below said parallel material lines and respective extensions using said parallel material lines and respective extensions as an etch mask to form a mask pattern; and

etching a conductive material provided below said mask pattern using said mask pattern as a second etch mask to form conductive lines having respective electrical contact landing pads.

13. The method of claim 1, wherein said at least one material comprises at least one conductive material and said extension is an electrically conductive contact landing pad.

14. The method of claim 13, wherein said conductive material comprises at least one of a metal, a metal silicide, and a polysilicon.

15. The method of claim 13, wherein a conductive material exposed at said angled end faces is used as a seed to grow said electrically conductive contact landing pads via selective deposition of a conductive material at said angled end.

16. A method of fabricating an integrated circuit structure, the method comprising:

forming a plurality of parallel spaced linearly extending material lines;

etching said material lines at an angle relative to the extending direction of said material lines to form respective angled end faces at each of the parallel material lines, said respective angled end faces being spaced in the linearly extending direction;

forming a contact landing pad mask in contact with each of said angled end faces; and

using said material lines and said contact landing pad masks as an etch mask to etch a conductive material below said

material lines and contact landing pad masks to form a plurality of conductive lines with a half-pitch of 45nm or less having respective conductive contact landing pad areas.

17. The method of claim 16, further comprising covering said material lines with an encapsulation insulating material prior to etching said material lines.

18. The method of claim 16, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the material lines simultaneously.

19. The method of claim 16, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

20. The method of claim 16, wherein said conductive lines have a half pitch of 20nm or less.

21. The method of claim 16, wherein said material lines comprise one of a processed photoresist, a processed block copolymer, a silicon, a polysilicon, and a metal.

22. The method of claim 16, wherein said growth includes using at least a portion of the material line at the angled end face as a seed, and growing said contact landing pad masks from the seed via selective deposition of an extension material.

23. The method of claim 22, wherein said selective deposition is one of chemical vapor deposition, atomic layer deposition, electroless plating, or epitaxial growth.

24. The method of claim 16, wherein said electrical contact landing pad areas are sufficiently large to form an area for electrical

connection to the respective conductive lines, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pads.

25. A method of fabricating an integrated circuit structure, the method comprising:

forming a plurality of parallel spaced linearly extending conductive lines;

etching said conductive lines at an angle relative to the extending direction of said conductive lines to form respective angled end faces at each of said conductive lines, said angled end faces being spaced in the linearly extending direction; and

forming an electrical contact landing pad in contact with each of said respective angled end faces.

26. The method of claim 25, further comprising covering said conductive lines with an encapsulation insulating material prior to cutting said material lines.

27. The method of claim 25, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the conductive lines simultaneously.

28. The method of claim 25, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

29. The method of claim 25, wherein said conductive lines have a half pitch of 20nm or less.

30. The method of claim 25, wherein at least one layer of said conductive lines comprise one of a metal, a metal silicide, and a polysilicon.

31. The method of claim 25, wherein said electrical contact landing pads are formed by using at least a portion of the conductive line at the angled end face as a seed, and growing an electrical contact landing pad from the seed via selective deposition of a conductive material.

32. The method of claim 31, wherein said selective deposition is one of chemical vapor deposition, atomic layer deposition or electroless plating.

33. The method of claim 25, wherein said electrical contact landing pads are sufficiently large to form an area for electrical connection to the respective lines, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pads.

34. An integrated circuit comprising:

a plurality of parallel linearly extending electrically conductive lines formed as part of said integrated circuit, the conductive lines each having an angled end face at a different location along the linearly extending direction of said lines; and

a contact landing pad formed in electrical contact with each angled end face.

35. The integrated circuit of claim 34, wherein said conductive lines have a half-pitch of less than 45nm.

36. The integrated circuit of claim 35, wherein said conductive lines have a half-pitch of less than 20nm.

37. The integrated circuit of claim 34, wherein said angled end faces are at an angle of between 5 degrees and 30 degrees relative to the linearly extending direction.

38. The integrated circuit of claim 34, wherein said conductive lines comprise a poly-silicon material and a metal silicide material.

39. The integrated circuit of claim 34, wherein said conductive lines comprise a metal material.

40. The integrated circuit of claim 34, wherein said conductive lines form at least one of wordlines and bitlines of a memory device.