Abstract

METHOD FOR FORMING SELF-ALIGNED CHANNEL IMPLANTS USING A GATE POLY REVERSE MASK

A method for forming a CMOS transistor gate with a self-aligned channel implant. A semiconductor structure having a first active area is provided. A first insulating layer is formed on the semiconductor structure, and a second insulating layer is formed on the first insulating layer. The second insulating layer is patterned using a poly reverse mask and an etch selective to the first insulating layer to form a first channel implant opening, and the poly reverse mask is removed. A first channel implant mask is formed exposing the first channel implant opening. Impurity ions are implanted through the first channel implant opening to form a first threshhold adjust region and a first anti-punchthrough region. A gate layer is formed over the semiconductor structure, and the first gate layer is planarized to form a gate electrode. The second insulating layer is removed, and lightly doped source and drain regions, sidewall spacers and source and drain regions can be formed adjacent the gate electrode.

(FIGURE 1A IS SUGGESTED FOR PUBLICATION)