SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SEMICONDUCTOR PACKAGE HAVING BUILD-UP INTERCONNECT STRUCTURE OVER SEMICONDUCTOR DIE WITH DIFFERENT CTE INSULATING LAYERS

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming a semiconductor package having a build-up interconnect structure over a semiconductor die with different CTE insulating layers to create a gradient dielectric across the interconnect structure. The insulating layers are optimized for adhesion to the adjacent layer.

Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated

semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of functions such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The atomic structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or base current or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and

active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed calculations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each semiconductor die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual semiconductor die from the finished wafer and packaging the die to provide structural support and environmental isolation. The term "semiconductor die" as used herein refers to both the singular and plural form of the words, and accordingly, can refer to both a single semiconductor device and multiple semiconductor devices.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller semiconductor die size can be achieved by improvements in the front-end process resulting in semiconductor die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

A build-up interconnect structure is commonly formed over a semiconductor die for electrical interconnect. The

build-up interconnect structure contains one or more insulating layers and one or more conductive layers between the insulating layers. The insulating layers are subject to cracking, particularly during temperature cycling tests, due to coefficient of thermal expansion (CTE) mismatches between adjacent surfaces. The insulating layers often exhibit low tensile strength and elongation with surface wrinkle and weak adhesion to the adjacent layer due to a non-optimal curing profile. The defects in the insulating layers of the build-up interconnect structure lead to lower manufacturing yield and higher cost.

Summary of the Invention

A need exists for a build-up interconnect structure over a semiconductor die which is robust against cracking and exhibits good adhesion to the adjacent surface. Accordingly, in one embodiment, the present invention is a semiconductor device comprising a semiconductor die and encapsulant deposited over a first surface of the semiconductor die and around a peripheral region of the semiconductor die. A first insulating layer is formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die with multiple dwell curing cycles to enhance adhesion to the semiconductor die and encapsulant. A first conductive layer is formed over the first insulating layer. A second insulating layer is formed over the first insulating layer and first conductive layer with multiple dwell curing cycles to enhance adhesion to the first insulating layer and first conductive layer.

In another embodiment, the present invention is a

semiconductor device comprising a semiconductor die and encapsulant deposited over a first surface of the semiconductor die and around a peripheral region of the semiconductor die. A first insulating layer is formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die. A first conductive layer is formed over the first insulating layer. A second insulating layer is formed over the first insulating layer and first conductive layer, the second insulating layer including a CTE different than a CTE of the first insulating layer.

In another embodiment, the present invention is a semiconductor device comprising a semiconductor die and first insulating layer formed over the semiconductor die with multiple dwell curing cycles. A first conductive layer is formed over the first insulating layer. A second insulating layer is formed over the first insulating layer and first conductive layer.

In another embodiment, the present invention is a semiconductor device comprising a semiconductor die and first insulating layer formed over the semiconductor die. A first conductive layer is formed over the first insulating layer. A second insulating layer is formed over the first insulating layer and first conductive layer. The second insulating layer has a CTE different than a CTE of the first insulating layer.

Brief Description of the Drawings

FIG. 1 illustrates a PCB with different types of packages mounted to its surface;

FIGs. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGs. 3a-3c illustrate a semiconductor wafer with a

plurality of semiconductor die separated by a saw street;

FIGs. 4a-4i illustrate a process of forming an ECWLP package having an interconnect structure over a semiconductor die with different CTE insulating layers and each insulating layer optimized for adhesion to the adjacent layer;

FIG. 5 illustrates the ECWLP package having an interconnect structure for a semiconductor die with different CTE insulating layers and each insulating layer optimized for adhesion to the adjacent layer;

FIGs. 6a-6g illustrate another process of forming an ECWLP package having an interconnect structure over a die with different CTE insulating layers and each insulating layer optimized for adhesion to the adjacent layer; and

FIG. 7 illustrates the ECWLP package having an interconnect structure for a semiconductor die with different CTE insulating layers and each insulating layer optimized for adhesion to the adjacent layer.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using

two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices, transforming the semiconductor material into an insulator, conductor, or dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition can involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and

electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

The layers can be patterned using photolithography, which involves the deposition of light sensitive material, e.g., photoresist, over the layer to be patterned. A pattern is transferred from a photomask to the photoresist using light. In one embodiment, the portion of the photoresist pattern subjected to light is removed using a solvent, exposing portions of the underlying layer to be patterned. In another embodiment, the portion of the photoresist pattern not subjected to light, the negative photoresist, is removed using a solvent, exposing portions of the underlying layer to be patterned. The remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive components. Planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface. Planarization involves polishing the surface of the wafer with a polishing pad. An abrasive material and corrosive chemical are added to the surface of the wafer during polishing. The combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.

Back-end manufacturing refers to cutting or

singulating the finished wafer into the individual die and then packaging the die for structural support and environmental isolation. To singulate the semiconductor die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual semiconductor die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. 1 illustrates electronic device 50 having a chip carrier substrate or printed circuit board (PCB) 52 with a plurality of semiconductor packages mounted on its surface. Electronic device 50 can have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. 1 for purposes of illustration.

Electronic device 50 can be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device 50 can be a subcomponent of a larger system. For example, electronic device 50 can be part of a cellular phone, personal digital assistant (PDA), digital video camera (DVC), or other electronic communication device. Alternatively, electronic device 50 can

be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASIC), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components. Miniaturization and weight reduction are essential for these products to be accepted by the market. The distance between semiconductor devices must be decreased to achieve higher density.

In FIG. 1, PCB 52 provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces 54 are formed over a surface or within layers of PCB 52 using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces 54 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 54 also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including bond wire package 56 and flipchip 58, are shown on PCB 52. Additionally, several types of second level packaging, including ball grid array (BGA) 60,

bump chip carrier (BCC) 62, dual in-line package (DIP) 64, land grid array (LGA) 66, multi-chip module (MCM) 68, quad flat non-leaded package (QFN) 70, and quad flat package 72, are shown mounted on PCB 52. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB 52. In some embodiments, electronic device 50 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using cheaper components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGs. 2a-2c show exemplary semiconductor packages. FIG. 2a illustrates further detail of DIP 64 mounted on PCB 52. Semiconductor die 74 includes an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active region of semiconductor die 74. Contact pads 76 are one or more layers of conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within

semiconductor die 74. During assembly of DIP 64, semiconductor die 74 is mounted to an intermediate carrier 78 using a gold-silicon eutectic layer or adhesive material such as thermal epoxy or epoxy resin. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads 80 and bond wires 82 provide electrical interconnect between semiconductor die 74 and PCB 52. Encapsulant 84 is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating semiconductor die 74 or bond wires 82.

FIG. 2b illustrates further detail of BCC 62 mounted on PCB 52. Semiconductor die 88 is mounted over carrier 90 using an underfill or epoxy-resin adhesive material 92. Bond wires 94 provide first level packaging interconnect between contact pads 96 and 98. Molding compound or encapsulant 100 is deposited over semiconductor die 88 and bond wires 94 to provide physical support and electrical isolation for the device. Contact pads 102 are formed over a surface of PCB 52 using a suitable metal deposition process such as electrolytic plating or electroless plating to prevent oxidation. Contact pads 102 are electrically connected to one or more conductive signal traces 54 in PCB 52. Bumps 104 are formed between contact pads 98 of BCC 62 and contact pads 102 of PCB 52.

In FIG. 2c, semiconductor die 58 is mounted face down to intermediate carrier 106 with a flipchip style first level packaging. Active region 108 of semiconductor die 58 contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active

region 108. Semiconductor die 58 is electrically and mechanically connected to carrier 106 through bumps 110.

BGA 60 is electrically and mechanically connected to PCB 52 with a BGA style second level packaging using bumps 112. Semiconductor die 58 is electrically connected to conductive signal traces 54 in PCB 52 through bumps 110, signal lines 114, and bumps 112. A molding compound or encapsulant 116 is deposited over semiconductor die 58 and carrier 106 to provide physical support and electrical isolation for the device. The flipchip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die 58 can be mechanically and electrically connected directly to PCB 52 using flipchip style first level packaging without intermediate carrier 106.

FIG. 3a shows a semiconductor wafer 120 with a base substrate material 122, such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support. A plurality of semiconductor die or components 124 is formed on wafer 120 separated by a non-active, inter-die wafer area or saw street 126 as described above. Saw street 126 provides cutting areas to singulate semiconductor wafer 120 into individual semiconductor die 124.

FIG. 3b shows a cross-sectional view of a portion of semiconductor wafer 120. Each semiconductor die 124 has a back surface 128 and active surface region 130 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical

design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active region 130 to implement analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die 124 may also contain integrated passive devices (IPDs), such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 124 is a flipchip type die.

An electrically conductive layer 132 is formed over active surface 130 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 132 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 132 operates as contact pads for the circuits on active surface 130. Contact pads 132 can be disposed side-by-side a first distance from the edge of semiconductor die 124. Alternatively, contact pads 132 can be offset in multiple rows such that a first row of contact pads is disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row is disposed a second distance from the edge of the die.

An insulating or passivation layer 134 is formed over active surface 130 and conductive layers 132 for electrical isolation using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer 134 contains one or more layers of solder resist, silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), or other material having similar insulating and structural properties. A portion of insulating layer 134 can be removed by an etching

process through a photoresist layer to expose conductive layer 132.

In FIG. 3c, semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 136 into individual semiconductor die 124.

FIGs. 4a-4i illustrate, in relation to FIGs. 1 and 2a-2c, a process of forming an embedded chip wafer level ball grid array (ECWLP) semiconductor package having a build-up interconnect structure over a semiconductor die with different CTE insulating layers and each insulating layer optimized for adhesion to the adjacent layer. FIG. 4a shows a substrate or carrier 140 containing temporary or sacrificial base material such as silicon, polymer, beryllium oxide, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 142 is formed over carrier 140 as a temporary adhesive bonding film or etch-stop layer.

Semiconductor die 124 from FIGs. 3a-3c is aligned with and mounted to carrier 140 with insulating layer 134 oriented toward the carrier. FIG. 4b shows semiconductor die 124 mounted to carrier 140 with insulating layer 134 bonded to interface layer 142.

In FIG. 4c, an encapsulant or molding compound 144 is deposited over and around semiconductor die 124 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 144 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 144 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 4d, a portion of back surface 146 of

encapsulant 144 is removed by grinder 148 in an optional back grinding operation to planarize the encapsulant and expose back surface 128 of semiconductor die 124. The grinding operation reduces the package profile.

Continuing from FIG. 4c, carrier 140 and interface layer 142 are removed by chemical etching, mechanical peeling, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose contact pads 132, insulating layer 134, and encapsulant 144, as shown in FIG. 4e.

In FIG. 4f, an insulating or dielectric layer 150 is formed over insulating layer 134, encapsulant 144, and the exposed conductive layer 132 using lamination, screen printing, slit coating, spin coating, or spray coating. The insulating layer 150 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric materials, such as low temperature cure negative tone polyimide (PI), positive tone polybenzoxazoles (PBO), non-photosensitive polymer dielectric with or without filler, or other suitable dielectric material. In particular, insulating layer 150 is patterned and cured for optimal adhesion to conductive layer 132, insulating layer 134, and encapsulant 144 of semiconductor die 124. The curing process for insulating layer 150 involves a multi-step dwell profile, e.g., with at least three different dwell steps, to enhance mechanical and adhesion properties to conductive layer 132, insulating layer 134 and encapsulant 144 under pressure cooker test (PCT), e.g., >400 kg/cm2 for 0 to 200 hours unbiased humidity accelerated stress testing (uHAST), without introducing surface wrinkle after curing. The multi-step dwell profile includes a first dwell step with a temperature less than 100°C, e.g., 70-90°C, for 30-90 minutes to remove solvent and moisture, second dwell step with a temperature between 120-150°C for 30-60

minutes, and third dwell step with a temperature between 180-240°C for 60-180 minutes.

The insulating layer 150 has a tensile strength >100MPa, high elongation >20%, and modulus <3.0 Gpa under 25°C. In particular, a CTE for insulating layer 150 is selected in the range of 30-90 ppm. A portion of insulating layer 150 is removed by an etching process, for example UV exposure followed by wet chemical developing, or laser (UV or excimer laser) via drilling only, to expose conductive layer 132.

In FIG. 4g, an electrically conductive layer or redistribution layer (RDL) 152 formed over insulating layer 150 and conductive layer 132 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 152 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, titanium (Ti), tungsten (W), TiW/Cu, Ti/Cu, or other suitable electrically conductive material. One portion of conductive layer 152 is electrically connected to conductive layer 132 of semiconductor die 124. Other portions of conductive layer 152 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

In FIG. 4h, an insulating or dielectric layer 154 is formed over insulating layer 150 and conductive layer 152 using lamination, screen printing, slit coating, spin coating, or spray coating. The insulating layer 154 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric materials, such as low temperature cure negative tone PI, positive tone PBO, non-photosensitive polymer dielectric with or without filler, or other suitable dielectric material. In particular, insulating layer 154 is patterned and cured for optimal adhesion to insulating layer 150 and conductive layer

152. The curing process for insulating layer 154 involves a multi-step dwell profile, e.g., with at least three different dwell steps, to enhance mechanical and adhesion properties to insulating layer 150 and conductive layer 152 under PCT, e.g., >400 kg/cm2 for 0 to 500 hours uHAST, without introducing surface wrinkle after curing. The multi-step dwell profile includes a first dwell step with a temperature less than 100°C, e.g., 70-90°C, for 30-90 minutes to remove solvent and moisture, second dwell step with a temperature between 120-150°C for 30-60 minutes, and third dwell step with a temperature between 180-240°C for 60-180 minutes.

The insulating layer 154 has a tensile strength >100 MPa, high elongation >20%, and modulus <3.0 Gpa under 25°C. In particular, a CTE for insulating layer 154 is selected to be different from the CTE of insulating layer 150. For example, the CTE of insulating layer 154 is selected in the range of 90-150 ppm. Alternatively, the CTE of insulating layer 150 is selected to be 90-150 ppm and the CTE of insulating layer 154 is selected to be 30-90 ppm. In one embodiment, the CTE of insulating layer 150 is selected to be 73 ppm, and the CTE of insulating layer 154 is selected to be 126 ppm. A portion of insulating layer 154 is removed by an etching process, for example UV exposure followed by wet chemical developing, or laser (UV or excimer laser) via drilling only, to expose conductive layer 152.

The different CTEs of insulating layers 150 and 154 create a dielectric gradient across interconnect structure 158. The dielectric gradient reduces stress induced by insulating layers 150 and 154 during temperature cycling, e.g., during reliability testing, especially due to the free boundary surface of insulating layer 154 and CTE mismatch between insulating

layer 150 and encapsulant 144 and semiconductor die 124.

In another embodiment, insulating layers 150 and 154 have similar CTE, e.g., +/- 30ppm/°C. The insulating layer 150 has good adhesion to conductive layer 132, insulating layer 134, and encapsulant 144 during the build-up process and after curing, as well as good mechanical properties of tensile strength > 100 MPa and high elongation > 20%. The insulating layer 154 has good adhesion to insulting layer 150 and conductive layer 152, as well as good mechanical properties of tensile strength > 100 MPa and high elongation (> 20%). In addition, insulating layer 154 has a dense material structure to block or delay the moisture penetration into the film, and therefore into insulating layer 150, 150/144 interface, and 150/134 interface. The dense state of insulating layer 154 also improves reliability in uHAST and PCT and prevents interface delamination at the 150/144 interface and 150/134 interface.

In another embodiment, insulating layers 150 and 154 have good adhesion to conductive layer 132, insulating layer 134, and encapsulant 144, as well as good mechanical properties of tensile strength > 100 MPa and high elongation > 20%. The insulating layer 150 is cured at higher temperature for example, 240°C +/- 10°C, while insulating layer 154 is cured at lower temperature, e.g., 215°C +/- 10°C. The different curing temperatures lower contact resistance between conductive layers 132 and 152, and package temperature cycling test reliability performance due to different residue stress, warpage behavior, out-gassing control in the seed layer PVD for conductive layer 152, and enhance interface between 150 and 154 under different temperatures.

In FIG. 4i, an electrically conductive bump material is deposited over conductive layer 152 using an evaporation,

electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 152 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 156. In some applications, bumps 156 are reflowed a second time to improve electrical contact to conductive layer 152. Bumps 156 can also be compression bonded to conductive layer 152. Bumps 156 represent one type of interconnect structure that can be formed over conductive layer 152. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect.

The insulating layers 150 and 154, conductive layer 152, and bumps 156 constitute a build-up interconnect structure 158 formed over active surface 130 of semiconductor die 124 and encapsulant 144. Semiconductor die 124 and build-up interconnect structure 158 represent an ECWLP in a reconstituted wafer form. The reconstituted wafer is singulated through build-up interconnect structure 158 and encapsulant 144 using a saw blade or laser cutting tool 160 into individual ECWLP packages 162 containing semiconductor die 124.

FIG. 5 shows ECWLP package 162 with semiconductor die 124 electrically connected to conductive layer 152 and bumps 156 for external interconnect to other semiconductor devices. In one embodiment, the CTE of insulating layer 150 is selected in the range of 30-90 ppm, and the CTE of insulating layer 154 is selected in the range of 90-150 ppm. Alternatively, the CTE of insulating layer 150 is selected to be 90-150 ppm and the CTE of

insulating layer 154 is selected to be 30-90 ppm. The different CTEs of insulating layers 150 and 154 create a dielectric gradient across interconnect structure 158. The dielectric gradient reduces stress induced by insulating layers 150 and 154 during temperature cycling, e.g., during reliability testing, especially due to the free boundary surface of insulating layer 154 and CTE mismatch between insulating layer 150 and encapsulant 144 and semiconductor die 124.

The insulating layer 150 is patterned and cured for optimal adhesion to conductive layer 132, insulating layer 134 and encapsulant 144 of semiconductor die 124. The curing process for insulating layer 150 involves a multi-step dwell profile to enhance mechanical and adhesion properties to conductive layer 132, insulating layer 134, and encapsulant 144, without introducing surface wrinkle. The insulating layer 154 is patterned and cured for optimal adhesion to insulating layer 150 and conductive layer 152. The curing process for insulating layer 154 involves a multi-step dwell profile to enhance mechanical and adhesion properties to insulating layer 150 and conductive layer 152, without introducing surface wrinkle.

FIGs. 6a-6g illustrate, in relation to FIGs. 1 and 2a-2c, another process of forming an ECWLP semiconductor package having a build-up interconnect structure over a semiconductor die with different CTE insulating layers and each insulating layer optimized for adhesion to the adjacent layer. Continuing from FIG. 4e, an insulating or dielectric layer 170 is formed over insulating layer 134, encapsulant 144, and the exposed conductive layer 132 using lamination, screen printing, slit coating, spin coating, or spray coating. The insulating layer 170 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric materials, such as low

temperature cure negative tone PI, positive tone PBO, non-photosensitive polymer dielectric with or without filler, or other suitable dielectric material. In particular, insulating layer 170 is patterned and cured for optimal adhesion to conductive layer 132, insulating layer 134, and encapsulant 144 of semiconductor die 124. The curing process for insulating layer 170 involves a multi-step dwell profile, e.g., with at least three different dwell steps, to enhance mechanical and adhesion properties to conductive layer 132, insulating layer 134 and encapsulant 144 under PCT, e.g., >400 kg/cm2 for 0 to 200 hours uHAST, without introducing surface wrinkle after curing. The multi-step dwell profile includes a first dwell step with a temperature less than 100°C, e.g., 70-90°C, for 30-90 minutes to remove solvent and moisture, second dwell step with a temperature between 120-150°C for 30-60 minutes, and third dwell step with a temperature between 180-240°C for 60-180 minutes. The insulating layer 170 has a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C. In particular, a CTE for insulating layer 170 is selected in the range of 30-90 ppm. A portion of insulating layer 170 is removed by an etching process, for example UV exposure followed by wet chemical developing, or laser (UV or excimer laser) via drilling only, to expose conductive layer 132.

In FIG. 6b, an electrically conductive layer or RDL 172 formed over insulating layer 170 and conductive layer 132 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 172 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, TiW/Cu, Ti/Cu, or other suitable electrically conductive material. One portion of conductive layer 172 is electrically connected to conductive layer 132 of semiconductor

die 124. Other portions of conductive layer 172 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

In FIG. 6c, an insulating or dielectric layer 174 is formed over insulating layer 170 and conductive layer 172 using lamination, screen printing, slit coating, spin coating, or spray coating. The insulating layer 174 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric materials, such as low temperature cure negative tone PI, positive tone PBO, non-photosensitive polymer dielectric with or without filler, or other suitable dielectric material. In particular, insulating layer 174 is patterned and cured for optimal adhesion to insulating layer 170 and conductive layer 172. The curing process for insulating layer 174 involves a multi-step dwell profile, e.g., with at least three different dwell steps, to enhance mechanical and adhesion properties to insulating layer 170 and conductive layer 172 under PCT, e.g., >400 kg/cm2 for 0 to 500 hours uHAST, without introducing surface wrinkle after curing. The multi-step dwell profile includes a first dwell step with a temperature less than 100°C, e.g., 70-90°C, for 30-90 minutes to remove solvent and moisture, second dwell step with a temperature between 120-150°C for 30-60 minutes, and third dwell step with a temperature between 180-240°C for 60-180 minutes.

The insulating layer 174 has a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C. In particular, a CTE for insulating layer 174 is selected to be different from the CTE of insulating layer 170. For example, the CTE of insulating layer 174 is selected in the range of 90-110 ppm. Alternatively, the CTE of insulating layer 170 is selected to be 90-110 ppm and the CTE of insulating layer 174 is

selected to be 30-90 ppm. In one embodiment, the CTE of insulating layer 170 is selected to be 73 ppm, and the CTE of insulating layer 174 is selected to be 106 ppm. A portion of insulating layer 174 is removed by an etching process, for example UV exposure followed by wet chemical developing, or laser (UV or excimer laser) via drilling only, to expose conductive layer 172.

Alternatively, insulating layer 174 has a dense structure after the multi-step dwell curing profile to block or delay the moisture penetration into the film, and therefore into insulating layer 170, 170/144 interface, and 170/134 interface.

In FIG. 6d, an electrically conductive layer or RDL 176 formed over insulating layer 174 and conductive layer 172 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 176 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, TiW/Cu, Ti/ Cu, or other suitable electrically conductive material. One portion of conductive layer 176 is electrically connected to conductive layer 172. Other portions of conductive layer 176 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

In FIG. 6e, an insulating or dielectric layer 178 is formed over insulating layer 174 and conductive layer 176 using lamination, screen printing, slit coating, spin coating, or spray coating. The insulating layer 178 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric materials, such as low temperature cure negative tone PI, positive tone PBO, non-photosensitive polymer dielectric with or without filler, or other suitable dielectric material. In particular, insulating layer 178 is patterned and cured for

optimal adhesion to insulating layer 174 and conductive layer 176. The curing process for insulating layer 178 involves a multi-step dwell profile, e.g., with at least three different dwell steps, to enhance mechanical and adhesion properties to insulating layer 174 and conductive layer 176 under PCT, e.g., >400 kg/cm2 for 0 to 500 hours uHAST, without introducing surface wrinkle after curing. The multi-step dwell profile includes a first dwell step with a temperature less than 100°C, e.g., 70-90°C, for 30-90 minutes to remove solvent and moisture, second dwell step with a temperature between 120-150°C for 30-60 minutes, and third dwell step with a temperature between 180-240°C for 60-180 minutes.

The insulating layer 178 has a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C. In particular, a CTE for insulating layer 178 is selected to be different from the CTE of insulating layers 170 and 174. For example, the CTE of insulating layer 178 is selected in the range of 110-150 ppm. Alternatively, the CTE of insulating layer 170 is selected to be 110-150 ppm, the CTE of insulating layer 174 is selected to be 90-110 ppm, and the CTE of insulating layer 178 is selected to be 30-90 ppm. In one embodiment, the CTE of insulating layer 170 is selected to be 73 ppm, the CTE of insulating layer 174 is selected to be 106 ppm, and the CTE of insulating layer 178 is selected to be 126 ppm. A portion of insulating layer 178 is removed by an etching process, for example UV exposure followed by wet chemical developing, or laser (UV or excimer laser) via drilling only, to expose conductive layer 176.

Alternatively, insulating layer 178 has a dense structure after the multi-step dwell curing profile to block or delay the moisture penetration into the film, and therefore into

insulating layer 178 and 178/174 interface.

The different CTEs of insulating layers 170, 174, and 178 create a dielectric gradient across interconnect structure 182. The dielectric gradient reduces stress induced by insulating layers 170, 174, and 178 during temperature cycling.

In FIG. 6f, an electrically conductive bump material is deposited over conductive layer 176 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 176 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 180. In some applications, bumps 180 are reflowed a second time to improve electrical contact to conductive layer 176. Bumps 180 can also be compression bonded to conductive layer 176. Bumps 180 represent one type of interconnect structure that can be formed over conductive layer 176. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect.

The insulating layers 170, 174, and 178, conductive layer 172 and 176, and bumps 180 constitute a build-up interconnect structure 182 formed over active surface 130 of semiconductor die 124 and encapsulant 144. Semiconductor die 124 and build-up interconnect structure 182 represent an ECWLP in a reconstituted wafer form. The reconstituted wafer is singulated through build-up interconnect structure 182 and encapsulant 144 using a saw blade or laser cutting tool 183 into individual ECWLP packages 184 containing semiconductor die 124.

FIG. 7 shows ECWLP package 184 with semiconductor die 124 electrically connected to conductive layers 172 and 176 and bumps 180 for external interconnect to other semiconductor devices. The different CTEs of insulating layers 170, 174, and 178 create a dielectric gradient across interconnect structure 182. The dielectric gradient reduces stress induced by insulating layers 170, 174, and 178 during temperature cycling.

The insulating layer 170 is patterned and cured for optimal adhesion to conductive layer 132, insulating layer 134 and encapsulant 144 of semiconductor die 124. The curing process for insulating layer 170 involves a multi-step dwell profile to enhance mechanical and adhesion properties to conductive layer 132, insulating layer 134, and encapsulant 144, without introducing surface wrinkle. The insulating layer 174 is patterned and cured for optimal adhesion to insulating layer 170 and conductive layer 172. The insulating layer 178 has a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

Alternatively, insulating layer 170 has a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C. The insulating layer 178 has a dense structure after the multi-step dwell curing profile to block moisture in the PCT. The insulating layer 174 can have properties of either insulating layer 170 or insulating layer 178.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die including a plurality of contact pads;

a first insulating layer formed in contact with an active surface of the semiconductor die;

an encapsulant deposited over a second surface of the semiconductor die opposite the active surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and first insulating layer, wherein the interconnect structure includes,

(a) a second insulating layer formed in direct contact with the encapsulant and first insulating layer, wherein a coefficient of thermal expansion (CTE) of the second insulating layer is within a first range of 30-90 parts per million (ppm),

(b) a first conductive layer formed over the second insulating layer and the plurality of contact pads,

(c) a third insulating layer formed in direct contact with the second insulating layer and first conductive layer, wherein a CTE of the third insulating layer is within a second range of 90-110 ppm,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a fourth insulating layer formed in direct contact with the third insulating layer and second conductive layer, wherein a CTE of the fourth insulating layer is within a third range of 110-150 ppm.

2. The semiconductor device of claim 1, wherein the second insulating layer, third insulating layer, and fourth insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

3. The semiconductor device of claim 1, further including a bump formed over the second conductive layer.

4. The semiconductor device of claim 1, wherein the second insulating layer, third insulating layer, and fourth insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

5. The semiconductor device of claim 1, wherein the CTE of the second insulating layer is 73 ppm, the CTE of the third insulating layer is 106 ppm, and the CTE of the fourth insulating layer is 126 ppm.

6. A semiconductor device, comprising:

a semiconductor die including a plurality of contact pads;

a first insulating layer formed in contact with an active surface of the semiconductor die;

an encapsulant deposited over a second surface of the semiconductor die opposite the active surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and first insulating layer, wherein the interconnect structure includes,

(a) a second insulating layer formed in direct contact with the encapsulant and first insulating layer, wherein

a coefficient of thermal expansion (CTE) of the second insulating layer is within a first range of 110–150 parts per million (ppm),

(b) a first conductive layer formed over the second insulating layer and the plurality of contact pads,

(c) a third insulating layer formed in direct contact with the second insulating layer and first conductive layer, wherein a CTE of the third insulating layer is within a second range of 90–110 ppm,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a fourth insulating layer formed in direct contact with the third insulating layer and second conductive layer, wherein a CTE of the fourth insulating layer is within a third range of 30–90 ppm.

7. The semiconductor device of claim 6, wherein the second insulating layer, third insulating layer, and fourth insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

8. The semiconductor device of claim 6, further including a bump formed over the second conductive layer.

9. The semiconductor device of claim 6, wherein the second insulating layer, third insulating layer, and fourth insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

10. The semiconductor device of claim 6, wherein the CTE of the second insulating layer is 73 ppm, the CTE of the third

insulating layer is 106 ppm, and the CTE of the fourth insulating layer is 126 ppm.

11. A semiconductor device, comprising:

a semiconductor die including a plurality of contact pads;

a first insulating layer formed in contact with a first surface of the semiconductor die;

an encapsulant deposited over a second surface of the semiconductor die opposite the first surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and first insulating layer, wherein the interconnect structure includes,

(a) a second insulating layer formed in direct contact with the encapsulant and the first insulating layer, wherein a coefficient of thermal expansion (CTE) of the second insulating layer is within a first range,

(b) a first conductive layer formed over the second insulating layer and the plurality of contact pads,

(c) a third insulating layer formed in direct contact with the second insulating layer and first conductive layer, wherein a CTE of the third insulating layer is within a second range overlapping in part and different in part with respect to the first range,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a fourth insulating layer formed in direct contact with the third insulating layer and second conductive layer, wherein a CTE of the fourth insulating layer is within a third range overlapping in part and different in part with respect to the second range.

12. The semiconductor device of claim 11, wherein the first range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

13. The semiconductor device of claim 11, wherein the second range is selected from the group consisting of 30-90 parts per million (ppm) and 90-110 ppm.

14. The semiconductor device of claim 11, wherein the third range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

15. The semiconductor device of claim 11, further including a bump formed over the second conductive layer.

16. The semiconductor device of claim 11, wherein the second insulating layer and third insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

17. The semiconductor device of claim 11, wherein the second insulating layer and third insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

18. A semiconductor device, comprising:

a semiconductor die including a plurality of contact pads;

an encapsulant deposited over the semiconductor die opposite the first surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and the semiconductor die, wherein the interconnect structure includes,

(a) a first insulating layer formed over the encapsulant and semiconductor die, wherein a coefficient of thermal expansion (CTE) of the first insulating layer is within a first range,

(b) a first conductive layer formed over the first insulating layer and the plurality of contact pads,

(c) a second insulating layer formed in direct contact with the first insulating layer and first conductive layer, wherein a CTE of the second insulating layer is within a second range overlapping in part and different in part with respect to the first range,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a third insulating layer formed in direct contact with the second insulating layer and second conductive layer, wherein a CTE of the third insulating layer is within a third range overlapping in part and different in part with respect to the second range.

19. The semiconductor device of claim 18, wherein the first range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

20. The semiconductor device of claim 18, wherein the second range is selected from the group consisting of 30-90 parts per million (ppm) and 90-110 ppm.

21. The semiconductor device of claim 18, wherein the third range is selected from the group consisting of 30–90 parts per million (ppm), 90–110 ppm, and 110–150 ppm.

22. The semiconductor device of claim 18, further including a bump formed over the second conductive layer.

23. The semiconductor device of claim 18, wherein the first insulating layer and second insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

24. The semiconductor device of claim 18, wherein the first insulating layer and second insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.