SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application claims priority to Korean Patent Application No. 10-2022-0081410, filed on 1 July 2022, in the Korean Intellectual Property Office (KIPO), the contents of which are incorporated by reference herein in their entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to semiconductor devices.

BACKGROUND

[0003] MBC-FETs including a plurality of vertically stacked channels have been developed. The MBC-FETs may be formed to have target electrical characteristics.

SUMMARY

[0004] The present disclosure relates to semiconductor devices such as, e.g., semiconductor devices including multi-bridge channel field effect transistors (MBC-FETs) and a having target electrical characteristics. In some implementations, the target electrical characteristics can be achieved by designing impurity region structures of a transistor to have volumes that depend on the width of a tapered fin structure disposed on a side or sides of a gate structure. In some implementations, the transistor can be a medium-frequency transistor that has both electrical characteristics of a high-frequency transistor, e.g., operating in the MHz frequency range, and electrical characteristics of a low-frequency transistor, e.g., operating in the order of Hz, as a result of the transistor's different target electrical characteristics such as, e.g., a size of the source and/or drain regions, on the sides of the gate structure. Thus, in some cases,

the transistor can serve as a high-power/low-power buffer based on the different source and drain characteristics.

[0005] In general, innovative aspects of the subject matter described in this specification can be embodied in a semiconductor device that includes a plurality of first channel structures on a substrate, a plurality of second channel structures on the substrate, a first impurity region structure between the first channel structures, a second impurity region structure between second channel structures, a third impurity region structure between the first and second channel structures, and a plurality of gate structures disposed between the first to third impurity region structures, respectively. The first channel structures may be spaced apart from each other in a first direction parallel to a surface of the substrate. Each of the first channel structure may have a first width in a second direction parallel to the surface of the substrate and perpendicular to the first direction, and may include silicon patterns spaced apart from each other in a vertical direction. The second channel structures may be spaced apart from each other in the first direction. Each of the second channel structure may have a second width in the second direction less than the first width, and may include silicon patterns spaced apart from each other in the vertical direction. The first impurity region structure may connect sidewalls of adjacent first channel structures, and may have a first volume. The second impurity region structure may connect sidewalls of adjacent second channel structures, and may have a second volume smaller than the first volume. The third impurity region structure may connect sidewalls of adjacent first and second channel structures, and may have a third volume smaller than the first volume and greater than the second volume. Each of the gate structure may cover one of the first and second channel structures, and may extend in the second direction.

[0006] In general, in another aspect, the subject matter of the present disclosure can be embodied in a semiconductor device that includes: a first transistor on a substrate, a second

transistor on the substrate, and a buffer transistor on the substrate. The first transistor may include a first channel structure having a first width in a second direction parallel to a surface of the substrate, a first gate structure extending in the second direction and parallel to the surface of the substrate to cover the first channel structure, and a first impurity region structure on both sides of the first gate structure in a first direction perpendicular to the second direction. The first impurity region structure may be connected to the first channel structure, and may have a first volume. The second transistor may include a second channel structure having a second width in the second direction less than the first width, a second gate structure extending in the second direction to cover the second channel structure, and a second impurity region structure on both sides of the second gate structure in the first direction. The second impurity region structure may be connected to the second channel structure, and may have a second volume smaller than the first volume. The buffer transistor may include a third channel structure between the first and second transistors, a third gate structure extending in the second direction to cover the third channel structure, a third impurity region structure on a side of the third gate structure in the first direction to be connected with the third channel structure, and a fourth impurity region structure on the other side of the third gate structure to be connected with the third channel structure. The fourth impurity region structure may have a volume different from a volume of the third impurity region structure.

[0007] In general, in another aspect, the subject matter of the present disclosure can be embodied in a semiconductor device including: a first transistor and a buffer transistor. The first transistor may include a first channel structure on a substrate, a first gate structure extending in a second direction parallel to the surface of the substrate to cover the first channel structure, and a first impurity region structure on both sides of the first gate structure in a first direction perpendicular to the second direction. The first impurity region structure

may be connected to the first channel structure, and may have a first volume. The buffer transistor may include a second channel structure on the substrate, a second gate structure extending in the second direction to cover the second channel structure, and a second impurity region on a side of the second gate structure in the first direction to be connected with the second channel structure. The second impurity region structure may have a second volume different from the first volume of the first impurity region structure. The first impurity region structure may contact on the other side of the second gate structure in the first direction.

[0008] In some implementations, the semiconductor device may include the buffer transistor including impurity region structures having different volumes. The buffer transistor may be provided as a transistor that operates with a performance of a middle power that of the first transistor having a high power characteristic and the second transistor having a low power characteristic.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Example implementations will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. FIGS. 1 to 26 represent non-limiting examples as described herein.

[0010] FIGS. 1 and 2 are a plan view and a cross-sectional view illustrating examples of semiconductor devices;

[0011] FIGS. 3 and 4 are a plan view and a perspective view illustrating an example of an active structure of the semiconductor device;

[0012] FIGS. 5A, 5B, 6 and 7 are perspective views illustrating examples of transistors included in the semiconductor device, respectively;

[0013] FIGS. 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21 and 22 are plan views, cross-sectional views and perspective views illustrating a method of manufacturing an

example of a semiconductor device;

[0014] FIGS. 23, 24 and 25 are plan views illustrating examples of semiconductor devices, respectively; and

[0015] FIG. 26 is a plan view illustrating an example of a semiconductor device.

DETAILED DESCRIPTION

[0016] Hereinafter, a direction parallel to a surface of a substrate is referred to as a first direction, and a direction parallel to the surface of the substrate and perpendicular to the first direction is referred to as a second direction. In addition, a direction perpendicular to the surface of the substrate is referred to as a vertical direction.

[0017] FIGS. 1 and 2 are a plan view and a cross-sectional view illustrating an example of a semiconductor device. FIGS. 3 and 4 are a plan view and a perspective view illustrating an example of an active structure of the semiconductor device. FIGS. 5A to 7 are perspective views illustrating examples of transistors included in the semiconductor device.

[0018] FIG. 2 is a cross-sectional view taken along line A-A' of FIG. 1. FIGS. 5A and 5B show first and second buffer multi-bridge channel transistors, respectively. FIG. 6 shows a first multi-bridge channel transistor, and FIG. 7 shows a second multi-bridge channel transistor.

[0019] Referring to FIGS. 1 to 7, the semiconductor device may include first multi-bridge channel transistors TR1, second multi-bridge channel transistors TR2, and buffer multi-bridge channel transistors TR3a and TR3b formed in an active structure 172.

[0020] The active structure 172 may be formed on a substrate 100 of an active region. The active structure 172 may extend in the first direction. The active structure 172 may include a single crystal semiconductor material.

[0021] The active structure 172 includes channel structures 170a and 170b spaced apart from each other and impurity region structures 150a, 150b, and 150c between the channel

structures 170a and 170b. The impurity region structures 150a, 150b, and 150c may contact both sidewalls of the channel structures 170a and 170b in the first direction, and may be connected with adjacent channel structures 170a and 170b. In the active structure, the channel structures 170a and 170b and the impurity region structures 150a, 150b, and 150c may be alternately and repeatedly arranged in the first direction.

[0022] The active structure 172A may include plurality of channel structures 170a and 170b having different widths in the second direction. In some implementations, the channel structures 170a and 170b may include first channel structures 170a having a first width W1 in the second direction and second channel structures 170b having a second width W2 less than the first width W1 in the second direction. In a plan view, the first channel structures 170a may be spaced apart from each other in the first direction, and may be arranged in parallel. In the plan view, the second channel structures 170b may be spaced apart from each other in the first direction and may be arranged in parallel. An interval (i.e., spacing) between the first channel structures 170a in the first direction may be substantially the same. In addition, intervals between the second channel structures 170b in the first direction may be substantially the same.

[0023] In some implementations, the channel structures 170a and 170b may have the same width in the first direction.

[0024] Referring to FIGS. 2 to 4, the channel structures 170a and 170b may have a stacked structure in which first silicon patterns 104a are vertically spaced apart from each other. A gap may be formed between the silicon patterns 104a. The first silicon pattern 104a may include single crystal silicon.

[0025] In the active structure 172, the impurity region structures 150a, 150b, and 150c may include a first impurity region structure 150a, a second impurity region structure 150b and a third impurity region structure 150c. The first impurity region structure 150a may be

disposed between the first channel structures 170a, and the second impurity region structure 150b may be disposed between the second channel structures 170b. The third impurity region structure 150c may be disposed between the first channel structure 170a and the second channel structure 170b.

[0026] The impurity region structures 150a, 150b and 150c may include a semiconductor material. In some implementations, each of the impurity region structures 150a, 150b and 150c may include single crystal silicon. In some implementations, each of the impurity region structures 150a, 150b and 150c may include single crystal silicon germanium.

[0027] In the cross-sectional view, each of the impurity region structures 150a, 150b, and 150c may contact sidewalls of silicon patterns 104a vertically disposed in the channel structures 170a and 170b, and may be connected with the adjacent channel structures 170a and 170b.

[0028] Each of the first, second and third impurity region structures 150a, 150b, and 150c may be formed by selective epitaxial growth from a first active fin protruding from the substrate. The first active fin may have a first portion, a second portion and a third portion. The first portion may have the first width in the second direction, and both sidewalls of the first portion in the second direction may have a line shape. The second portion may have the second width less than the first width in the second direction, and both sidewalls of the second portion in the direction may have a line shape. The third portion may be positioned between the first and second portions, and at least one sidewall of the third portion in the second direction may have a tapered shape.

[0029] In some implementations, first sidewalls of the first to third portions in the second direction may have a straight line shape extending in the first direction. A second sidewall of the third portion in the second direction may have the tapered shape.

[0030] The first impurity region structure 150a may be formed by growing from the first

portion by a selective epitaxial growth process. The second impurity region structure 150b may be formed by growing from the second portion by a selective epitaxial growth process. The third impurity region structure 150c may be formed by growing from the third portion by a selective epitaxial growth process.

[0031] A maximum width of the first impurity region structure 150a in the second direction may have a third width W3 greater than the first width W1. In the plan view, the first impurity region structures 150a may have the same first size. The first impurity region structures 150a may have the same first volume. In some implementations, in the plan view, the first impurity region structure 150a may be symmetrical to each other with respect to a straight line passing through a center thereof in the first direction. In the plan view, the first impurity region structure 150a may be symmetrical to each other with respect to a straight line passing through a center thereof in the second direction.

[0032] A maximum width of the second impurity region structure 150b in the second direction may have a fourth width W4. The fourth width W4 may be greater than the second width W2, and may be less than the third width W3. In the plan view, the second impurity region structures 150b may have a second size smaller than the first size. The second impurity region structures 150b may have a second volume smaller than the first volume.

[0033] In some implementations, in the plan view, the second impurity region structure 150b may be symmetrical to each other with respect to a straight line passing through a center thereof in the first direction. In the plan view, the second impurity region structure 150b may be symmetrical to each other with respect to a straight line passing through a center thereof in the second direction.

[0034] A maximum width of the third impurity region structure 150c in the second direction may have a fifth width W5. The fifth width W5 may be greater than the fourth width W4,

and may be less than the third width W3. In the plan view, the third impurity region structures 150c may have a third size smaller than the first size and greater than the second size. The third impurity region structures 150c may have a third volume smaller than the first volume and greater than the second volume.

[0035] In some implementations, in the plan view, the third impurity region structure 150c may be asymmetrical to each other with respect to a straight line passing through a center thereof in the first direction. In the plan view, the third impurity region structure 150c may be asymmetrical to each other with respect to a straight line passing through a center thereof in the second direction. In the plan view, in the third impurity region structure 150b, a portion grown from the tapered second sidewall of the third portion in the first active fin may have a shape different from a shape of a portion grown from the liner first sidewall of the third portion in the first active fin.

[0036] In each of the first to third impurity region structures 150a, 150b and 150c, lengths in the second direction of uppermost flat surfaces in the first to third impurity region structures 150a, 150b and 150c may be different from each other. As the width of the impurity region structure in the second direction increases, the length of the uppermost flat surface may increase. Accordingly, the length of the flat surface of the first impurity region structure 150a may be the longest and the length of the flat surface of the second impurity region structure 150b may be the shortest.

[0037] The impurity region structures 150a, 150b and 150c may include a single crystal silicon material. In some implementations, the impurity region structures 150a, 150b and 150c may include silicon or silicon germanium. The impurity region structure 150a, 150b and 150c may be doped with impurities. The impurity region structures 150a, 150b, and 150c may serve as source/drain regions of the multi-bridge channel transistors.

[0038] In a cross-sectional view cut in the second direction, each of the impurity region

structures 150a, 150b, and 150c may have a polygonal shape (e.g., a pentagon, a hexagon, or a partial of a quadrangle) in which a central portion protrudes. The first impurity region structure 150a may protrude from sidewalls of adjacent first channel structure 170a in the second direction. The second impurity region structure 150b may protrude from sidewalls of adjacent second channel structure 170b in the second direction. The third impurity region structure 150c may protrude from sidewalls of each of the adjacent first and second channel structures 170a and 170b in the second direction. The maximum width in the second direction of each of the impurity region structures 150a, 150b, and 150c may be greater than the width in the second direction of the channel structures 170a and 170b adjacent to each of the impurity region structures 150a, 150b, and 150c. In some implementations, each of the first to third impurity region structures 150a, 150b, and 150c may have the same width in the first direction.

[0039] Gate structures 180a, 180b, 180c, and 180d may extend in the second direction while surrounding each of the channel structures 170a and 170b. The gate structures 180a, 180b, 180c and 180d may serve as gates of the multi-bridge channel transistors. Each of the gate structures 180a, 180b, 180c and 180d may include an interface pattern (not shown), a gate insulation pattern 181a, a gate electrode 181b, and a capping pattern 181c. Each of the gate structures 180a, 180b, 180c and 180d may cover surfaces of the channel structures 170a and 170b, and may fill the gap included in the each of channel structures 170a and 170b.

[0040] In some implementations, each of the gate structures 180a, 180b, 180c and 180d may have the same width in the first direction.

[0041] In some implementations, spacers (referred to FIG. 2, 196) may be further formed on upper sidewalls of the gate structures 180a, 180b, 180c and 180d. In some implementations, inner spacers (referred to FIG. 2, 198) may be further formed on both sidewalls of the gate structures 180a, 180b, 180c and 180d formed in the gaps included in each of the channel

structures 170a and 170b.

[0042] As the gate structures 180a, 180b, 180c, and 180d are formed on the active structure 172, the first multi-bridge channel transistors TR1, the second multi-bridge channel transistor TR2 and buffer multi-bridge channel transistors TR3a and TR3b, e.g., buffer transistors, may be formed on the active structure 172.

[0043] In some implementations, the active structure 172 may further include a diffusion break region (DB) for electrically isolating the multi-bridge channel transistors. The diffusion break region DB may be positioned between adjacent impurity region structures. A separation pattern 190 may be formed in the diffusion break region DB. The separation pattern 190 may include an insulation material, e.g., silicon oxide, silicon nitride, or the like.

[0044] The first multi-bridge channel transistors TR1, the second multi-bridge channel transistors TR2 and the buffer multi-bridge channel transistors TR3a and TR3b may be arranged in the first direction, and may be connected in series in the first direction to be shared source/drains region with each other.

[0045] As shown in FIG. 6, the first multi-bridge channel transistor TR1 may be a high-power transistor having high performance. The first multi-bridge channel transistor TR1 may include a first gate structure 180a and the first impurity region structures 150a adjacent to both sides of the first gate structure 180a. The first impurity region structures 150a may serve as first source/drain regions of the first multi-bridge channel transistor TR1. Since the first impurity region structures 150a have the first volume, the first source/drain regions may have the same first volume. The first gate structure 180a may extend in the second direction while surrounding the first channel structure 170a disposed between the first impurity region structures 150a. In the first multi-bridge channel transistor TR1, a width of a channel may have the first width, and the first source/drain regions may have the first volume. Therefore, on-currents during operation of the first multi-bridge channel transistor

TR1 may be increased, and the first multi-bridge channel transistor TR1 may have high operation speed.

[0046] As shown in FIG. 7, the second multi-bridge channel transistor TR2 may be a low-power transistor having lower performance than that of the first multi-bridge channel transistor TR1. The second multi-bridge channel transistor TR2 may include a second gate structure 180b and the second impurity region structures 150b adjacent to both sides of the second gate structure. The second impurity region structures 150b may serve as second source/drain regions of the second multi-bridge channel transistor TR2. Since the second impurity region structures 150b have the second volume smaller than the first volume, the second source/drain regions may have the same second volume. The second gate structure 180b may extend in the second direction while surrounding the second channel structure 170b disposed between the second impurity region structures 150b. In the second multi-bridge channel transistor TR2, a width of the channel may have the second width less than the first width. Since the second multi-bridge channel transistor TR2 has a width of a channel less than the width of the channel of the first multi-bridge channel transistor TR1 and the volume of the second source/drain regions smaller than the volume of the first source/drain regions in the first multi-bridge channel transistor TR1, on currents during operation of the second multi-bridge channel transistor TR2 may be decreased and the operation speed thereof may be low.

[0047] The buffer multi-bridge channel transistors TR3a and TR3b may operate with an intermediate performance of the first and second multi-bridge channel transistors TR1 and TR2. The buffer multi-bridge channel transistors TR3a and TR3b may be electrically connected to at least one of the first multi-bridge channel transistor TR1 and the second multi-bridge channel transistor TR2.

[0048] In some implementations, the buffer multi-bridge channel transistors TR3a and TR3b

may include a plurality of transistors having different electrical characteristics. For example, the buffer multi-bridge channel transistors TR3a and TR3b may include a first buffer multi-bridge channel transistor TR3a and a second buffer multi-bridge channel transistor TR3b.

[0049] As shown in FIG. 5A, the first buffer multi-bridge channel transistor TR3a may include a third gate structure 180c, a third impurity region structure 150c adjacent to one side of the third gate structure 180c and the second impurity region structure 150b adjacent to the other side of the third gate structure 180c. The third gate structure 180c can serve as a gate to the to the first buffer multi-bridge channel transistor TR3. The third impurity region structure 150c may serve as a third source region of the first buffer multi-bridge channel transistor TR3a. The second impurity region structure 150b may serve as a third drain region of the first buffer multi-bridge channel transistor TR3a. The second impurity region structure 150b may be shared with the first buffer multi-bridge channel transistor TR3a and the second multi-bridge channel transistor TR2, and the second impurity region structure 150b may serve as a common impurity region. The first buffer multi-bridge channel transistor TR3a may be electrically connected to the second multi-bridge channel transistor TR2.

[0050] Therefore, the third source region may have the third volume smaller than the first volume and greater than the second volume, and the third drain region may have the second volume. In the first buffer multi-bridge channel transistor TR3a, the third source region and the third drain region may have different volumes.

[0051] The third gate structure 180c may extend in the second direction while surrounding the second channel structure 170b disposed between the third source/drain regions. As the third gate structure 180c overlaps the second channel structure 170b, the channel of the first buffer multi-bridge transistor TR3a may have the second width W2 in the second direction.

[0052] In this case, the width in the second direction of the second channel structure 170b overlapping the third gate structure 180c may not vary depending on positions of the second channel structure 170b. Since the width in the second direction of the channel of the first buffer multi-bridge transistor TR3a does not vary according to the positions of the channel, variation of electrical characteristics generated as the width of the channel in the second direction is changed may not occur.

[0053] As shown in FIG. 5B, the second buffer multi-bridge channel transistor TR3b may include a fourth gate structure 180d, the third impurity region structure 150c adjacent to one side of the fourth gate structure 180d and the first impurity region structure 150a adjacent to the other side of the fourth gate structure 180d. The fourth gate structure 180d can serve as a gate to the to the second buffer multi-bridge channel transistor TR3b. The third impurity region structure 150c may serve as a fourth source region of the second buffer multi-bridge channel transistor TR3b. The first impurity region structure 150a may serve as a fourth drain region of the second buffer multi-bridge channel transistor TR3b. The first impurity region structure 150a may be shared with the second buffer multi-bridge channel transistor TR3b and the first multi-bridge channel transistor TR1, and may serve as a common impurity region. The second buffer multi-bridge channel transistor TR3b may be electrically connected to the first multi-bridge channel transistor TR1.

[0054] Therefore, the fourth source region may have the third volume smaller than the first volume and greater than the second volume. The fourth drain region may have the first volume. In the second buffer multi-bridge channel transistor TR3b, the fourth source region and the fourth drain region may have different volumes.

[0055] Since the volume of the fourth drain region of the second buffer multi-bridge channel transistor TR3b is greater than that of the third drain region of the first buffer multi-bridge channel transistor TR3a, the second buffer multi-bridge channel transistor TR3b may have a

performance higher than a performance of the first buffer multi-bridge channel transistor TR3a.

[0056] The fourth gate structure 180d may extend in the second direction while surrounding the first channel structure 170a disposed between the fourth source/drain regions. As the fourth gate structure 180d overlaps the first channel structure 170a, the channel of the second buffer multi-bridge transistor TR3a may have the first width W1 in the second direction greater than the second width W2.

[0057] In this case, the width in the second direction of the first channel structure 170a overlapping the fourth gate structure 180d may not vary depending on the position of the first channel structure 170a. Since the width in the second direction of the channel of the second buffer multi-bridge transistor TR3a does not vary depending on the position of the channel, variation of electrical characteristics generated as the width of the channel in the second direction is changed may not occur.

[0058] The separation pattern 190 may be adjacent to the third impurity region structure 150c and may extend in the second direction. The separation pattern 190 may be disposed between the impurity region structures to electrically isolate the impurity region structures. In some implementations, the separation pattern 190 may be disposed between the first impurity region structure 150a and the third impurity region structure 150c. In some implementations, the separation pattern 190 may be disposed between the second impurity region structure 150b and the third impurity region structure 150c.

[0059] In some implementations, one separation pattern 190 and at least one buffer multi-bridge channel transistor TR3a and TR3b may be formed between the first multi-bridge channel transistor TR1 and the second multi-bridge channel transistor TR2.

[0060] The buffer multi-bridge channel transistors TR3a and TR3b may be disposed adjacent to the separation pattern 190. For example, the separation pattern 190 may be

disposed between the first buffer multi-bridge channel transistor TR3a and the first multi-bridge channel transistor TR1. For example, the separation pattern 190 may be disposed between the second buffer multi-bridge channel transistor TR3b and the second multi-bridge channel transistor TR2.

[0061] An insulating interlayer 192 may cover the first to fourth gate structures 180a, 180b, 180c and 180d and a sidewall of the separation pattern 190.

[0062] As described above, the first multi-bridge channel transistor, the second multi-bridge channel transistor and the buffer multi-bridge channel transistor may have different electrical characteristics.

[0063] FIGS. 8 to 22 are plan views, cross-sectional views and perspective views illustrating a method of manufacturing an example of a semiconductor device.

[0064] Referring to FIG. 8, a silicon germanium layer 102 and a silicon layer 104 may be alternately and repeatedly stacked on a substrate 100. A mask pattern 106 may be formed on an uppermost silicon layer 104. The substrate 100 may be a single crystal silicon substrate.

[0065] The silicon germanium layer 102 and the silicon layer 104 may be formed by a selective epitaxial growth process. The silicon germanium layer 102 may be formed on the substrate 100 by the selective epitaxial growth process using an upper surface of the substrate 100 as a seed.

[0066] In some implementations, the silicon layer 104 may be formed by a selective epitaxial growth process using a silicon source gas such as disilane (Si_2H_6) gas. The silicon layer 104 may include single crystal silicon.

[0067] In some implementations, the silicon germanium layer 102 may be formed by a selective epitaxial growth process using a silicon source gas such as dichlorosilane (SiH_2Cl_2) gas, and a germanium source gas such as germanium tetrahydride (GeH_4) gas. The silicon

germanium layer 102 may include single crystal silicon germanium.

[0068] The mask pattern 106 may be formed by a deposition process of a mask layer and a patterning process of the mask layer. The mask pattern 106 may include, e.g., nitride such as silicon nitride. The mask pattern 106 may have a line shape extending in the first direction.

[0069] In a plan view, the mask pattern 106 may include a first portion 106a, a second portion 106b and a third portion 106c. The first portion may have a first width W1 in the second direction, and both sidewalls of the first portion in the second direction may have a straight line shape. The second portion 106b may have a second width W2 less than the first width W1, and both sidewalls of the second portion in the second direction may have a straight line shape. The third portion 106c may be disposed between the first and second portions 106a and 106b, and at least one of sidewalls of the third portion in the second direction may have a tapered shape. Accordingly, the width of the third portion 106c in the second direction may gradually decrease from the first portion 106a toward the second portion 106b.

[0070] FIGS. 9 and 10, the silicon germanium layers 102, the silicon layers 104 and an upper portion of the substrate 100 may be etched using the mask pattern 106 as an etching mask to form first trenches. The etching process may include an anisotropic etching process.

[0071] Accordingly, the substrate 100 may be etched to form an active pattern 112 extending in the first direction. A first fin structure 120 may be formed on the active pattern 112. The first fin structure 120 may include first silicon germanium patterns 102a and first silicon patterns 104a that are alternately and repeatedly stacked on the active pattern 112. The first fin structure 120 and the mask pattern 106 may be formed on the active pattern 112.

[0072] Preferably, a sidewall profile of the first fin structure 120 in the second direction may

be a vertical profile. Therefore, the sidewall profile of the first fin structure 120 in the second direction is illustrated as the vertical profile. However, according to characteristics of the anisotropic etching process, the sidewall profile of the first fin structure 120 in the second direction may have an inclined profile such that a width of the first fin structure 120 may be gradually increased to downward.

[0073] A device isolation layer may be formed to fill the first trenches. An upper portion of the device isolation layer may be removed, so that the device isolation pattern 122 covering a sidewall of the active pattern 112 may be formed in the first trench. The mask pattern 106 may be removed. The first fin structure 120 may be between the device isolation patterns 122, and may protrude upward from the device isolation patterns 122.

[0074] Since the first fin structure 120 is formed by using the mask pattern 106 as the etching mask, in a plan view, the first fin structure 120 may have a shape substantially the same as a shape of the mask pattern 106. Accordingly, in the plan view, the first fin structure 120 may include a first portion 120a, a second portion 120b and a third portion 120c. The first portion 120a may have the first width W1 in the second direction and both sidewalls of the first portion 120a in the second direction may have a straight line shape. The second portion 120b may have the second width W2 less than the first width W1 in the second direction, and both sidewalls of the second portion 120b in the second direction may have a straight line shape. The third portion 120c may be between the first and second portions 120a and 120b, and at least one sidewalls of the third portion 120c in the second direction may have a tapered shape.

[0075] Referring to FIGS. 11 and 12, dummy gate structures 130 may be formed to partially cover the device isolation pattern 122 and the first fin structure 120. The dummy gate structures 130 may extend in the second direction. Accordingly, the dummy gate structures 130 may extend to cross the first fin structure 120. In some implementations, each of the

dummy gate structures 130 may have the same width.

[0076] The dummy gate structures 130 may be spaced apart from each other in the first direction. In some implementations, the dummy gate structures 130 may be spaced apart from each other at equal spacing in the first direction.

[0077] Each of the dummy gate structures 130 may include a dummy gate insulation pattern, a dummy gate electrode, and a dummy gate mask pattern.

[0078] A region where the dummy gate structures 130 are formed may be a region where a gate structure of a multi-bridge channel transistor or a diffusion break region is subsequently formed, respectively. A portion of the first fin structure 120 covered by the dummy gate structures 130 may be formed as a channel structure of the multi-bridge channel transistor by subsequent processes. A portion of the first fin structure 120 between the dummy gate structures 130 may be formed as an impurity region structure of the multi-bridge channel transistor by subsequent processes.

[0079] In some implementations, the dummy gate structures 130 may be formed to cover a part of the first portion 120a of the first fin structure 120 and a part of the second portion 120b of the first fin structure 120. In some implementations, the dummy gate structures 130 may not be formed on the third portion 120c of the first fin structure 120, and may not cover the third portion 120c of the first fin structure 120.

[0080] Referring to FIGS. 13 and 14, the first fin structure 120 disposed between the dummy gate structures 130 may be removed to form openings 142. Accordingly, the first fin structure 120 may be cut to form preliminary channel structures 140a and 140b. The preliminary channel structures 140a and 140b may be disposed in parallel, and may be spaced apart from each other in the first direction. Each of the preliminary channel structures 140a and 140b may include a first silicon germanium pattern 102a and a first silicon pattern 104a alternately and repeatedly stacked.

[0081] The preliminary channel structures 140a and 140b may include a first preliminary channel structure 140a having the first width W1 in the second direction and a second preliminary channel structure 140a having the second width W2 in the second direction. An active pattern 112 may be exposed by a bottom surface of the opening 142 between the preliminary channel structures 140a and 140b.

[0082] Although not shown, in some implementations, after forming the openings 142, a spacer may be formed on the sidewalls of the dummy gate structures.

[0083] Although not shown, in some implementations, after forming the openings 142, a portion of the sidewall of the exposed first silicon germanium pattern 102a may be etched to form a recess, and an inner spacer may be further formed in the recess.

[0084] Referring to FIG. 15, a selective epitaxial growth process may be performed at the openings 142 to form impurity region structures 150a, 150b and 150c in the openings 142. The impurity region structures 150a, 150b and 150c may include a semiconductor material.

[0085] In some implementations, each of the impurity region structures 150a, 150b and 150c may include single crystal silicon. In some implementations, each of the impurity region structures 150a, 150b and 150c may include single crystal silicon germanium.

[0086] In some implementations, impurities may be doped in situ during the selective epitaxial growth process. Accordingly, the impurity region structures 150a, 150b, and 150c may serve as source/drain regions of multi-bridge channel transistors subsequently formed.

[0087] In the selective epitaxial growth process, crystal growth may be performed in the vertical direction from the active pattern 112 exposed by the bottom surface of the opening 142. In addition, in the selective epitaxial growth process, crystal growth may be further performed in the second direction. Accordingly, each of the impurity region structures 150a, 150b and 150c may have a polygonal shape in which a center portion protrudes, in a cross-sectional view in the second direction.

[0088] The impurity region structures 150a, 150b, and 150c may contact both sidewalls of the preliminary channel structures 140a and 140b in the first direction, and thus the impurity region structures 150a, 150b, and 150c may be connected with the preliminary channel structures 140a and 140b.

[0089] The impurity region structures may include a first impurity region structure 150a, a second impurity region structure 150b and a third impurity region structure 150c. The first impurity region structure 150a may be disposed between the first preliminary channel structures 140a. The second impurity region structure 150b may be disposed between the second preliminary channel structures 140b. The third impurity region structure 150c may be disposed between the first and second preliminary channel structures 140a and 140b.

[0090] The first impurity region structure 150a may be formed by crystal growth from sidewalls of the first preliminary channel structures 140a and the active pattern 112. Therefore, the first impurity region structure 150a may have a third width W3 greater than the first width W1 in the second direction. In the plan view, the first impurity region structures 150a may have the same first size. The first impurity region structures 150a may have the same first volume.

[0091] In some implementations, in the plan view, the first impurity region structure 150a may be symmetrical to each other with respect to a straight line passing through a center of the first impurity region structure 150a in the first direction. In the plan view, the first impurity region structure 150a may be symmetrical to each other with respect to a straight line passing through a center of the first impurity region structure 150a in the second direction.

[0092] The second impurity region structure 150b may be formed by crystal growth from sidewalls of the second preliminary channel structures 140b and the active pattern 112. Therefore, the maximum width of the second impurity region structure 150b in the second

direction may be a fourth width W4. The fourth width W4 may be greater than the second width W2, and may be less than the third width W3. The second impurity region structures 150b may have a second size smaller than the first size. The second impurity region structures 150b may have a second volume smaller than the first volume.

[0093] In some implementations, in the plan view, the second impurity region structure 150b may be symmetrical to each other with respect to a straight line passing through a center of the second impurity region structure 150b in the first direction. In the plan view, the second impurity region structure 150b may be symmetrical to each other with respect to a straight line passing through a center of the second impurity region structure 150b in the second direction.

[0094] A maximum width of the third impurity region structure 150c in the second direction may be a fifth width W5. The fifth width W5 may be greater than the fourth width W4, and may be less than the third width W3. In the plan view, the third impurity region structures 150c may have a third size smaller than the first size and greater than the second size. The third impurity region structures 150c may have a third volume smaller than the first volume and greater than the second volume.

[0095] In some implementations, in the plan view, the third impurity region structure 150c may be asymmetrical to each other with respect to a straight line passing through a center of the third impurity region structure 150c in the first direction. In the plan view, the third impurity region structure 150c may be asymmetrical to each other with respect to a straight line passing through a center of third impurity region structure 150c in the second direction. In the plan view, in the third impurity region structure 150b, a portion grown from the second sidewall having a tapered shape of the third portion of the first active fin and a portion grown from the first sidewall having a straight line shape of the third portion of the first active fin may have different shapes.

[0096] FIG. 17 is a perspective view of the impurity region structure and a first preliminary channel structure. FIG. 18 is a perspective view of the impurity region structure and a channel structure.

[0097] Referring to FIGS. 16 and 17, an insulating interlayer (not shown) may be formed to cover the first to third impurity region structures 150a, 150b and 150c, the device isolation pattern and the dummy gate structure 130. Thereafter, the insulating interlayer may be planarized until a top surface of the dummy gate structure 130 may be exposed.

[0098] The dummy gate structures 130 may be removed to form a first gate trench (not shown). The first silicon germanium patterns 102a and the first silicon patterns 104a in the preliminary channel structures 140a and 140b may be exposed by the first gate trench.

[0099] Referring to FIG. 18, the first silicon germanium patterns 102a exposed by the first gate trench may be selectively removed to form gaps 154 between the first silicon patterns 104a. The first silicon patterns 104a spaced apart from each other in the vertical direction. The first silicon patterns may serve as a channel region of the multi-bridge channel transistor.

[00100] As the first silicon germanium pattern 102a is removed, the preliminary channel structures 140a and 140b may be formed as channel structures. The channel structure may include a first channel structure 170a having the first width W1 in the second direction and a second channel structure 170b having the second width W2 in the second direction.

[00101] The channel structure and the impurity region structure may be alternately disposed in the first direction, and may be connected to each other to form the active structure 172. The active structure 172 may include first channel structures 170a, second channel structures 170b, the first impurity region structure 150a between the first channel structures 170a, the second impurity region structure 150b between the second channel structures 170b and the third impurity region structure 150c between the first and second channel structures 170a and 170b.

[00102] Referring to FIGS. 19 and 20, gate structures 180a, 180b, 180c, 180d and 180 may be formed to fill the first gate trench and gaps 154 to form multi-bridge channel transistors.

[00103] Particularly, a thermal oxidation process may be performed on surfaces of the active pattern 112 and the first silicon patterns 104a exposed by the first gate trench and gaps 154 to form an interface layer. A gate insulation layer may be formed on the interface layer. A gate electrode layer may be formed on the gate insulation layer to fill the first gate trench and the gaps 154. The gate electrode layer may include a metal material. Thereafter, the gate electrode layer and the gate insulating layer may be planarized until an upper surface of the insulating interlayer 192 may be exposed. Upper portions of the gate electrode layer and the gate insulation layer may be removed, and a capping layer pattern may be formed on the remained the gate electrode layer and the gate insulation layer. Accordingly, gate structures 180a, 180b, 180c and 180d including an interface pattern (not shown), a gate insulation pattern 181a, a gate electrode 181b, and a capping pattern 181c may be formed.

[00104] Each of the multi-bridge channel transistors may include the gate structures 180a, 180b, 180c, and 180d and source/drain regions formed in the impurity region structures 150a, 150b, and 150c adjacent to both sides of the gate structures 180a, 180b, 180c, and 180d. The multi-bridge channel transistors may be connected to each other in series in the first direction, and may be shared with source/drain regions.

[00105] However, the impurity region structures may include first to third impurity region structures 150a, 150b, and 150c having different volumes. Accordingly, the electrical characteristics of each of the multi-bridge channel transistors may vary according to the volumes of the source/drain regions.

[00106] Through the above process, a first multi-bridge channel transistor TR1, a second multi-bridge channel transistor TR2, and buffer multi-bridge channel transistors TR3a and TR3b having different electrical characteristics may be formed.

[00107] The first multi-bridge channel transistor TR1 may include a first gate structure 180a and first impurity region structures 150a adjacent to both sides of the first gate structure 180a. The first impurity region structures 150a may serve as first source/drain regions of the first multi-bridge channel transistor TR1. The first gate structure 180a may extend in the second direction while surrounding the first channel structure 170a disposed between the first source/drain regions.

[00108] The second multi-bridge channel transistor TR2 may include a second gate structure 180b and second impurity region structures 150b adjacent to both sides of the second gate structure. The second impurity region structures 150b may serve as second source/drain regions of the second multi-bridge channel transistor TR2. The second gate structure 180b may extend in the second direction while surrounding the second channel structure 170b disposed between the second source/drain regions.

[00109] The buffer multi-bridge channel transistors TR3a and TR3b may include a first buffer multi-bridge channel transistor TR3a and a second buffer multi-bridge channel transistor TR3b.

[00110] The first buffer multi-bridge channel transistor TR3a may include a third gate structure 180c, the third impurity region structure 150c adjacent to one side of the third gate structure 180c and the second impurity region structure 150b adjacent to the other side of the third gate structure 180c. The third impurity region structure 150c may serve as a third source region of the first buffer multi-bridge channel transistor TR3a. The second impurity region structure 150b may serve as a third drain region of the first buffer multi-bridge channel transistor TR3a.

[00111] The second buffer multi-bridge channel transistor TR3b may include a fourth gate structure 180d, the third impurity region structure 150c adjacent to one side of the fourth gate structure 180d, and the first impurity region structure 150a adjacent to the other side of the

fourth gate structure 180d. The third impurity region structure 150c may serve as a fourth source region of the second buffer multi-bridge channel transistor TR3b. The first impurity region structure 150a may serve as a fourth drain region of the second buffer multi-bridge channel transistor TR3b.

[00112] Referring to FIGS. 21 and 22, the gate structure 180 positioned at a diffusion break region DB may be selectively removed. Subsequently, the channel structure exposed by a removed portion of the gate structure 180 may be removed. In this case, the active structure 172 may be cut in the diffusion break region DB.

[00113] An insulation material may be formed to fill an opening formed by removing the gate structure 180 and the channel structure in the diffusion break region DB to form a separation pattern 190. The separation pattern 190 may serve as a diffusion break pattern.

[00114] The buffer multi-bridge channel transistors TR3a and TR3b may be adjacent to the separation pattern 190. For example, the separation pattern 190 may be disposed between the first buffer multi-bridge channel transistor TR3a and the first multi-bridge channel transistor TR1. Alternatively, the separation pattern 190 may be disposed between the second buffer multi-bridge channel transistor TR3b and the second multi-bridge channel transistor TR2.

[00115] Through the above processes, a semiconductor device including the first multi-bridge channel transistors TR1, the second multi-bridge channel transistors TR2 and the buffer multi-bridge channel transistors TR3a and TR3b may be manufactured. The buffer multi-bridge channel transistors TR3a and TR3b may have an intermediate performance of the first and second multi-bridge channel transistors TR1 and TR2.

[00116] FIGS. 23 to 25 are plan views illustrating examples of semiconductor devices.

[00117] The semiconductor devices shown in FIGS. 23 to 25 may be the same as the semiconductor device described with reference to FIGS. 1 to 7, except for presence and

absence of the separation pattern and a position of the separation pattern. Therefore, redundant description thereof may be omitted.

[00118] Referring to FIG. 23, the active structure may not include a diffusion break region. Accordingly, only buffer multi-bridge channel transistors may be formed between the first and second multi-bridge channel transistors TR1 and TR2.

[00119] In some implementations, each of the first and second buffer multi-bridge channel transistors TR3a and TR3b may be disposed between the first and second multi-bridge channel transistors TR1 and TR2.

[00120] In some implementations, the first multi-bridge channel transistor TR2, the second buffer multi-bridge channel transistor TR3b, the first buffer multi-bridge channel transistor TR3a and the second multi-bridge channel transistor TR2 may be electrically connected to each other.

[00121] Referring to FIG. 24, one separation pattern 190 and one first buffer multi-bridge channel transistor TR3a may be disposed between the first and second multi-bridge channel transistors TR1 and TR2.

[00122] The first buffer multi-bridge channel transistor TR3a may include the third gate structure 180c surrounding the second channel structure 170b, the third impurity region structure 150c adjacent to one side of the third gate structure 180c, and the second impurity region structure 150b adjacent to the other side of the third gate structure 180c. The separation pattern 190 may be disposed between the first buffer multi-bridge channel transistor TR3a and the first multi-bridge channel transistor TR1.

[00123] The second multi-bridge channel transistor TR2 may be electrically connected to the first buffer multi-bridge channel transistor TR3a.

[00124] Referring to FIG. 25, one separation pattern 190 and one second buffer multi-bridge channel transistor TR3b may be disposed between the first and second multi-bridge channel

transistors TR1 and TR2.

[00125] The second buffer multi-bridge channel transistor TR3b may include the fourth gate structure 180d, the third impurity region structure 150c adjacent to one side of the fourth gate structure 180d, and the first impurity region structure 150a adjacent to the other side of the fourth gate structure 180d. The third impurity region structure 150c may serve as a fourth source region of the second buffer multi-bridge channel transistor TR3b. The separation pattern 190 may be disposed between the second buffer multi-bridge channel transistor TR3b and the second multi-bridge channel transistor TR2.

[00126] The first multi-bridge channel transistor TR1 may be electrically connected to the second buffer multi-bridge channel transistor TR3b.

[00127] FIG. 26 is a plan view illustrating an example of a semiconductor device.

[00128] The semiconductor device shown in FIG. 26 may be the same as the semiconductor device described with reference to FIGS. 1 to 7, except for a plurality of separation patterns. Therefore, redundant description thereof may be omitted.

[00129] Referring to FIG. 26, a plurality of separation patterns 190 and at least one buffer multi-bridge channel transistor TR3a and TR3b may be disposed between the first and second multi-bridge channel transistors TR1 and TR2.

[00130] In a region between the first and second multi-bridge channel transistors TR1 and TR2, the second buffer multi-bridge channel transistor TR3b may be disposed adjacent to the first multi-bridge channel transistor TR1 positioned at an end in a region of the first multi-bridge channel transistors TR1.

[00131] In the region between the first and second multi-bridge channel transistors TR1 and TR2, a first buffer multi-bridge channel transistor TR3a may be disposed adjacent to the second multi-bridge channel transistor TR2.

[00132] In addition, in the region between the first and second multi-bridge channel

transistors TR1 and TR2, the plurality of separation patterns 190 may be formed between the buffer multi-bridge channel transistors. The impurity region structures 151a, 151b and 151c adjacent to both sides of each of the separation patterns 190 may have different volumes. The volumes of the impurity region structures 151a, 151b, and 151c adjacent to both sides of each of separation patterns 190 may be gradually decreased from a region formed the first multi-bridge channel transistor TR3a toward a region formed the second multi-bridge channel transistor TR3b.

[00133] The foregoing is illustrative of example implementations and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, all such modifications are intended to be included within the scope of the present inventive concept as defined in the claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures. Therefore, it is to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

What is claimed is:

1. A semiconductor device, comprising:

a plurality of first channel structures on a substrate, the first channel structures spaced apart from each other in a first direction parallel to a surface of the substrate, each of the first channel structure having a first width in a second direction parallel to the surface of the substrate and perpendicular to the first direction, and including silicon patterns spaced apart from each other in a vertical direction;

a plurality of second channel structures on the substrate, the second channel structures spaced apart from each other in the first direction, each of the second channel structure having a second width in the second direction less than the first width, and including silicon patterns spaced apart from each other in the vertical direction;

a first impurity region structure between the first channel structures, the first impurity region structure connecting sidewalls of adjacent first channel structures, and having a first volume;

a second impurity region structure between second channel structures, the second impurity region structure connecting sidewalls of adjacent second channel structures, and having a second volume smaller than the first volume;

a third impurity region structure between the first and second channel structures, the third impurity region structure connecting sidewalls of adjacent first and second channel structures, and having a third volume smaller than the first volume and greater than the second volume; and

a plurality of gate structures disposed between the first to third impurity region structures, respectively, each of the gate structure covering one of the first and second channel structures, and extending in the second direction.

2. The semiconductor device of claim 1, wherein a maximum width of the first impurity region structure in the second direction is a third width greater than the first width, and a maximum width of the second impurity region structure in the second direction is a fourth width greater than the second width and less than the third width.

3. The semiconductor device of claim 2, wherein a maximum width of the third impurity region structure in the second direction is a fifth width less than the third width and greater than the fourth width.

4. The semiconductor device of any one of claims 1 to 3, wherein each of the first to third impurity region structures has substantially the same width in the first direction.

5. The semiconductor device of any one of claims 1 to 4, further comprising:

first buffer gate structures covering the second channel structure between the second and third impurity region structures for serving as a gate of a first buffer transistor; and

second buffer gate structures covering the first channel structure between the first and third impurity region structure for serving as a gate of a second buffer transistor.

6. The semiconductor device of any one of claims 1 to 4, further comprising:

first buffer gate structures covering the second channel structure between the second and third impurity region structures for serving as a gate of a first buffer transistor; and

a first separation pattern between the first and third impurity region structures adjacent to the first buffer gate structures.

7. The semiconductor device of any one of claims 1 to 4, further comprising:

second buffer gate structures covering the first channel structure between the first and third impurity region structures for serving as a gate of a second buffer transistor; and

a second separation pattern between the second and third impurity region structures adjacent to the second buffer gate structure.

8. The semiconductor device of any one of claims 1 to 7, wherein the first impurity region structure protrudes in the second direction from a sidewall of an adjacent first channel structure, the second impurity region structure protrudes from a sidewall of an adjacent second channel structure, and the third impurity region structures protrude in the second direction from sidewalls of each of the adjacent first and second channel structures.

9. The semiconductor device of any one of claims 1 to 8, wherein the first to third impurity region structures include a semiconductor material.

10. The semiconductor device of any one of claims 1 to 9, wherein, in a plan view, the third impurity region structure is asymmetrical with respect to a straight line passing through a center thereof in the first direction.

11. The semiconductor device of any one of claims 1 to 9, wherein, in a plan view, the third impurity region structure is asymmetric with respect to a straight line passing through a center thereof in the second direction.

12. The semiconductor device of any one of claims 1 to 9, wherein, in a plan view, each of the first and second impurity region structures is symmetrical with respect to a

straight line passing through a center thereof in the first direction.

13. A semiconductor device, comprising:

a first transistor on a substrate, the first transistor including a first channel structure having a first width in a second direction parallel to a surface of the substrate, a first gate structure extending in the second direction and parallel to the surface of the substrate to cover the first channel structure, and a first impurity region structure on both sides of the first gate structure in a first direction perpendicular to the second direction, wherein the first impurity region structure is connected to the first channel structure, and have a first volume;

a second transistor on the substrate, the second transistor including a second channel structure having a second width in the second direction less than the first width, a second gate structure extending in the second direction to cover the second channel structure, and a second impurity region structure on both sides of the second gate structure in the first direction, wherein the second impurity region structure is connected to the second channel structure, and has a second volume smaller than the first volume; and

a buffer transistor on the substrate, the buffer transistor including a third channel structure between the first and second transistors, a third gate structure extending in the second direction to cover the third channel structure, a third impurity region structure on a side of the third gate structure in the first direction connected to the third channel structure, and a fourth impurity region structure on another side of the third gate structure connected to the third channel structure, wherein the fourth impurity region structure has a volume different from a volume of the third impurity region structure.

14. The semiconductor device of claim 13, wherein the third impurity region structure and the first impurity region structure are shared with each other to serve as a single

impurity region structure, and the fourth impurity region structure has a third volume smaller than the first volume and greater than the second volume.

15. The semiconductor device of claim 14, further comprising a separation pattern between the fourth impurity region structure and the second impurity region structure.

16. The semiconductor device of claim 13, wherein the third impurity region structure and the second impurity region structure are shared with each other to serve as a single impurity region structure, and the fourth impurity region structure has a third volume smaller than the first volume and greater than the second volume.

17. The semiconductor device of claim 16, further comprising a separation pattern between the fourth impurity region structure and the first impurity region structure.

18. The semiconductor device of any one of claims 13 to 17, wherein each of the first to third channel structures includes silicon patterns spaced apart from each other in a vertical direction perpendicular to the surface of the substrate, and

each of the first to third gate structures extends to fill a gap between the silicon patterns.

19. The semiconductor device of any one of claims 13 to 18, wherein the buffer transistor is electrically connected to at least one of the first transistor and the second transistor.

20. A semiconductor device, comprising:

a first transistor including a first channel structure on a substrate, a first gate structure extending in a second direction parallel to a surface of the substrate to cover the first channel structure, and a first impurity region structure on both sides of the first gate structure in a first direction perpendicular to the second direction, wherein the first impurity region structure is connected to the first channel structure, and has a first volume; and

a buffer transistor including a second channel structure on the substrate, a second gate structure extending in the second direction to cover the second channel structure, and a second impurity region structure on a side of the second gate structure in the first direction to be connected with the second channel structure,

wherein the second impurity region structure has a second volume different from the first volume of the first impurity region structure, and

wherein the first impurity region structure contacts the other side of the second gate structure in the first direction.