ABSTRACT

A semiconductor package includes a first chip and a second chip bonded to and electrically connected to a front surface of the first chip. The first chip includes a first semiconductor substrate including a first through via, a semiconductor element positioned on a front surface of the first semiconductor substrate, and a back side wiring layer including a back side power wiring positioned on a rear surface of the first semiconductor substrate and electrically connected to the semiconductor element unit. The second chip includes a second through via having a size greater than a size of the first through via.

FIG. 1