

TITLE

MULTILAYER PRINTED CIRCUIT BOARD FORMATION

BACKGROUND OF THE INVENTION

5 The present invention is directed to formation of multilayer printed circuit boards and articles formed thereby.

10 Multilayer PCB's are typically constructed by interleaving imaged conductive layers such as one containing copper with dielectric layers such as a partially cured B-stage resin, i.e., a prepreg, into a multilayer sandwich which is then bonded together by applying heat and pressure. Since a conductive layer with a smooth copper surface does not bond well to the
15 prepreg, rough copper surfaces have been employed to obtain a better bond to a dielectric. Therefore, a portion of the multilayer PCB industry applies a mechanical roughening process step to assure better bonding. However, as circuit patterns get finer, there
20 is an increasing risk of physically damaging the conductor traces during this surface preparation.

Another process employed by the industry to improve bonding between the conductive layer and the dielectric are various copper surface oxidation procedures widely
25 practiced in the plating industry to assure good interphasial adhesion.

A common drawback for all processes relying mainly on the mechanical interlocking of a rough copper surface with the dielectric is the marginal bond strength with
30 polyimide prepreg and the fact that there is no flexible bonding interphase to absorb the stresses originating from the different thermal expansion coefficients of copper and dielectric which can cause thermal shock failures.

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REPLACED SHEETS		SG
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Other technologies to improve bonding of conductive layers to dielectric layers in multilayer boards are described in U.S. Patent 3,536,546, as well as European Patent Application 216,531 and also to U.S. Patent 4,657,632, and involve the deposition of tin on the conductive layer prior to bonding. Whereas these techniques give improved bond strength compared to a copper surface, yield a surface less susceptible to mechanical damage than copper oxide, and require only ambient temperature processing in a less corrosive environment than copper oxide treatments, the resulting bond strengths are considered to be comparable to copper oxide on epoxy prepreg, and inferior to brown oxide on polyimide prepreg. Also the bond strength can deteriorate with time at elevated temperatures, as does the oxide bond. In addition, delamination after solder shock is occasionally observed.

An example of disclosure of a black oxide layer on a copper clad laminate as a step in the process of preparing multilayer circuit boards is disclosed in U.S. Patent 4,512,818. The major drawbacks of these procedures are considered to be marginal bond strength on polyimide prepreps, corrosivity and high temperature processing, a surface coating prone to mechanical damage, partial delamination around through-holes called "pink ring" due to the removal of the bonding oxide layer by aggressive (acidic, reductive) hole cleaning chemicals, and a decay of the bond strength with time at elevated temperatures.

The formation of conductive layer topographies particularly suitable to improved bonding with prepreg without the drawbacks of the oxide treatments have been recently described at the Printed Circuit World Conference IV, Tokyo, Japan, June 2-5, 1987. H. Akahoshi et al. (WCIV-9) describe the formation of a

surface oxide which gets removed prior to bonding, leaving a copper surface with roughness and bonding characteristics comparable to the oxide surface. Nakaso et al. (WCIV-10) describe the formation of a rough
5 conductive layer surface by forming an electroless copper deposit on the conductive layer for better bonding. Silanes, deposited on this clean metallic copper surface are reported to yield a marginal increase in bond strength.

10 Likewise, U.S. Patent 3,508,983 discloses the use of gamma-amino propyl triethoxysilane to bond copper to a polyester base adhesive in the manufacture of a printed circuit board. This reference emphasizes the point that copper oxide should be removed prior to the
15 silane treatment to affect good bonding.

U.S. Patent 4,499,152 discloses formation of a metal laminate with utility of high resolution printed circuit patterns. The laminate preferably contains a resin-bonded, glass reinforced substrate, a layer of
20 coupling agent covering and bonded to a major surface of the substrate and a layer of ultra-thin copper adjacent the layer of coupling agent, and a composite bonding layer dispersed between the copper layer and the layer of coupling agent. A disclosure class of coupling
25 agents includes organosilanes.

European Patent Application 88115951.1, published as 0310010 on April 5, 1989, discloses a process for forming multilayer printed circuit boards wherein a ureido silane is used to improve adhesion between tin-
30 plated copper circuitry and the cured insulating layer during subsequent soldering operations. While this process is generally effective when the resulting laminates are prebaked before soldering, in some instances when prebaking is not employed delamination
35 can occur during soldering.



SUMMARY OF THE INVENTION

The present invention is directed to a process and article formed thereby in formation of a multilayer printed circuit board containing conductive through-holes which make electrical connections to a series of electrically conducting layers through several insulating and dielectric layers comprising the steps of:

(a) forming electrically conductive copper circuitry on a surface of a dielectric layer support with the circuitry having a thickness of at least 4 microns;

(b) forming on the copper circuitry a layer of an oxide, hydroxide or combination thereof of tin by application of tin to the copper circuitry whereby during application or subsequent thereto the applied tin is converted on its surface to the corresponding oxide, hydroxide or combination thereof with the proviso that the layer of oxide, hydroxide or combination is not greater than 1.5 microns in thickness;

(c) applying a silane bonding mixture to the surface of the oxide, hydroxide or combination thereof formed in step (b) or on an insulating layer to be bonded to the copper circuitry, the insulating layer comprising a partially cured thermosetting polymer composition and the silane bonding mixture consisting essentially of:

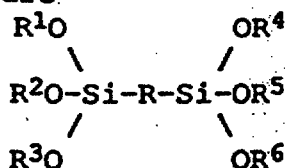
(I) a ureido silane having the structure



wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2 each B need not be identical; and



(II) a disilyl crosslinking agent having the structure



wherein R^1 , R^2 , R^3 , R^4 , R^5 and R^6

independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

(d) repeating steps (a), (b) and (c);

(e) bonding materials formed by steps (a), (b), (c) and (d) into a single article whereby an

organosilane coating is between a layer of the oxide, hydroxide or combination and an insulating layer whereby during bonding the partially cured insulating layer is cured;

(f) forming a number of holes through the bonded article formed in step (e);

(g) metallizing walls of the through-hole to form electrically conductive paths from opposite openings of the through-hole to form a multilayer circuit board with the proviso that the multilayer printed circuit board will not delaminate upon exposure to thermal stress at 550°F for 10 seconds after baking at 250°F for 6 hours and then pre-conditioning at 85°C and 85% relative humidity for twenty-four (24) hours.

The present invention is also directed to a silane bonding mixture for forming a moisture resistant multilayer circuit board consisting essentially of:

(I) a ureido silane having the structure

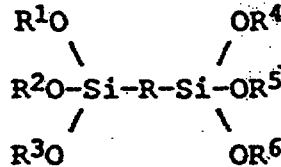


wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1,



2, or 3 with the proviso that if n is 1 or 2 each B need not be identical; and

(II) a disilyl crosslinking agent having the structure



wherein R^1 , R^2 , R^3 , R^4 , R^5 and R^6 independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a process for forming a multilayer printed circuit board. The circuit board has alternating layers of dielectric material which support copper circuitry (which may have interspaced other layers such as a copper sheet which serves as a conductive ground plane) which are adhered to an insulating layer through intermediate layers. The circuit board has conductive through-holes which form electrical paths across the entire thickness of the board.

In formation of multilayer circuit boards several dozen conductive and nonconductive layers can be employed. Also, for formation of multilayer circuit boards, it is necessary to drill holes and defects can occur due to delamination of layers in the areas immediately surrounding a hole. If a defect is present in one of the layers or if delamination occurs, generally the entire board must be scrapped. Therefore high quality in each of the steps of formation of the printed circuit board is essential for commercial production.

With the techniques of the present invention, various articles can be formed. Illustratively one

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article can contain in order, a dielectric layer, copper circuitry with layer of tin and an oxide, hydroxide or combination thereof of the underlying tin, organosilane, an insulating layer, a second dielectric layer, copper circuitry with a layer of tin, an oxide, hydroxide or combination thereof of the underlying tin, organosilane and a second insulating layer. In the above article the (first) insulating layer can be contacted to the second dielectric layer directly or through an adhesive layer. (Such adhesives are well known in the art, e.g., a high temperature epoxy.)

In an alternate article the second dielectric layer need not be present with all other layers having the same order. In a further alternate embodiment of the invention a dielectric layer can be present which has copper circuitry on opposite surfaces. Thereafter on the opposite surface the various layers are applied including optionally a layer of tin with an oxide, hydroxide or combination thereof of the underlying tin, organosilane and insulating layer.

For the multilayer circuit board or a portion thereof containing layers bonded together, a conventional test to determine whether an effective bond is formed with or without intermediate layers is a measurement of the bond strength. The force necessary to separate the layers can be measured by an Instron test apparatus. However, in some instances it is found that the bond strength alone is not a sufficiently rigorous test procedure since failure can occur due to the conditions in which a multilayer board is subjected during processing in commercial use. A useful test in accordance with the present procedure is whether delamination will occur at elevated temperature due to thermal stress is described in MIL-P-55110-D. In actual use the outer surface of a multilayer bond is

conventionally exposed to molten solder. Although the inner layers may not be exposed to the solder, they are subjected to elevated temperature. Therefore a practical test for broad commercial use to correlate whether the multilayer board can be used for general widespread commercial application is one or more tests set forth in MIL-P-55110-D.

One of the tests in MIL-P-55110-D requires thermal stress at 550°F for 10 seconds after a pre-conditioning bake at 275-300°F for two (2) hours. The specimen, i.e., the article, is visually inspected for cracking or plating, separation or plating and conductors, blistering or delamination. Laminate voids with the largest dimension of 0.003 inch (0.08 mm) or less are permitted provided the conductor spacing is not reduced below the minimum dielectric spacing, laterally or vertically. In a more preferred mode for a more stringent test, a time period of 60 seconds is employed rather than 10 seconds.

In another mode for the test procedure the final multilayer circuit board meets all applicable test procedures of MIL-P-51110D.

One reason why this test is applicable to commercial use is due to the diversity of materials employed in the multilayer construction. Although copper is the metal of choice in formation of conductive circuitry, dielectric and insulating layers (which can be of the same material with dielectric employed in the present context to refer to the initial support for a copper sheet which is formed into circuitry while insulating layer refers to another layer to which the circuitry is bonded through intermediate layers) material can drastically differ. Examples of preferred materials are epoxy and polyimide.



- Although the above tests are generally useful in predicting layer bonding in printed circuit manufacture, a more rigid test is needed in the instance when multilayer circuit boards are soldered without a prior baking step to remove moisture. In such instances, delamination at the interface between the circuit and cured insulator layer may occur during soldering, presumably due to residual water or other materials which are volatilized during soldering at the interface.
- 5 A useful test in accordance with this alternate procedure is a "solder immersion stress test" wherein test multilayer printed circuit test boards are first baked at 250°F (121°C) for 6 hours and then conditioned in an environmental test chamber maintained at 85°C and 85% relative humidity (RH) for 0, 4, 24, 48, and 72 hours, after which they are immersed in solder: maintained at 550°F (288°C) for 10 seconds. Each multilayer test board contains eight 100% ground planes of copper and except for the specific variation under test, is made under the same conditions. If no subtle or gross delamination effects are observed, the board is considered acceptable and the evaluation of one group of test boards vs. others is made based on the minimum conditioning time needed before failure is observed.
- 10 20 25 The criteria of acceptability which corresponds to printed circuit manufacturing standards requires that there be no delamination after at least 24 hours conditioning time and preferably after 72 hours conditioning.
- 30 A starting material in the present invention is a dielectric layer which contains on one or opposite surfaces a cladding of copper. This copper layer is of a thickness of at least 4 microns and more preferably 32 microns and it is used to form conductive circuitry.
- 35 Well-known techniques in the prior art can be employed

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to form such circuitry such as by photoimaging technique of a photosensitive resist film followed by etching of unprotected areas of the copper. An example of a suitable technique is disclosed in U.S. Patent

5 3,469,982. The composition of the dielectric layer is not critical provided it functions as an electrical insulator. Useful support materials are disclosed in U.S. Patent 4,499,152 such as epoxy reinforced with glass fiber. Preferably a partially cured thermosetting
10 polymer composition is employed which is known in the art as a prepreg or "B" stage resin. Use of such polymer composition adds in subsequent bonding operations.

After formation of the conductive circuitry, it
15 typically is necessary to form a thin outer layer of an oxide, hydroxide or combination thereof. This layer which is of a thickness not greater than 1.5 microns and more preferably not greater than 1.0 microns can be directly formed by oxidation of the copper circuitry.
20 Well-known techniques used to form so-called "brown" or "black" oxide coatings can be employed. However major problems have been encountered due to a phenomenon known as pink ring formation whereby the oxide is dissolved or is at least partially destroyed due to later required
25 processing steps. Significant research efforts have been undertaken to solve this pink ring effect. Also in formation of oxide coatings corrosive chemicals have been employed which causes problems due to the use of harsh chemicals with special processing necessary. In
30 instances when multilayer circuit boards are soldered without a prior baking step to remove moisture, delamination at the interface between the circuit and cured insulator layer has been observed during soldering. It is theorized that residual water absorbed
35 by the laminate from the ambient environment is



concentrated at the interface and vaporizes during soldering to cause this localized delamination.

In an embodiment of this invention a conductive layer is formed from tin. As will be more fully described below, a preferred technique of application of the coating is by immersion metal plating. The thickness of the metal layer is not critical and can be, e.g., 0.15 to 0.25 microns. During, and subsequent to, the application of tin, a thin coating of an oxide, hydroxide or combination thereof is formed. Since this coating can be extremely thin preferably not greater than 1.5 microns or in some instances only monolayers in thickness, air oxidation can be employed. In such case, the oxide/hydroxide can be formed upon standing at room temperature wherein the copper surface reacts with ambient oxygen and water vapor. Other techniques for formation of the oxide/hydroxide include immersion in or exposure to an oxidative aqueous bath.

An organosilane mixture of this invention is applied as a coating either to the oxide, hydroxide or combination or to a partially cured thermosetting polymer composition, also known in the art as a prepreg or "B" stage resin. The same materials of construction as the dielectric layer can be employed for this layer which is termed an insulating layer to more readily distinguish the layers from one another. Turning to the silane which can be employed in the present invention, it is a requirement that the silane forms an adherent intermediate layer which bonds this oxide, hydroxide or combination thereof to the partially cured and converted to the fully cured insulating layer. It is a requirement that the silane functions to prevent delamination in accordance with the thermal stress test as defined herein. In a preferred mode the multilayer

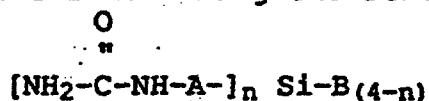
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circuit board with fully cured insulating layer meets all specifications of MIL-P-55110D.

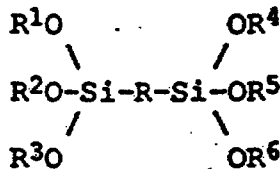
Turning to organosilane, it is considered that the ureido silane forms hydrogen bridge bonds with silanole (Si-OH)-groups of the silane and/or form covalent metal -O-Si bonds in a condensation reaction. The silanes are considered to interact with the adjacent layers through a functionally substituted organic group to provide van der Waals force interaction, strong polar force/hydrogen bridge interaction, or covalent bond formation with the dielectric resin. It is considered that the disilyl crosslinking agent forms a network with the ureido silane to reduce the moisture sensitivity of the resulting adherent organosilane layer.

The moisture resistant, adherent, organosilane layers of this invention are prepared from a silane bonding mixture which has as its essential components (I) at least one ureido silane having the structure:



where A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 2 or 3, B need not be identical; and

(II) a disilyl crosslinking agent having the structure



wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms.

Preferably in Formula I each B group is identical if more than one B group is present. Also preferably R^1 , R^2 , R^3 , R^4 , R^5 and R^6 are identical. In the ureido silane (I), the alkylene group, A, preferably is a
5 divalent ethylene or propylene and the alkoxy group, B, preferably is a methoxy or ethoxy group. A particularly preferred ureido silane is gamma-ureidopropyl-triethoxy-silane. In the disilyl crosslinking agent (II), the
10 alkyl group preferably is methyl or ethyl and the alkylene group, R, preferably is a divalent ethylene or propylene group. A particularly preferred disilyl crosslinking agent is hexamethoxydisilylethane.

The component concentrations of the silane bonding mixture may vary widely to meet the needs of a
15 particular application. Thus the weight ratio of the ureido silane (I) to the disilyl crosslinking agent (II) may be between 99:1 and 1:99. Preferably the weight ratio of (I):(II) is between 90:10 and 10:90 and more preferably is between 90:10 and 70:30. Typically a
20 single ureido silane is used with a single disilyl crosslinking agent, however, it is within the scope of this invention to use in the silane bonding mixture, two or more ureido silanes as defined and/or two or more disilyl crosslinking agents as defined.

25 In the practice of this invention the silane bonding mixtures may be applied as a liquid solution to the tin hydroxide/oxide surface or insulating layer surface. In this instance the silane bonding mixture contains a mutual solvent for the ureido silane and the
30 disilyl crosslinking agent. The solution is applied by any conventional means, e.g., by dipping, spraying, brushing, immersion, etc.

The immersion metal coatings disclosed in European Patent Application 88115951.1 supra, European Patent
35 216,531 as well as U.S. Patent 4,657,632 are directly

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useful in the present invention for initial bonding to the copper circuitry. These publications are incorporated by reference herein. However, it is considered that the immersion tin coatings are

5 insufficient to form a direct bond between the electrically conductive layer copper surface and a dielectric material since delamination can occur particularly due to thermal stress. The organosilane has the ability to increase the bond strength. A

10 preferred coating composition contains a thiourea compound, a tin salt, a reducing agent, an acid and a urea compound. In accordance with the teachings of these prior art publications a urea compound is necessary. However a urea compound is not necessary

15 with an organosilane layer. Therefore it is directly within the scope of the present invention that wherever the term urea compound is present in reference to the above publications it can be deleted. Therefore similar formulations can be deleted directly employed as

20 disclosed in these publications except the urea compound can be omitted. In a preferred embodiment the urea will be present.

Since in a preferred embodiment compositions which employ a thiourea compound, a tin salt, a reducing

25 agent, an acid and a urea compound, pertinent disclosure for these publications is reproduced herein.

The tin salt preferably comprises a stannous salt. Although stannous salts of an inorganic (mineral) acid or organic acid may be used (e.g., stannous formate,

30 stannous acetate and the like) the tin salt may comprise a stannous salt of a mineral acid such as the sulfur, phosphorous, and halogen acids, especially the sulfur acids such as sulfuric acid or sulfamic acid. Alkali metal stannates may also be used such as sodium or

35 potassium stannate and the art known equivalents



thereof. In one embodiment stannous sulfate, stannous sulfamate or stannous acetate is used as the tin salt. Where tin lead coatings are deposited, lead acetate may be used as the lead salt.

5 The acids that are employed may be organic acids or inorganic acids (mineral acids) based on sulfur, phosphorous, or the halogens, the sulfur based mineral acids being preferred such as sulfuric acid or sulfamic acid. Some of the organic acids that may be employed
10 comprise monocarboxylic or dicarboxylic acids having up to about six carbon atoms such as formic acid, acetic acid, malic acid, maleic acid, and the like.

It is preferred, if possible not to use halogen acids or halogen salts since halide residues will be
15 produced in the tin coating deposited, these salts interfering with the electrical properties of the tin and may also act as corrosive materials in the coating.

The chelating agents that may be employed generally comprise the various classes of chelating agents and
20 specific compounds disclosed in Kirk-Othmer, Encyclopedia of Chemical Technology, Third Edition, Volume 5, pages 339-368 incorporated herein by reference. Chelating agents that are especially preferred comprise the aminocarboxylic acids and the
25 hydroxycarboxylic acids. Some specific aminocarboxylic acids that may be employed in this respect comprise ethylenediaminetetraacetic acid, hydroxyethyl-ethylenediaminetriacetic acid, nitrilotriacetic acid, N-dihydroxyethylglycine, and ethylenebis(hydroxy-
30 phenylglycine). Hydroxy carboxylic acids that may be employed comprise tartaric acid, citric acid, gluconic acid and 5-sulfosalicylic acid.

The various reducing agents that may be employed are well known in the art and generally comprise organic
35 aldehyde whether saturated or unsaturated, aliphatic or



cyclic, having up to about ten carbon atoms. Lower alkyl aldehydes having up to about six carbon atoms may be employed in this respect such as formaldehyde, acetaldehyde, propionaldehyde, butyraldehyde, and the like. Especially preferred aldehydes comprise hydroxy aliphatic aldehydes such as glyceral-dehyde; erythrose; threose; arabinose and the various position isomers thereof and glucose and the various position isomers thereof. Glucose has been found to act to prevent oxidation of the metal salts to a higher oxidation state, e.g., SnII to SnIV, but also as a chelating agent and is especially useful for these reasons.

The surfactants that may be employed comprise any non-ionic, anionic, cationic or amphoteric surfactant such as those listed in Kirk-Othmer, Encyclopedia of Chemical Technology, Third Edition, Volume 22, pp. 332-387 which is incorporated herein by reference. The non-ionic surfactants are especially preferred.

The surface area of the tin oxide/hydroxide layer to which the hydrolyzed silane is applied is a factor in the resulting bond strength. Thus high surface areas such as produced by oxidizing a copper surface to copper oxide, then hydrolyzing the oxide and conversion to tin oxide by an immersion process give a high surface area which gave the highest bond strength when bonded to polyimide after the silane treatment.

In accordance with the present invention is a requirement that the bonding of the metal layer which is generally supported by an insulating layer to a dielectric layer can withstand a solder immersion stress test as defined hereinafter relative humidity (RH) preconditioning for at least 14 hours.

After having bonded the various layers of a multilayer construction by applying pressure and heat in a lamination press holes (for electrical interconnect)



are drilled through the multilayer, typically using a numerically controlled drilling machine with multiple heads and air bearings. Such drilling operations are described, e.g., in Handbook of Printed Circuit Design, Manufacture, Components and Assembly (Chapter 4.3.2. pg. 5 254) by G. Leonida, Electrochemical Publications, 1981 and Printed Circuits Handbook (Chapter 5.8-5.12) Edited by Clyde F. Coombs, Jr., McGraw-Hill Book Co., 2nd Edition.

10 Well known techniques for hole formation and making the hole conductive can be employed herein, e.g., see Printed Circuit Technology, edited by N. S. Einarson, 1977, Chapter 7.

To further define the present invention the
15 following example is provided. In this example all parts and percentages are by weight and degrees are in Centigrade unless otherwise described. In the example, copper clad laminate or copper foil was employed as a sheet rather than processed to form circuitry. The use
20 of a copper sheet was considered to denote more reproductivity in test measurements. Also, in the example, hole drilling was not employed which likewise was considered to allow greater reproductivity to test results.

25

EXAMPLE 1

The copper surface of the test samples were chemically cleaned, treated with an immersion tin composition and a silane bonding mixture in an inline spray system, and evaluated versus an organosilane
30 coupling agent, gamma-ureidopropyl triethoxysilane, and conventional brown and black oxide.

The test samples were Norplex/OAK FR-4 epoxy laminate panels (18 inches wide, 24 inches long and 0.014 inches thick) containing 1 oz. copper on both
35 sides. Test samples of 0.0014 inch thick copper foil

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(1 oz. copper) was also processed for bond strength determinations.

The inline spray system used to prepare the sample surfaces had a conveyor speed of 4 feet per minute and
5 contained the following process steps and conditions.

			Rinse (Solution)		Spray	
			Conveyor Length	Water Flow	Temp (°F)	Pressure (PSI)
10	1.	Panel Feed (Input)	23"	---	---	---
	2.	Alkaline Cleaner	20"	---	120	25
	3.	Water Rinse	20"	5 GPM*	60	20
15	4.	Microetch	27"	---	110	25
	5.	Water Rinse	20"	5 GPM	60	20
	6.	Immersion Tin Application	48"	---	75	25
20	7.	Water Rinse (Recycle)	20"	---	110	25
	8.	Water Rinse followed by air knife drying	20"	5 GPM	60	20
25	9.	Silane Treatment	20"	---	75	25
	10.	Hot Air Dryer	30"	---	130	---
	11.	Output Conveyor	41"	---	---	---
30						

*GPM is gallons per minute

The alkaline cleaner used in the system was
35 Versaclean® 415 (Du Pont) and the microetch was

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Sureetch® 550 (Du Pont) potassium peroxy monosulfate/sulfuric acid.

In Step 6 the immersion tin composition was formed by mixing Solution A and Solution B of the following composition:

Solution A

	D.I. Water	200 ml
	Conc. H ₂ SO ₄	100 ml
10	Hypophosphorus acid (50%)	40 ml
	Stannous Sulfate	20 gms
	D.I. Water	To 0.5 liter

Solution B

	Thiourea	60 gms
15	Urea	40 gms
	D.I. Water	To 0.5 liter

Sufficient solution is prepared to adequately fill the system reservoir.

Several test solutions were prepared for use in the silane treatment Step 8.

Solution 1 is prepared by adding 57 ml of glacial acetic acid to 57 liters of deionized water. 570 grams of gamma-ureidopropyltriethoxysilane (A-1160 Union Carbide) coupling agent is then added and mixed by activating the recirculating system of the spray module. The solution is allowed to mix for 15 to 20 minutes to insure complete hydrolysis of the organosilane to an organosilane-triol. This solution is hereinafter identified as 1% A-1160.

Solution 2 is prepared as in Solution 1 but contains 0.15% of 1,2-bis(trimethoxysilyl)ethane in addition to the 1% of A-1160 and will hereinafter be identified as 1% A-1160/0.15% BIS (and as Sample A in Table 1).

Solution 3 is prepared as in Solution 1 but contains 0.20% of 1,2-bis(trimethoxysilyl)ethane in addition to the 1% of A-1160 and will hereinafter be identified as 1% A-1160/0.20% BIS (and as Sample B in Table 1).

To compare the effect of silane treatment to a commercially accepted standard, samples of FR-4 epoxy laminate and copper foil were prepared which were treated with commercial black oxide (MacDermid MAC-u-BLACK* Black Oxide) and brown oxide (Electrochemicals 499 Brown Oxide) hereinafter identified as Black Oxide and Brown Oxide respectively.

After treatment, all laminate and copper foil samples were baked at 250 to 270°F for 1 hour. This exposure was considered to simulate conditions actual laminates typically would be subjected to prior to preparation of a multilayer board. The higher temperature and time assured removal of moisture which could result in delamination during manufacturing of the multilayer boards.

Following the bake treated laminates and foils are used with prepreg sheets to prepare 8-layer multilayer composite boards. Two types of Norplex/OAK prepreg were used to prepare two sets of multilayer boards; Type 1080 contains approximately 65.5% resin content with fine weave glass cloth, and Type 7628 contains $45 \pm 5\%$ resin content with heavy weave glass cloth. The multilayer composites were prepared as follows. Each composite was assembled from 3 laminates (one inner and two outer), two outer foil sheets and 8 prepreg sheets so that two prepreg sheets are between the treated copper surfaces of each outer laminate and the adjacent copper foil sheet. Ten multilayer assemblies are stacked to form a package with each assembly being separated from the other by a 0.025 inch thick aluminum sheet. The package



is enclosed in a vacuum bag which is then evacuated to remove air and sealed. The package is then loaded and centered as rapidly as possible into a hydraulic press preheated to 190°F. The platens are closed and pressure of 25 psi is applied for 12 minutes. Then the pressure is increased to 200 psi and the temperature raised to 365°F and held for 90 minutes. While maintaining the pressure constant, the package is cooled using chilled 60°F water for 45 minutes. The pressure is then relaxed and the package removed which is then post baked for 8 hours at 324°F.

A 1/4 inch wide strip of each multilayer composite formed during the lamination is removed for bond strength determination and the remainder of the composite panel is processed through an etcher to remove the outer foil layers. The panel is then routed on an Excellion Router/Driller, Model EX-200, into 1-3/8 inch by 2-7/8 inches samples. The samples are then baked in a circulating hot air oven at 250°F for 6 hours. After cooling to room temperature the samples are placed in an environmental chamber maintained at 85°C and 85% relative humidity. Samples are removed at 4, 24, 48 and 72 hours and immersed in a 550°F molten solder bath for 20 seconds. The samples are then rated for delamination; if there is no apparent delamination the sample is designated "OK"; if there is subtle delamination or measles, the sample is designated "SLT"; and if there is gross delamination, the sample is designated "FAIL".

Bond or peel strength determinations are made on an Instron Tensile Tester, (Instron Eng. Corp., Quinsey, Mass., U.S.A.) Model TT-B with a crosshead speed of 2 inches/minute. The Instron Unit is in an environmentally controlled area at 70°F, 5°F and 50%, 10% relative humidity.

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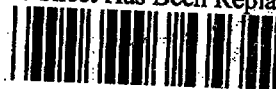


TABLE 1

THERMAL STRESS AND BOND STRENGTHS

		Bond					Strength	
		<u>Hours at 85°C/85% RH</u>						
		<u>0</u>	<u>4</u>	<u>24</u>	<u>48</u>	<u>72</u>	<u>lbs./in.</u>	
5	Sample A	1080	Prepreg	OK	OK	OK	OK	8.8
		(High Resin)						
	Sample A	7628	Prepreg	OK	OK	OK	FAIL	FAIL 8.2
		(Low Resin)						
10	Sample B	1080	Prepreg	OK	OK	OK	OK	8.0
	Sample B	7628	Prepreg	OK	OK	OK	SLT	FAIL 8.2
	1% A-1160	1080	Prepreg	OK	FAIL	FAIL	FAIL	FAIL 8.4
	1% A-1160	7628	Prepreg	OK	FAIL	FAIL	FAIL	FAIL 7.6
	Black Oxide	1080	Prepreg	OK	OK	OK	FAIL	OK 3.5
15	Black Oxide	7628	Prepreg	OK	OK	OK	SLT	SLT 5.0
	Brown Oxide	1080	Prepreg	OK	OK	OK	FAIL	FAIL 5.9;
	Brown Oxide	7628	Prepreg	OK	OK	OK	FAIL	FAIL 7.1

Sample A is 1% A-1160/0.15% BIS

20 Sample B is 1% A-1160/0.20% BIS

25 Test data in Table 1 clearly show the dramatic improvement in moisture insensitivity when the bonding mixture of A-1160 (i.e., gamma-uriedopropyltriethoxy-silane) and BIS (i.e., 1,2-bis(trimethoxysilyl)ethane). Results are comparable to commercially acceptable black oxide treatment and better than brown oxide while maintaining the high bond strength of the simple silane treatment.

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WHAT IS CLAIMED IS:

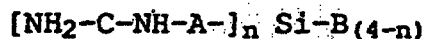
1. A process for forming a multilayer printed circuit board containing conductive through-holes which make electrical connections to a series of electrically conducting layers through several insulating layers comprising the steps of:

(a) forming electrically conductive copper circuitry on a surface of a dielectric layer support with the circuitry having a thickness of at least 4
10 microns;

(b) forming on the copper circuitry a layer of an oxide, hydroxide or combination thereof of tin by application of tin to the copper circuitry whereby during application or subsequent thereto the applied tin
15 is converted on its surface to the oxide, hydroxide or combination thereof with the proviso that the layer of oxide, hydroxide or combination is not greater than 1.5 mils in thickness;

(c) applying a silane bonding mixture to the
20 surface of the oxide, hydroxide or combination thereof formed in step (b) or an insulating layer to be bonded to the copper circuitry to form an adherent organosilane coating thereon, the insulating layer comprising a partially cured thermosetting polymer composition and
25 the silane bonding mixture consisting essentially of:

(I) a ureido silane having the structure

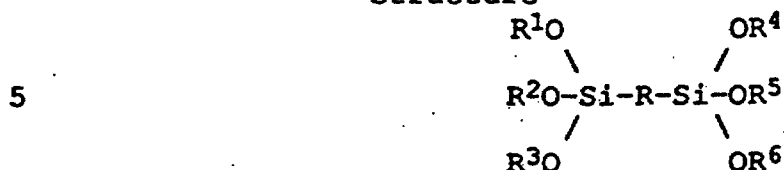


30 wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or
35 2, each B need not be identical; and

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(II) a disilyl crosslinking agent having the structure



wherein R^1 , R^2 , R^3 , R^4 , R^5 and R^6 independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

(d) repeating steps (a), (b) and (c);

(e) bonding materials formed by steps (a), (b), (c) and (d) into a single article whereby an organosilane coating is between a layer of the oxide, hydroxide or combination and an insulating layer whereby during bonding the partially cured insulating layer is cured;

(f) forming a number of holes through the bonded article formed in step (e);

(g) metallizing walls of the through-hole to form electrically conductive paths from opposite openings of the through-hole to form a multilayer circuit board with the proviso that the multilayer printed circuit board will not delaminate upon exposure to thermal stress at 550°F for 10 seconds after baking at 250°F for 6 hours and then pre-conditioning at 85°C and 85% relative humidity for twenty-four (24) hours.

2. The process of claim 1 wherein steps (a) to (d) include two insulating layers wherein a dielectric layer contacts directly or through an adhesive or insulating layer.

3. The process of claim 1 wherein steps (a) to (d) comprise one insulating layer supporting a layer of copper circuitry.





4. The process of claim 1 wherein the dielectric layer contains copper circuitry on two opposite surfaces.

5. The process of claim 1 in which the tin is applied by an immersion process.

6. The process of claim 1 in which the dielectric layer contains glass epoxy or polyimide.

7. The process of claim 1 in which the circuit board will not delaminate upon exposure at 550°F for 60 seconds.

8. The process of claim 1 wherein the silane bonding mixture further contains a mutual solvent for the ureido silane and the disilyl crosslinking agent.

9. The process of claim 1 wherein the weight ratio of (I):(II) in the silane bonding mixture is between 99:1 and 1:99.

10. The process of claim 9 wherein the weight ratio of (I):(II) is between 90:10 and 10:90.

11. The process of claim 9 wherein the weight ratio of (I):(II) is between 90:10 and 70:30.

12. The process of claim 1 wherein A is a divalent ethylene or propylene group.

13. The process of claim 1 wherein B is a methoxy or ethoxy group.

14. The process of claim 1 wherein the ureido silane is gamma-ureidopropyl-triethoxy-silane.

15. The process of claim 1 wherein R denotes a methoxy or ethoxy group.

16. The process of claim 1 wherein R' denotes a divalent ethylene or propylene group.

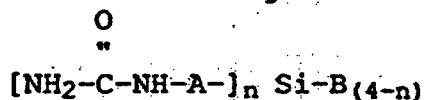
17. The process of claim 1 wherein the disilyl crosslinking agent is hexamethoxydisilylethane.

18. A silane bonding mixture for forming a moisture resistant multilayer circuit board consisting essentially of:



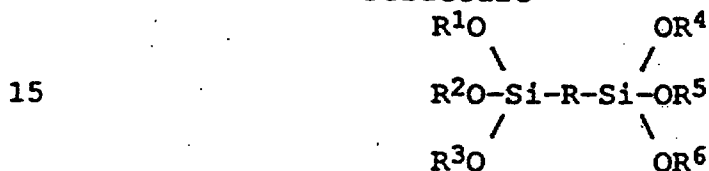


(I) a ureido silane having the structure



5 wherein A is an alkylene having 1 to 8
carbon atoms, B is a hydroxy or an alkoxy
having 1 to 8 carbon atoms and n is an
integer of 1, 2, or 3 with the proviso
that if n is 1 or 2, each B need not be
10 identical; and

(II) a disilyl crosslinking agent having the
structure



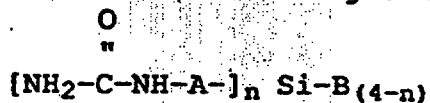
15 wherein R¹, R², R³, R⁴, R⁵ and R⁶
independently of the other is an alkyl
with 1 to 8 carbon atoms and where R
denotes an alkylene group having 1 to 8
20 carbon atoms.

19. A multilayer printed circuit board containing
conductive through-holes which make electrical
25 connections to a series of electrically conducting
layers through several insulating layers comprising:

- (a) a dielectric layer;
- (b) copper circuitry having a thickness of at
least 4 microns;
- 30 (c) a layer of an oxide, hydroxide or
combination thereof of tin metal of a thickness not
greater than 1-5 mils which overlies the tin;

(d) an organosilane layer formed from a
silane bonding mixture consisting essentially of:

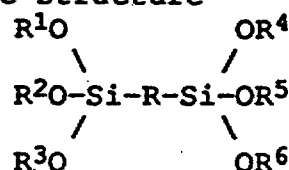
35 (I) a ureido silane having the structure





wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2, each B need not be identical; and

(II) a disilyl crosslinking agent having the structure



wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

- (e) an insulating layer comprising a cured thermosetting polymer composition;
 - (f) a dielectric layer;
 - (g) copper circuitry having a thickness of at least 4 microns;
 - (h) a layer of an oxide, hydroxide or combination thereof of tin of a thickness not greater than 1-5 mils which overlies the tin;
 - (i) an organosilane layer formed from the silane bonding mixture;
 - (j) an insulating layer comprising a cured thermosetting polymer composition;
- with the proviso that the multilayer printed circuit board will not delaminate upon exposure to thermal stress of solder immersion at 550°F for 10 seconds after baking at 250°F for 6 hours and then pre-conditioning at 850°C and 85% relative humidity for twenty-four hours.

20. A multilayer printed circuit board containing conductive through-holes which make electrical

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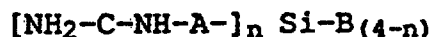




connections to a series of electrically conducting layers through several insulating layers comprising:

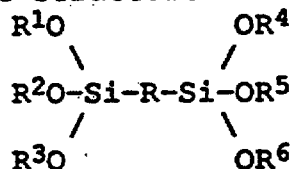
- (a) a dielectric layer;
- (b) copper circuitry having a thickness of at least 4 microns;
- (c) a layer of an oxide, hydroxide or combination thereof of tin of a thickness not greater than 1-5 mils which overlies tin;
- (d) an organosilane layer formed from a silane bonding mixture consisting essentially of:

(I) a ureido silane having the structure



wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2, each B need not be identical; and

(II) a disilyl crosslinking agent having the structure



wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

- (e) an insulating layer comprising a cured thermosetting polymer composition;
- (f) an organosilane layer formed from the silane bonding mixture;





(g) a layer of an oxide, hydroxide or combination thereof of tin of a thickness not greater than 1-5 mils which overlies the tin;

(h) copper circuitry having a thickness of at least 4 microns;

(i) a dielectric layer;
with the proviso that the multilayer printed circuit board will not delaminate upon exposure to thermal stress of solder immersion at 350°F for 10 seconds after baking at 250°F for 6 hours and then pre-conditioning at 85°C and 85% relative humidity for twenty-four (24) hours.

21. A multilayer printed circuit board containing conductive through-holes which make electrical connections to a series of electrically conducting layers through several insulating layers comprising:

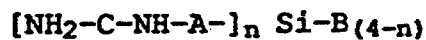
(a) a dielectric layer;

(b) copper circuitry having a thickness of at least 4 microns;

(c) a layer of an oxide, hydroxide or combination thereof of tin of a thickness not greater than 1-5 mils which overlies the in;

(d) an organosilane layer formed from a silane bonding mixture consisting essentially of:

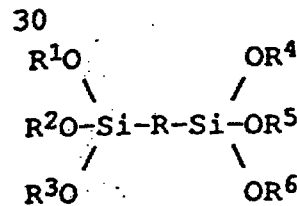
(I) a ureido silane having the structure



wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2, each B need not be identical; and

(II) a disilyl crosslinking agent having the structure





wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

(e) an insulating layer comprising a cured thermosetting polymer composition;

(f) copper circuitry having a thickness of at least 4 microns;

(g) a layer of an oxide, hydroxide or combination thereof of tin of a thickness not greater than 1-5 mils which overlies the tin;

(h) an organosilane layer formed from the silane bonding mixture;

(i) an insulating layer comprising a cured thermosetting polymer composition; with the proviso that the multilayer printed circuit board will not delaminate upon exposure to thermal stress of solder immersion at 550°F for 10 seconds after baking at 250°F for 6 hours and then pre-conditioning at 85°C and 85% relative humidity for twenty-four (24) hours.

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TITLE

MULTILAYER PRINTED CIRCUIT BOARD FORMATION

ABSTRACT

- 5 Multilayer printed circuit boards having a number of through-holes are formed employing intermediate layers in bonding copper circuitry to an insulating layer.

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TITLEMULTILAYER PRINTED CIRCUIT BOARD FORMATIONBACKGROUND OF THE INVENTION

The present invention is directed to a process of forming multilayer printed circuit boards, multilayer printed circuit boards obtainable thereby and a silane bonding mixture used therein.

Multilayer PCB's are typically constructed by interleaving imaged conductive layers such as one containing copper with dielectric layers such as a partially cured B-stage resin, i.e., a prepreg, into a multilayer sandwich which is then bonded together by applying heat and pressure. Since a conductive layer with a smooth copper surface does not bond well to the prepreg, rough copper surfaces have been employed to obtain a better bond to a dielectric. Therefore, a portion of the multilayer PCB industry applies a mechanical roughening process step to assure better bonding. However, as circuit patterns get finer, there is an increasing risk of physically damaging the conductor traces during this surface preparation.

Another process employed by the industry to improve bonding between the conductive layer and the dielectric are various copper surface oxidation procedures widely practiced in the plating industry to assure good interphasial adhesion.

A common drawback for all processes relying mainly on the mechanical interlocking of a rough copper surface with the dielectric is the marginal bond strength with polyimide prepreg and the fact that there is no flexible bonding interphase to absorb the stresses originating from the different thermal expansion coefficients of copper and dielectric which can cause thermal shock failures.

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☒ Claim(s)	: paged 23 to paged 25
☐ Drawing(s)	: paged to paged
☒ Abstract	: paged 21 to paged 22
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surface oxide which gets removed prior to bonding, leaving a copper surface with roughness and bonding characteristics comparable to the oxide surface. Nakaso et al. (WCIV-10) describe the formation of a rough
5 conductive layer surface by forming an electroless copper deposit on the conductive layer for better bonding. Silanes, deposited on this clean metallic copper surface are reported to yield a marginal increase in bond strength.

10 Likewise, U.S. Patent 3,508,983 discloses the use of gamma-amino propyl triethoxysilane to bond copper to a polyester base adhesive in the manufacture of a printed circuit board. This reference emphasizes the point that copper oxide should be removed prior to the
15 silane treatment to affect good bonding.

U.S. Patent 4,499,152 discloses formation of a metal laminate with utility of high resolution printed circuit patterns. The laminate preferably contains a resin-bonded, glass reinforced substrate, a layer of
20 coupling agent covering and bonded to a major surface of the substrate and a layer of ultra-thin copper adjacent the layer of coupling agent, and a composite bonding layer dispersed between the copper layer and the layer of coupling agent. A disclosure class of coupling
25 agents includes organosilanes.

European Patent Application 88115951.1, published as EP-A-0,310,010 on April 5, 1989, discloses a process for forming multilayer printed circuit boards wherein a ureido silane is used to improve adhesion between tin-
30 plated copper circuitry and the cured insulating layer during subsequent soldering operations. While this process is generally effective when the resulting laminates are prebaked before soldering, in some instances when prebaking is not employed delamination
35 can occur during soldering.

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SUMMARY OF THE INVENTION

The present invention is directed to a process for forming a multilayer printed circuit board containing conductive through-holes which make electrical connections to a series of electrically conducting layers through several insulating layers comprising the steps of:

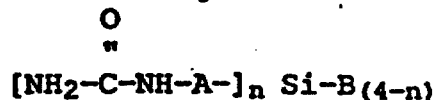
- (a) forming electrically conductive copper circuitry on a surface of a dielectric layer support with the circuitry having a thickness of at least 4 μm ;
- (b) forming on the copper circuitry a layer of an oxide, hydroxide or combination thereof of tin by application of tin to the copper circuitry whereby during application or subsequent thereto the applied tin is converted on its surface to the oxide, hydroxide or combination thereof with the proviso that the layer of oxide, hydroxide or combination is not greater than 38 μm (1,5 mils) in thickness;
- (c) applying a silane bonding mixture to the surface of the oxide, hydroxide or combination thereof formed in step (b) or to an insulating layer to be bonded to the copper circuitry to form an adherent organosilane coating thereon, the insulating layer comprising a partially cured thermosetting polymer composition;
- (d) repeating steps (a), (b) and (c);
- (e) bonding materials formed by steps (a), (b), (c) and (d) into a single article whereby an organosilane coating is between a layer of the oxide, hydroxide or combination and an insulating layer whereby during bonding the partially cured insulating layer is cured;
- (f) forming a number of holes through the bonded article formed in step (e);
- (g) metallizing walls of the through-holes to form electrically conductive paths from opposite openings of the through-holes to form a multilayer

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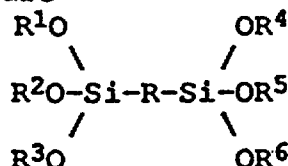
circuit board, the process being characterized in that the silane bonding mixture is consisting essentially of:

- (I) a ureido silane having the structure



wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2, each B need not be identical; and

- (II) a disilyl crosslinking agent having the structure

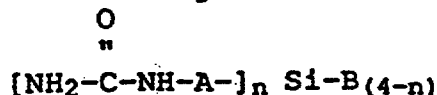


wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

so that the formed multilayer printed circuit board will not delaminate upon exposure to thermal stress at 288 °C (550 °F) for 10 seconds after baking at 121 °C (250 °F) for 6 hours and then pre-conditioning at 85 °C and 85% relative humidity for twenty-four (24) hours.

The present invention is also directed to a silane bonding mixture for forming a moisture resistant multilayer circuit board consisting essentially of:

- (I) a ureido silane having the structure



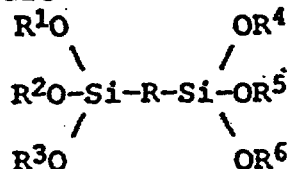
wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1,

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2, or 3 with the proviso that if n is 1 or 2 each B need not be identical; and

5 (II) a disilyl crosslinking agent having the structure



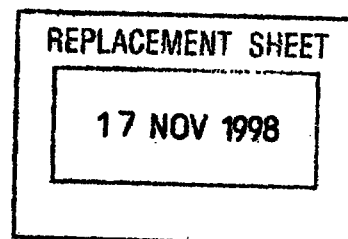
10 wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms and to circuit boards obtainable by the above process.

15 DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a process for forming a multilayer printed circuit board as defined in claim 1. The circuit board has alternating layers of dielectric material which support copper circuitry (which may have interspaced other layers such as a copper sheet which serves as a conductive ground plane) which are adhered to an insulating layer through intermediate layers. The circuit board has conductive through-holes which form electrical paths across the entire thickness of the board.

In formation of multilayer circuit boards several dozen conductive and nonconductive layers can be employed. Also, for formation of multilayer circuit boards, it is necessary to drill holes and defects can occur due to delamination of layers in the areas immediately surrounding a hole. If a defect is present in one of the layers or if delamination occurs, generally the entire board must be scrapped. Therefore high quality in each of the steps of formation of the printed circuit board is essential for commercial production.

With the techniques, various articles can be formed. Illustratively one

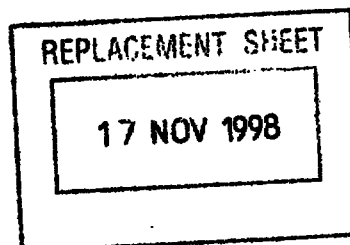


conventionally exposed to molten solder. Although the inner layers may not be exposed to the solder, they are subjected to elevated temperature. Therefore a practical test for broad commercial use to correlate whether the multilayer board can be used for general widespread commercial application is one or more tests set forth in MIL-P-55110-D.

One of the tests in MIL-P-55110-D requires thermal stress at 288°C (550°F) for 10 seconds after a pre-conditioning bake at 135-149°C (275-300°F) for two (2) hours. The specimen, i.e., the article, is visually inspected for cracking or plating, separation or plating and conductors, blistering or delamination. Laminate voids with the largest dimension of 0.08 mm (0.003 inch) or less are permitted provided the conductor spacing is not reduced below the minimum dielectric spacing, laterally or vertically. In a more preferred mode for a more stringent test, a time period of 60 seconds is employed rather than 10 seconds.

In another mode for the test procedure the final multilayer circuit board meets all applicable test procedures of MIL-P-51110D.

One reason why this test is applicable to commercial use is due to the diversity of materials employed in the multilayer construction. Although copper is the metal of choice in formation of conductive circuitry, dielectric and insulating layers (which can be of the same material with dielectric employed in the present context to refer to the initial support for a copper sheet which is formed into circuitry while insulating layer refers to another layer to which the circuitry is bonded through intermediate layers) material can drastically differ. Examples of preferred materials are epoxy and polyimide.



Although the above tests are generally useful in predicting layer bonding in printed circuit manufacture, a more rigid test is needed in the instance when multilayer circuit boards are soldered without a prior baking step to remove moisture. In such instances, delamination at the interface between the circuit and cured insulator layer may occur during soldering, presumably due to residual water or other materials which are volatilized during soldering at the interface.

- 5 baking step to remove moisture. In such instances, delamination at the interface between the circuit and cured insulator layer may occur during soldering, presumably due to residual water or other materials which are volatilized during soldering at the interface.
- 10 A useful test in accordance with this alternate procedure is a "solder immersion stress test" wherein test multilayer printed circuit test boards are first baked at 121°C (250°F) for 6 hours and then conditioned in an environmental test chamber maintained at 85°C and
- 15 85% relative humidity (RH) for 0, 4, 24, 48, and 72 hours, after which they are immersed in solder: maintained at 288°C (550°F) for 10 seconds. Each multilayer test board contains eight 100% ground planes of copper and except for the specific variation under
- 20 test, is made under the same conditions. If no subtle or gross delamination effects are observed, the board is considered acceptable and the evaluation of one group of test boards vs. others is made based on the minimum conditioning time needed before failure is observed.
- 25 The criteria of acceptability which corresponds to printed circuit manufacturing standards requires that there be no delamination after at least 24 hours conditioning time and preferably after 72 hours conditioning.

- 30 A starting material in the process of the present invention is a dielectric layer which contains on one or opposite surfaces a cladding of copper. This copper layer is of a thickness of at least 4 μm and more preferably 32 μm and it is used to form conductive
- 35 circuitry.

Well-known techniques in the prior art can be employed

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to form such circuitry such as by photoimaging technique of a photosensitive resist film followed by etching of unprotected areas of the copper. An example of a suitable technique is disclosed in U.S. Patent

5 3,469,982. The composition of the dielectric layer is not critical provided it functions as an electrical insulator. Useful support materials are disclosed in U.S. Patent 4,499,152 such as epoxy reinforced with glass fiber. Preferably a partially cured thermosetting
10 polymer composition is employed which is known in the art as a prepreg or "B" stage resin. Use of such polymer composition adds in subsequent bonding operations.

After formation of the conductive circuitry, it
15 typically is necessary to form a thin outer layer of an oxide, hydroxide or combination thereof. This layer which is of a thickness not greater than 1.5 μm and more preferably not greater than 1.0 μm can be directly formed by oxidation of the copper circuitry.
20 Well-known techniques used to form so-called "brown" or "black" oxide coatings can be employed. However major problems have been encountered due to a phenomenon known as pink ring formation whereby the oxide is dissolved or is at least partially destroyed due to later required
25 processing steps. Significant research efforts have been undertaken to solve this pink ring effect. Also in formation of oxide coatings corrosive chemicals have been employed which causes problems due to the use of harsh chemicals with special processing necessary. In
30 instances when multilayer circuit boards are soldered without a prior baking step to remove moisture, delamination at the interface between the circuit and cured insulator layer has been observed during soldering. It is theorized that residual water absorbed
35 by the laminate from the ambient environment is

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concentrated at the interface and vaporizes during soldering to cause this localized delamination.

In an embodiment of this invention a conductive layer is formed from tin. As will be more fully described below, a preferred technique of application of the coating is by immersion metal plating. The thickness of the metal layer is not critical and can be, e.g., 0.15 to 0.25 μm . During, and subsequent to, the application of tin, a thin coating of an oxide, hydroxide or combination thereof is formed. Since this coating can be extremely thin preferably not greater than 1.5 microns or in some instances only monolayers in thickness, air oxidation can be employed. In such case, the oxide/hydroxide can be formed upon standing at room temperature wherein the copper surface reacts with ambient oxygen and water vapor. Other techniques for formation of the oxide/hydroxide include immersion in or exposure to an oxidative aqueous bath.

An organosilane mixture of this invention is applied as a coating either to the oxide, hydroxide or combination or to a partially cured thermosetting polymer composition, also known in the art as a prepreg or "B" stage resin. The same materials of construction as the dielectric layer can be employed for this layer which is termed an insulating layer to more readily distinguish the layers from one another. Turning to the silane which can be employed in the present invention, it is a requirement that the silane forms an adherent intermediate layer which bonds this oxide, hydroxide or combination thereof to the partially cured and converted to the fully cured insulating layer. It is a requirement that the silane functions to prevent delamination in accordance with the thermal stress test as defined herein. In a preferred mode the multilayer

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Preferably in Formula I each B group is identical if more than one B group is present. Also preferably R^1 , R^2 , R^3 , R^4 , R^5 and R^6 are identical. In the ureido silane (I), the alkylene group, A, preferably is a
5 divalent ethylene or propylene and the alkoxy group, B, preferably is a methoxy or ethoxy group. A particularly preferred ureido silane is gamma-ureidopropyl-triethoxy-silane. In the disilyl crosslinking agent (II), the
10 alkyl group preferably is methyl or ethyl and the alkylene group, R, preferably is a divalent ethylene or propylene group. A particularly preferred disilyl crosslinking agent is hexamethoxydisilylethane.

The component concentrations of the silane bonding mixture may vary widely to meet the needs of a
15 particular application. Thus the weight ratio of the ureido silane (I) to the disilyl crosslinking agent (II) may be between 99:1 and 1:99. Preferably the weight ratio of (I):(II) is between 90:10 and 10:90 and more preferably is between 90:10 and 70:30. Typically a
20 single ureido silane is used with a single disilyl crosslinking agent, however, it is within the scope of this invention to use in the silane bonding mixture, two or more ureido silanes as defined and/or two or more disilyl crosslinking agents as defined.

25 In the practice of this invention the silane bonding mixtures may be applied as a liquid solution to the tin hydroxide/oxide surface or insulating layer surface. In this instance the silane bonding mixture contains a mutual solvent for the ureido silane and the
30 disilyl crosslinking agent. The solution is applied by any conventional means, e.g., by dipping, spraying, brushing and immersion.

The immersion metal coatings disclosed in European Patent Application 88115951.1 supra, European Patent
35 216,531 as well as U.S. Patent 4,657,632 are directly

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useful in the present invention for initial bonding to the copper circuitry. These publications are incorporated by reference herein. However, it is considered that the immersion tin coatings are
5 insufficient to form a direct bond between the electrically conductive layer copper surface and a dielectric material since delamination can occur particularly due to thermal stress. The organosilane has the ability to increase the bond strength. A
10 preferred coating composition contains a thiourea compound, a tin salt, a reducing agent, an acid and a urea compound. In accordance with the teachings of EP-A-0 216 531 and U.S. Patent 4,657,632, supra, a urea compound is necessary. However, as taught in EP-A-0
15 310 010, supra, a urea compound is not necessary with an organosilane layer. Therefore it is directly possible to delete the term urea compound from referenced formulations when used in conjunction with the silane bonding mixture disclosed herein. In a
20 preferred embodiment the urea will be present.

Since in a preferred embodiment compositions which employ a thiourea compound, a tin salt, a reducing
25 agent, an acid and a urea compound, pertinent disclosure for these publications is reproduced herein.

The tin salt preferably comprises a stannous salt. Although stannous salts of an inorganic (mineral) acid or organic acid may be used (e.g., stannous formate,
30 stannous acetate) the tin salt may comprise a stannous salt of a mineral acid such as the sulfur, phosphorous, and halogen acids, especially the sulfur acids such as sulfuric acid or sulfamic acid. Alkali metal stannates may also be used such as sodium or
35 potassium stannate and the art known equivalents

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thereof. In one embodiment stannous sulfate, stannous sulfamate or stannous acetate is used as the tin salt. Where tin lead coatings are deposited, lead acetate may be used as the lead salt.

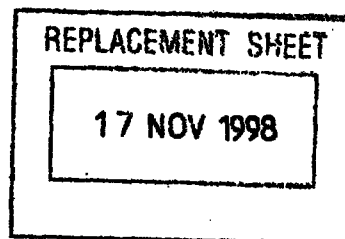
5 The acids that are employed may be organic acids or inorganic acids (mineral acids) based on sulfur, phosphorous, or the halogens, the sulfur based mineral acids being preferred such as sulfuric acid or sulfamic acid. Some of the organic acids that may be employed
10 comprise monocarboxylic or dicarboxylic acids having up to about six carbon atoms such as formic acid, acetic acid, malic acid and maleic acid.

 It is preferred, if possible not to use halogen acids or halogen salts since halide residues will be
15 produced in the tin coating deposited, these salts interfering with the electrical properties of the tin and may also act as corrosive materials in the coating.

 The chelating agents that may be employed generally comprise the various classes of chelating agents and
20 specific compounds disclosed in Kirk-Othmer, Encyclopedia of Chemical Technology, Third Edition, Volume 5, pages 339-368.

 Chelating agents that are especially preferred comprise the aminocarboxylic acids and the
25 hydroxycarboxylic acids. Some specific aminocarboxylic acids that may be employed in this respect comprise ethylenediaminetetraacetic acid, hydroxyethyl-ethylenediaminetriacetic acid, nitrilotriacetic acid, N-dihydroxyethylglycine, and ethylenebis(hydroxy-
30 phenylglycine). Hydroxy carboxylic acids that may be employed comprise tartaric acid, citric acid, gluconic acid and 5-sulfosalicylic acid.

 The various reducing agents that may be employed are well known in the art and generally comprise organic
35 aldehyde whether saturated or unsaturated, aliphatic or



cyclic, having up to about ten carbon atoms. Lower alkyl aldehydes having up to six carbon atoms may be employed in this respect such as formaldehyde, acetaldehyde, propionaldehyde, butyraldehyde, and the like. Especially preferred aldehydes comprise hydroxy aliphatic aldehydes such as glyceral-dehyde; erythrose; threose; arabinose and the various position isomers thereof and glucose and the various position isomers thereof. Glucose has been found to act to prevent oxidation of the metal salts to a higher oxidation state, e.g., SnII to SnIV, but also as a chelating agent and is especially useful for these reasons.

The surfactants that may be employed comprise any non-ionic, anionic, cationic or amphoteric surfactant such as those listed in Kirk-Othmer, Encyclopedia of Chemical Technology, Third Edition, Volume 22, pp. 332-387. The non-ionic surfactants are especially preferred.

The surface area of the tin oxide/hydroxide layer to which the hydrolyzed silane is applied is a factor in the resulting bond strength. Thus high surface areas such as produced by oxidizing a copper surface to copper oxide, then hydrolyzing the oxide and conversion to tin oxide by an immersion process give a high surface area which gave the highest bond strength when bonded to polyimide after the silane treatment.

In accordance with the present invention is a requirement that the bonding of the metal layer which is generally supported by an insulating layer to a dielectric layer can withstand a solder immersion stress test as defined hereinafter relative humidity (RH) preconditioning for at least 14 hours.

After having bonded the various layers of a multilayer construction by applying pressure and heat in a lamination press holes (for electrical interconnect)

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are drilled through the multilayer, typically using a numerically controlled drilling machine with multiple heads and air bearings. Such drilling operations are described, e.g., in Handbook of Printed Circuit Design, Manufacture, Components and Assembly (Chapter 4.3.2. pg. 254) by G. Leonida, Electrochemical Publications, 1981 and Printed Circuits Handbook (Chapter 5.8-5.12) Edited by Clyde F. Coombs, Jr., McGraw-Hill Book Co., 2nd Edition.

Well known techniques for hole formation and making the hole conductive can be employed herein, e.g., see Printed Circuit Technology, edited by N. S. Einarson, 1977, Chapter 7.

To further explain the present invention the following example is provided. In this example all parts and percentages are by weight and degrees are in Centigrade unless otherwise described. In the example, copper clad laminate or copper foil was employed as a sheet rather than processed to form circuitry. The use of a copper sheet was considered to denote more reproductivity in test measurements. Also, in the example, hole drilling was not employed which likewise was considered to allow greater reproductivity to test results.

EXAMPLE 1

The copper surface of the test samples were chemically cleaned, treated with an immersion tin composition and a silane bonding mixture in an inline spray system, and evaluated versus an organosilane coupling agent, gamma-ureidopropyl triethoxysilane, and conventional brown and black oxide.

The test samples were Norplex/OAK FR-4 epoxy laminate panels [45.7 cm (18 inches) wide, 61cm (24 inches) long and 0.36mm (0.014 inches) thick] containing 28.4 g (1 oz.) copper on both side. Test samples of 0.036 (0.0014 inch) thick copper foil

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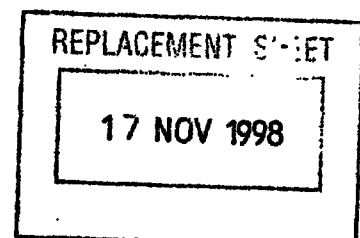
[28.4 g (1 oz.) copper] was also processed for bond strength determinations.

The inline spray system used to prepare the sample surfaces had a conveyor speed of 1.22 m (4 feet) per 5 minute and contained the following process steps and conditions.

		Conveyor Length cm (inch)	Rinse Water Flow	(Solution) Temp °C (°F)	Spray Pressure bar (PSI)
10	1. Panel Feed (Input)	58 (23)	--	-- --	-- --
	2. Alkaline Cleaner	50 (20)	--	49 (120)	1.72 (25)
	3. Water Rinse	50 (20)	5 GPM*	16 (60)	1.38 (20)
15	4. Microetch	69 (27)	--	43 (110)	1.72 (25)
	5. Water Rinse	50 (20)	5 GPM*	16 (60)	1.38 (20)
	6. Immersion Tin Application	122 (48)	--	24 (75)	1.72 (25)
20	7. Water Rinse (Recycle)	50 (20)	--	43 (110)	1.72 (25)
	8. Water Rinse followed by air knife drying	50 (20)	5 GPM*	16 (60)	1.38 (20)
25	9. Silane Treat- ment	50 (20)	--	24 (75)	1.72 (25)
	10. Hot Air Dryer	76 (30)	--	54 (130)	-- --
	11. Output Conveyor	104 (41)	--	-- --	-- --
30					

*GPM is gallons per minute; 5 GPM $\hat{=}$ 19 l/min

The alkaline cleaner used in the system was
35 Versaclean® 415 (Du Pont) and the microetch was



Solution 3 is prepared as in Solution 1 but contains 0.20% of 1,2-bis(trimethoxysilyl)ethane in addition to the 1% of A-1160 and will hereinafter be identified as 1% A-1160/0.20% BIS (and as Sample B in Table 1).

To compare the effect of silane treatment to a commercially accepted standard, samples of FR-4 epoxy laminate and copper foil were prepared which were treated with commercial black oxide (MacDermid MAC-u-BLACK* Black Oxide) and brown oxide (Electrochemicals 499 Brown Oxide) hereinafter identified as Black Oxide and Brown Oxide respectively.

After treatment, all laminate and copper foil samples were baked at 121 to 132°C (250 to 270°F) for 1 hour. This exposure was considered to simulate conditions actual laminates typically would be subjected to prior to preparation of a multilayer board. The higher temperature and time assured removal of moisture which could result in delamination during manufacturing of the multilayer boards.

Following the bake treated laminates and foils are used with prepreg sheets to prepare 8-layer multilayer composite boards. Two types of Norplex/OAK prepreg were used to prepare two sets of multilayer boards; Type 1080 contains approximately 65.5% resin content with fine weave glass cloth, and Type 7628 contains 45 ± 5% resin content with heavy weave glass cloth. The multilayer composites were prepared as follows. Each composite was assembled from 3 laminates (one inner and two outer), two outer foil sheets and 8 prepreg sheets so that two prepreg sheets are between the treated copper surfaces of each outer laminate and the adjacent copper foil sheet. Ten multilayer assemblies are stacked to form a package with each assembly being separated from the other by a 0.64 mm (0.025 inch) thick aluminium sheet.

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The package is enclosed in a vacuum bag which is then evacuated to remove air and sealed. The package is then loaded and centered as rapidly as possible into a hydraulic press preheated to 88°C (190°F). The platens
5 are closed and pressure of 1.72 bar (25 psi) is applied for 12 minutes. Then the pressure is increased to 13.8 bar (200 psi) and the temperature raised to 185°C (365°F) and held for 90 minutes. While maintaining the pressure constant, the package is cooled using chilled
10 16°C (60°F) water for 45 minutes. The pressure is then relaxed and the package removed which is then post baked for 8 hours at 162°C (324°F).

A 6.4 mm (1/4 inch) wide strip of each multilayer composite formed during the lamination is removed for
15 bond strength determination and the remainder of the composite panel is processed through an etcher to remove the outer foil layers. The panel is then routed on an Excellion Router/Driller, Model EX-200, into 3.5cm (1-3/8 inch) by 7.3cm (2-7/8 inches) samples.
20 The samples are then baked in a circulating hot air oven at 121°C (250°F) for 6 hours. After cooling to room temperature the samples are placed in an environmental chamber maintained at 85°C and 85% relative humidity. Samples are removed at 4, 24, 48
25 and 72 hours and immersed in a 288°C (550°F) molten solder bath for 20 seconds. The samples are then rated for delamination; if there is no apparent delamination the sample is designated "OK"; if there is subtle delamination or measles, the sample is designated "SLT"; and if there is gross delamination, the sample is designated "FAIL".

30 Bond or peel strength determinations are made on an Instron Tensile Tester, (Instron Eng. Corp., Quinsey, Mass., U.S.A.) Model TT-B with a crosshead speed of 5.1 cm/min (2 inches/minute). The Instron Unit is in an environmentally controlled area at 21°C (70°F), -15°C
35 (5°F) and 50%, 10% relative humidity.

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TABLE 1

THERMAL STRESS AND BOND STRENGTHS

		<u>Hours at 85°C/85% RH</u>						<u>Bond Strength</u>		
		<u>0</u>	<u>4</u>	<u>24</u>	<u>48</u>	<u>72</u>	<u>kg/cm</u>	<u>(lbs./in.)</u>		
5	Sample A	1080	Prepreg	OK	OK	OK	OK	OK	1.57	(8.8)
	(High Resin)									
	Sample A	7628	Prepreg	OK	OK	OK	FAIL	FAIL	1.46	(8.2)
	(Low Resin)									
10	Sample B	1080	Prepreg	OK	OK	OK	OK	OK	1.43	(8.0)
	Sample B	7628	Prepreg	OK	OK	OK	SLT	FAIL	1.46	(8.2)
	1% A-1160	1080	Prepreg	OK	FAIL	FAIL	FAIL	FAIL	1.50	(8.4)
	1% A-1160	7628	Prepreg	OK	FAIL	FAIL	FAIL	FAIL	1.36	(7.6)
	Black Oxide	1080	Prepreg	OK	OK	OK	FAIL	OK	0.63	(3.5)
15	Black Oxide	7628	Prepreg	OK	OK	OK	SLT	SLT	0.89	(5.0)
	Brown Oxide	1080	Prepreg	OK	OK	OK	FAIL	FAIL	1.05	(5.9)
	Brown Oxide	7628	Prepreg	OK	OK	OK	FAIL	FAIL	1.27	(7.1)

Sample A is 1% A-1160/0.15% BIS

20 Sample B is 1% A-1160/0.20% BIS

Test data in Table 1 clearly show the dramatic improvement in moisture insensitivity when the bonding mixture of A-1160 (i.e., gamma-uriedopropyltriethoxy-silane) and BIS (i.e., 1,2-bis(trimethoxysilyl)ethane). Results are comparable to commercially acceptable black oxide treatment and better than brown oxide while maintaining the high bond strength of the simple silane treatment.

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WHAT IS CLAIMED IS:

1. A process for forming a multilayer printed circuit board containing conductive through-holes which make electrical connections to a series of electrically conducting layers through several insulating layers comprising the steps of:

(a) forming electrically conductive copper circuitry on a surface of a dielectric layer support with the circuitry having a thickness of at least 4 μm ;

10

(b) forming on the copper circuitry a layer of an oxide, hydroxide or combination thereof of tin by application of tin to the copper circuitry whereby during application or subsequent thereto the applied tin is converted on its surface to the oxide, hydroxide or combination thereof with the proviso that the layer of oxide, hydroxide or combination is not greater than 38 μm (1,5 mils) in thickness;

(c) applying a silane bonding mixture to the surface of the oxide, hydroxide or combination thereof formed in step (b) or to an insulating layer to be bonded to the copper circuitry to form an adherent organosilane coating thereon, the insulating layer comprising a partially cured thermosetting polymer composition;

25

(d) repeating steps (a), (b) and (c);

(e) bonding materials formed by steps (a), (b), (c) and (d) into a single article whereby an organosilane coating is between a layer of the oxide, hydroxide or combination and an insulating layer whereby during bonding the partially cured insulating layer is cured;

(f) forming a number of holes through the bonded article formed in step (e);

35

(g) metallizing walls of the through-holes to form electrically conductive paths from opposite openings of the through-holes to form a multilayer

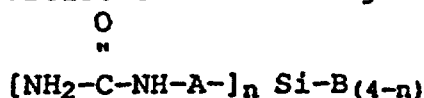
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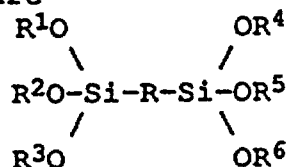
circuit board, the process being characterized in that the silane bonding mixture is consisting essentially of:

- (I) a ureido silane having the structure



wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2, each B need not be identical; and

- (II) a disilyl crosslinking agent having the structure

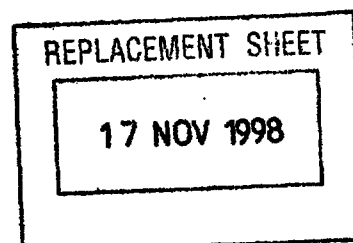


wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms;

so that the formed multilayer printed circuit board will not delaminate upon exposure to thermal stress at 288 °C (550 °F) for 10 seconds after baking at 121 °C (250 °F) for 6 hours and then pre-conditioning at 85 °C and 85 % relative humidity for twenty-four (24) hours.

2. The process of claim 1 wherein steps (a) to (d) include forming two insulating layers wherein a dielectric layer contacts directly, or through an adhesive, the second insulating layer.

3. The process of claim 1 wherein steps (a) to (d) comprise forming one insulating layer supporting a layer of copper circuitry.





4. The process of claim 1 wherein the dielectric layer contains copper circuitry on two opposite surfaces.

5. The process of claim 1 in which the tin is applied by an immersion process.

6. The process of claim 1 in which the dielectric layer contains glass epoxy or polyimide.

7. The process of claim 1 in which the circuit board will not delaminate upon exposure at 288 °C (550 °F) for 60 seconds.

8. The process of claim 1 wherein the silane bonding mixture further contains a mutual solvent for the ureido silane and the disilyl crosslinking agent.

9. The process of claim 1 wherein the weight ratio of (I):(II) in the silane bonding mixture is between 99:1 and 1:99.

10. The process of claim 9 wherein the weight ratio of (I):(II) is between 90:10 and 10:90.

11. The process of claim 9 wherein the weight ratio of (I):(II) is between 90:10 and 70:30.

12. The process of claim 1 wherein A is a divalent ethylene or propylene group.

13. The process of claim 1 wherein B is a methoxy or ethoxy group.

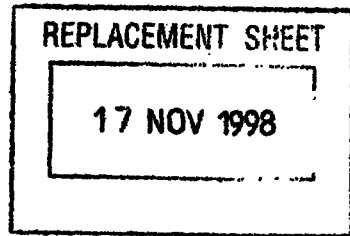
14. The process of claim 1 wherein the ureido silane is gamma-ureidopropyl-triethoxy-silane.

15. The process of claim 1 wherein R denotes a methoxy or ethoxy group.

16. The process of claim 1 wherein R' denotes a divalent ethylene or propylene group.

17. The process of claim 1 wherein the disilyl crosslinking agent is hexamethoxydisilylethane.

18. A silane bonding mixture for forming a moisture resistant multilayer circuit board consisting essentially of:



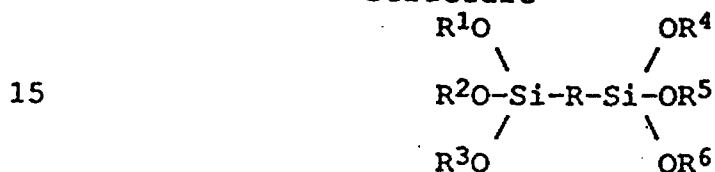


(I) a ureido silane having the structure



5 wherein A is an alkylene having 1 to 8 carbon atoms, B is a hydroxy or an alkoxy having 1 to 8 carbon atoms and n is an integer of 1, 2, or 3 with the proviso that if n is 1 or 2, each B need not be identical; and

10 (II) a disilyl crosslinking agent having the structure



15 wherein R¹, R², R³, R⁴, R⁵ and R⁶ independently of the other is an alkyl with 1 to 8 carbon atoms and where R denotes an alkylene group having 1 to 8 carbon atoms.

19. A multilayer printed circuit board obtainable by a process according to any claims 1-17 and containing
25 conductive through-holes which make electrical connections to a series of electrically conducting layers through several insulating layers, wherein the multilayer printed circuit board will not delaminate upon exposure to thermal stress of solder immersion at
30 288 °C (550 °F) for 10 seconds after baking at 121 °C (250 °F) for 6 hours and then pre-conditioning at 85 °C and 85% relative humidity for twenty-four hours.

20. The multilayer printed circuit board according to claim 19 comprising the following layers

- 35 (a) a dielectric layer;
(b) copper circuitry having a thickness of at least 4 μm;
(c) a layer of an oxide, hydroxide or combination thereof of tin metal of a thickness not greater than 0.025-0.127 mm (1-5 mils) which overlies the tin;

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(d) an organosilane layer formed from the silane bonding mixture as defined in claim 18;

(e) an insulating layer comprising a cured thermosetting polymer composition;

5 (f) a dielectric layer;

(g) copper circuitry having a thickness of at least 4 μm ;

(h) a layer of an oxide, hydroxide or combination thereof of tin a thickness not greater than 0.025-0.127 mm (1-5 mils) which overlies the tin;

10 (i) an organosilane layer formed from the silane bonding mixture as defined in claim 18; and

(j) an insulating layer comprising a cured thermosetting polymer composition.

21. The multilayer printed circuit board according to claim 19 comprising the following layers

(a) a dielectric layer;

20 (b) copper circuitry having a thickness of at least 4 μm ;

(c) a layer of an oxide, hydroxide or combination thereof of tin a thickness not greater than 0.025-0.127 mm (1-5 mils) which overlies the tin;

25 (d) an organosilane layer formed from the silane bonding mixture as defined in claim 18;

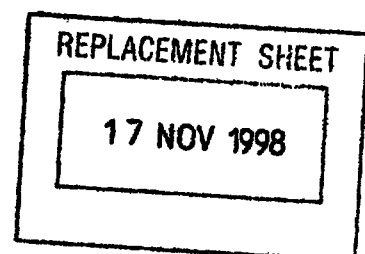
(e) an insulating layer comprising a cured thermosetting polymer composition;

(f) an organosilane layer formed from the silane bonding mixture as defined in claim 18;

30 (g) a layer of an oxide, hydroxide or combination thereof of tin of a thickness not greater than 0.025-0.127 mm (1-5 mils) which overlies the tin;

(h) copper circuitry having a thickness of at least 4 μm and;

35 (i) a dielectric layer.

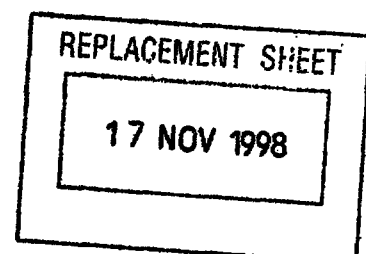




22. The multilayer printed circuit board according to claim 19 comprising the following layers:

- (a) a dielectric layer;
- (b) copper circuitry having a thickness of at
5 least 4 μm ;
- (c) a layer of an oxide, hydroxide or
combination thereof of tin of a thickness not greater
than 0.025-0.127 mm (1-5 mils) which overlies the tin;
- (d) an organosilane layer formed from the
10 silane bonding mixture as defined in claim 18;
- (e) an insulating layer comprising a cured
thermosetting polymer composition;
- (f) copper circuitry having a thickness of at
least 4 μm ;
- 15 (g) a layer of an oxide, hydroxide or
combination thereof of tin of a thickness not greater
than 0.025-0.127 mm (1-5 mils) which overlies the tin;
- (h) an organosilane layer formed from the
silane bonding mixture as defined in claim 18; and
- 20 (i) an insulating layer comprising a cured
thermosetting polymer composition.

25



TITLE

MULTILAYER PRINTED CIRCUIT BOARD FORMATION

ABSTRACT

- 5 Multilayer printed circuit boards having a number of through-holes are formed employing intermediate layers in bonding copper circuitry to an insulating layer.

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