

BICMOS CIRCUIT WITH NEGATIVE V_{BE} PROTECTIONFIELD OF THE INVENTION

The present invention relates to the field of integrated circuits which combine bipolar and complementary metal-oxide semiconductor (CMOS) devices on the same substrate.

BACKGROUND OF THE INVENTION

In recent years, much effort has been directed toward developing digital logic circuits which combine bipolar and CMOS technologies in a single integrated circuit. The combination of bipolar and CMOS technologies is particularly advantageous since the superior aspects of each may be exploited to yield optimal circuit performance.

For example, CMOS circuits have the advantages of extremely low quiescent power consumption, rail to rail output capability, high density, and a very high input impedance. Bipolar logic circuits, on the other hand, are useful in driving large capacitive loads, have fast switching capabilities, and feature better performance over temperature and power supply. These attributes have led to the development of a family of BiCMOS inverting logic circuits which employ bipolar transistors to drive output loads, while utilizing CMOS devices to perform the basic logic functions.

One problem with bipolar devices is that they suffer from a reliability problem when the voltage across the base and emitter junction (V_{BE}) is negative. This reliability problem typically results in creation of base-emitter leakage current that is a function of negative base-emitter stress voltage and stress time. This leakage current degrades the circuit performance of the bipolar transistors. For example, consider the "bare-base" buffer circuit 10 of Figure 1. If input node 11 is initially at high voltage level (e.g. +5V), bipolar transistor 12 will be on, since the base is driven by the input signal and bipolar transistor 12 is connected as an emitter follower. Also, when input node 11 is at a high voltage level, a low voltage level will result at the gate of MOS transistor

15 due to inverter 16. Transistor 15 will thus be turned off, electrically isolating output node 14 from ground V_{SS} . Output node 14 will then be at a high voltage level due to the emitter follower operation of bipolar transistor 12 with its collector coupled to the V_{DD} mode. Conversely, when input node 11 switches to a low voltage level, transistor 12 is off, preventing any current flow from V_{DD} node 13 to output node 14. Transistor 15 is on, discharging the voltage at output node 14 to ground. However, input node 11 can go low faster than output node 14 due to the delay through inverter 16 and transistor 15. When this occurs, the base-emitter voltage V_{BE} across bipolar transistor 12 will be negative (i.e. lower on the base side than the emitter side) causing the reliability voltage stress problem discussed above.

Similarly, a bipolar device cannot be used in a signal bus pre-charge circuit due to reliability problems caused by the negative V_{BE} that can develop. For example, if the circuit 20 of Figure 2 were used as a pre-charge circuit, transistor 22 would charge output node 24 so long as node 21 is at a high voltage state (logical one). This is due to the bipolar emitter follower between input node 21 and output node 24. Once the base is turned off (node 21 at a low voltage state, i.e. logical zero), a negative base-emitter voltage will result due to the remaining charge on output node 24.

What is needed is an integrated circuit combining CMOS and bipolar technologies which does not develop a negative V_{BE} during operation. Such a circuit should be implemented with a minimum device count and should retain the advantages of both bipolar and CMOS technologies discussed above. Additionally, the circuitry used to protect the base should also be capable of tri-stating the bipolar device.

SUMMARY OF THE INVENTION

A BiCMOS circuit with protection against negative base-emitter junction voltage (V_{BE}) is disclosed. The circuit includes means for discharging the base of a bipolar device through the output, rather than a first input, whenever the first input goes low. Therefore, since the base of the bipolar device is discharged through the same output as the emitter, there can never be a negative base-emitter voltage. A second input is provided which is coupled to the gates of a pair of CMOS devices. The CMOS devices are configured such that whenever the second input is low, the first input is coupled to the base of the bipolar device allowing it to turn on or off as a function of the input signal, while the coupling between the base and the output is open. Whenever the second input is high, the base of the bipolar device is coupled to the output, and the coupling between the first input and the base is open.

When used in place of a bare-base bipolar device, as a two state buffer, or as a pre-charge device, the second input is the inverted signal of the first input. The invented circuit can also be used as part of an inverting or non-inverting tri-state buffer where the first input is coupled to a "data" line, and the second input is coupled to an "enable" line. When used as a tri-state buffer, additional circuitry is disclosed which causes the output to float whenever the enable line is low.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an example of a prior art "bare-base" circuit.

Figure 2 is an example of a prior art pre-charge device.

Figure 3A shows the circuit of the present invention when used as protection against a negative V_{BE} of a bipolar transistor.

Figure 3B shows the improvement of the circuit of Figure 3A.

Figure 4 shows the circuit of Figure 3A when used in a pre-charge circuit.

Figure 5 shows the circuit of Figure 3A when used in a bare-base circuit.

Figure 6 shows the circuit of Figure 3A when used as part of a non-inverting tri-state buffer.

Figure 7 shows the circuit of Figure 3A when used as part of an inverting tri-state buffer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A BiCMOS circuit with protection against negative V_{BE} is described. In the following description, numerous specific details are set forth, such as device types, voltages, etc., in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known elements have not been shown or described to avoid unnecessarily obscuring the present invention. Additionally, although the use of this circuit is illustrated as part of a bare-base buffer circuit, as part of a pre-charge circuit and as part of an inverting and non-inverting tri-state buffer, it will be appreciated by one skilled in the art that the circuit of the present invention can be used in any type circuit requiring protection against negative V_{BE} or where a tri-state circuit device is desirable.

Referring to Figure 3A, circuit 30 shows the currently preferred embodiment of the BiCMOS circuit with negative V_{BE} protection. In the currently preferred embodiment, transistor 33 is a PMOS transistor, transistor 34 is an NPN bipolar transistor, and transistor 35 is an NMOS transistor. The gates of transistors 33 and 35 are coupled to the control line through node 36. The drain of transistor 33 is coupled to the drain of transistor 35 at node 37. In addition, the base of transistor 34 is coupled to the drain of transistor 33 at node 37. The emitter of transistor 34 is coupled to node 39. Node 39 is coupled to ground via one or more transistor devices or other circuits.

If input node 31 of Figure 3A is at a high voltage state while control node 32 is at a low voltage state, transistor 33 will be on while transistor 35 is off. This in turn will cause the input high voltage to propagate to the base of bipolar transistor 34 turning it on, creating an emitter follower between nodes 37 and 39. Node 39 is the output node of the circuit. In this case, the result of input node 31 being high while control node 32 is low is a logical high voltage state at node 39.

If input node 31 is then turned to logical low voltage state while control node 32 maintains the logical low state, node 37 is pulled to within a V_{tp} voltage

of the low voltage on node 31. Note that the V_{tp} voltage is the threshold voltage of transistor 33 which includes body effect since the source of transistor 33 is below the bulk N-WELL potential of V_{CC} . N-channel transistor 35 is turned off at this time. Therefore, a negative V_{BE} voltage can be developed, but the maximum possible negative V_{BE} is lower than the V_{CC} voltage by the V_{tp} drop.

When control node 32 receives a logical high control signal, transistor 33 is turned off and transistor 35 is turned on. At this time, if node 37 registers a logical high voltage, it is discharged through output node 39 via the turned-on transistor 35. Circuit 30 is then disabled receiving any input signal from input node 31. In this situation, node 37 is assured not to be discharged faster than the emitter of transistor 34 since it is now discharged through node 39.

Figure 3B illustrates a circuit 30A which is an improvement of circuit 30 of Figure 3A. In Figure 3B, circuit 30A is identical to circuit 30 of Figure 3A, except a P-channel transistor 35a is coupled in parallel with N-channel transistor 35. The source of transistor 35a is coupled to node 37 and the drain of transistor 35a is coupled to node 39. The gate of P-channel transistor 35a receives the control signal at node 32 via an inverter 35b. Logically speaking, transistor 35a is turned on and off by the control signal in the same manner as transistor 35.

In an alternative embodiment, N-channel transistor 35 and P-channel transistor 35a can be made of appropriate width to achieve the desired resistance between nodes 39 and 37, when transistors 35 and 35a are meant to be "on."

The purpose of providing P-channel transistor 35a in parallel with N-channel transistor 35 is to provide a better discharge path between nodes 37 and 39 when control node 32 receives a logical high control signal to turn transistor 35 on.

Because transistor 35 is an N-channel transistor, it may be turned off even if control node 32 receives the logical high control signal. When node 39 registers a voltage which is above the voltage level of the logical high control signal minus a threshold voltage V_{tn} of transistor 35, transistor 35 is turned off even if control node 32 registers the logical high control signal. The V_{tn} voltage

is the threshold voltage of an N-channel transistor. When P-channel transistor 35a is coupled in parallel with transistor 35 as shown in Figure 3B, the discharge path between nodes 37 and 39 is not broken when node 39 registers a voltage which is higher than the voltage level of the logical high control signal minus the V_{Tn} voltage of transistor 35. When node 39 experiences a voltage which is above the voltage level of the logical high control signal at control node 32 minus the V_{Tn} voltage, transistor 35 is off but transistor 35a is on, which equalizes the voltage level between nodes 37 and 39. By coupling P-channel transistor 35a in parallel with N-channel transistor 35, a CMOS switch is formed and either of or both of transistors 35 and 35a will be turned on depending on the voltage at node 39 when control node 32 register the logical high control signal.

In Figures 4-7, circuit 30 of Figure 3A is shown as part of various circuits, including as part of a pre-charge circuit (Figure 4), as part of a bare-base buffer circuit (Figure 5), as part of a non-inverting tri-state BiCMOS buffer circuit (Figure 6), and as part of an inverting tri-state BiCMOS buffer circuit (Figure 7). It shall also be noted that circuit 30A of Figure 3B can replace circuit 30 of Figure 3A to be used as part of the circuits shown in Figures 4-7.

Referring to Figure 4, the currently preferred embodiment of pre-charge circuit 40 is shown. Circuit 40 includes input node 41 and inverter 42 coupled to input node 41. In the currently preferred embodiment, input node 41 is coupled to node 31 of circuit 30, while the output of inverter 42 is coupled to node 32 of circuit 30. Output node 43 of circuit 40 is coupled to node 39 of circuit 30 and to the next stage of circuits (not shown). The use of pre-charge circuit 40 includes precharging an SRAM array, for example. The pre-charge circuit 40 can also be used to precharge register file bits. In general, precharge is a mechanism where a node is charged to a high voltage state and conditionally discharged to low or remain high. This saves the transition time it takes to generate a high voltage from a low voltage state.

If input node 41 is taken to a logical high voltage state, the output of inverter 42 will be low. In this case, transistor 33 will be on thus turning

transistor 34 on and forming an emitter follower between V_{DD} and output node 43. The low output of inverter 42 will also cause transistor 35 to be off thus isolating the base of transistor 34 from the output. The result will be to charge output node 43.

When input node 41 is taken to a logical low voltage state, the output of inverter 42 will be high, turning transistor 33 off and transistor 35 on. In this case, the base of transistor 34 will be shorted to the output through transistor 35 which is coupled to output node 43 at node 39. The circuit 40 then waits for events to happen in the next stage of the circuit to which output node 43 is coupled to discharge output node 43. Note that unlike transistor 22 of circuit 20 of Figure 2, transistor 34 of Figure 4 cannot develop a negative V_{BE} as input node 41 is switched from high to low due to the isolation of the base from input node 41 provided by transistor 33 and the shorting of the base to the output through transistor 35 when input node 41 switches from high to low.

Figure 5 shows a bare-base circuit 50 which employs circuit 30 of Figure 3A of the present invention. When input node 51 is taken high, the output of inverter 52 will be low. Node 31, coupled to node 51, will be high while node 32, coupled to the output of inverter 52, will be low. The operation of the circuit 30 portion of circuit 50 under these circumstances is identical to that described in connection with Figure 3A when node 31 is high and node 32 is low. Note that nodes 31 and 32 cannot be both at the low voltage, the case which causes some level of negative V_{BE} for Figure 3A. Node 39 will be high under these conditions. Output 55 of Figure 5 (coupled to node 39) will then be high when input node 51 is high. Note that under these conditions transistor 54, coupled to inverter 52 at node 53, will be off due to the low from inverter 52 thus isolating node 39 (and, therefore, output 55) from ground V_{SS} . Transistor 54 is an n-type MOS transistor in the currently preferred embodiment.

When node 51 is taken low, the output of inverter 52 will be high. In this case, node 31 will be low and node 32 high and the operation of the circuit 30 portion of circuit 50 will be identical to that described for these conditions in conjunction with Figure 3A. Transistors 33 and 34 will be off and transistors 35

and 54 will be on. In this case, the output, as well as the base of transistor 34, are discharged to ground V_{SS} through transistor 54. Thus, the base of transistor 34 can never be discharged faster than the output (as is the case for the bare-base circuit of Figure 1) since it is discharged through the output rather than through input node 51. Thus, a negative V_{BE} cannot develop. The circuit 50 of Figure 5 can be used as, for example, a two state non-inverting buffer.

Figure 6 shows a tri-state noninverting buffer circuit 60 which employs circuit 30 of Figure 3A of the present invention. Data node 61 is coupled to input node 31. Data node 61 is also coupled to inverter 64, the output of which is coupled to transistors 65 and 66, which are connected in parallel as a switch as shown in Figure 6. Enable node 62 couples an Enable signal to the gate of transistor 66. Enable node 62 also couples the Enable signal to inverter 63, the output of which is coupled to node 32. The output of inverter 63 is also coupled to node 67, which is further coupled to the gate of transistor 65 through node 68, and to the gate of transistor 69. The output of transistors 65 and 66 are coupled to the gate of transistor 72. In the currently preferred embodiment, transistors 66, 69, and 72 are n-type MOS transistors, and transistor 65 is a p-type MOS transistor.

When enable node 62 is high (i.e., a high Enable signal), transistor 66 is on. The output of inverter 63 is low. As a result of the low at the output of inverter 63, transistor 33 is on, transistor 35 is off, transistor 65 is on, and transistor 69 is off.

Now consider the operation of circuit 60 of Figure 6 while enable node 62 is high. If data node 61 is high, the output of inverter 64 will be low. Since transistors 65 and 66 are on, transistor 72 is off, isolating output node 70 from ground V_{SS} . Also, since transistor 33 is on, transistor 34 is turned on allowing current to flow from node 38 to output node 70 (emitter follower from node 37), resulting in a high voltage state at output node 70.

With enable node 62 still high, if data node 61 is low, node 37 is pulled down to V_{TP} from the ground V_{SS} . This causes node 37 to gradually discharge the high voltage through the drain to substrate current flowing through transistor

33. Also, while data node 61 is low, the output of inverter 64 will be high thus turning transistor 72 on (since transistors 65 and 66 are on) and thereby quickly discharging output node 70 to ground V_{SS} through transistor 72.

Thus, while enable node 62 is at a high state, output 70 will be at a high state when data node 61 is high, and at a low state when data node 61 is low (i.e. when enable = 1, output node 70 = data).

When enable node 62 is low, the output of inverter 63 will be high. Transistors 65 and 66 will be off while transistor 69 will be on. Since transistor 69 is connected to ground, node 71 will be low whenever enable node 62 is low thus turning off transistor 72 thereby isolating output node 70 from ground. Additionally, due to the high output of inverter 63, transistor 33 will be off, isolating transistor 34 from data node 61. Transistor 35 will be on, coupling the base of transistor 34 to output node 70 through transistor 35. Thus, when enable node 62 is low, output node 70 is floating.

Therefore, when enable node 62 is high, output node 70 equals data, and when enable node 62 is low, output node 70 is floating.

Figure 7 shows tri-state inverting buffer circuit 80. Circuit 80 is similar to circuit 60 of Figure 6 except that inverter 84 is placed between the data node 81 and input node 31 of circuit 30, and there is no inverter between data node 81 and the parallel transistors 85 and 86. The operation of the enable circuitry is the same in circuit 80 as in circuit 60 of Figure 6. Whenever enable node 82 is high, output node 90 will be at the same level as the output from inverter 84. Thus, output 90 will be the inverted signal of the data node 81 whenever enable node 82 is high. Whenever enable node 82 is low, output node 90 will float. Thus, when enable equals 1, out equals inverted data, and when enable equals 0, output node 90 is floating.

Thus, a BiCMOS circuit is disclosed which can be used as protection against negative V_{BE} or to tri-state a bipolar device. Illustrative uses of this circuit, including in place of a bare-base bipolar device, as a pre-charge device,

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as a two-state non-inverting buffer and as a tri-state inverting and non-inverting buffer have been shown.



CLAIMS

1. A BiCMOS circuit, comprising:
a first input node and a second input node;
an output node;
a bipolar transistor having a base, a collector coupled to a power supply, and an emitter; and
means for electrically coupling said base of said bipolar transistor to said output node whenever a low potential is applied to said first input node, said means comprising a pair of CMOS transistors comprising a first transistor and a second transistor, each having a gate, a source, and a drain, wherein said gates of said transistors are coupled to said second input node, said source of said first transistor is coupled to said first input node, said drain of said first transistor is coupled to said base of said bipolar transistor and to said drain of said second transistor, and said source of said second transistor and said emitter of said bipolar transistor are coupled to said output node, wherein said means substantially reduces a negative base-emitter voltage on said bipolar transistor.
2. The circuit as described in Claim 1, wherein said first transistor is a p-type MOS transistor and said second transistor is an n-type MOS transistor.
3. The circuit as described in Claim 2, further comprising a third transistor coupled in parallel with the second transistor, wherein the third transistor is a p-type MOS transistor, wherein the third transistor has a gate coupled to the second input node via an inverter.
4. The circuit as described in claim 1, wherein said circuit is used as a pre-charge circuit, wherein said output node is charged by said bipolar transistor when said first input is at a high state, wherein said bipolar transistor is isolated from said first input node when said first input node is at a low state,



and wherein said base of said bipolar transistor is coupled to said output node when said second input node is at a low state.

5. A BiCMOS circuit, comprising:
- a first input node;
 - an output node;
 - an inverter coupled to said first input node;
 - a bipolar transistor having a base, a collector coupled to a power supply, and an emitter coupled to said output node;

means for electrically coupling said base of said bipolar transistor to said output whenever a low potential is applied to said first input node, said means comprising a pair of CMOS transistors comprising a first and a second transistor, each of said first and second transistors having a gate, a source, and a drain, wherein the gates of said first and second transistors are coupled to an output of said inverter, said source of said first transistor is coupled to said first input node, said drain of said first transistor is coupled to said base of said bipolar transistor and to said drain of said second transistor, and said source of said second transistor and said emitter of said bipolar transistor are coupled to said output node; and

a third transistor having a gate, a source, and a drain, wherein said gate of said third transistor is coupled to said output of said inverter, said drain of said third transistor is coupled to said output node, and said source of said third transistor is coupled to ground.

6. The circuit as described in Claim 5, wherein said first transistor is a p-type MOS transistor, said second transistor is an n-type MOS transistor, and said third transistor is an n-type MOS transistor.

7. The circuit as described in claim 6, further comprising a fourth transistor coupled in parallel with the second transistor, wherein the fourth



transistor is a p-type MOS transistor, wherein the fourth transistor has a gate coupled to the first input node.

8. A BiCMOS non-inverting tri-state buffer circuit, comprising:

- a) a bipolar transistor having a base, a collector coupled to a power supply, and an emitter coupled to an output of said circuit;
- b) a first transistor having a gate coupled to a first input via a first inverter, a drain coupled to said output node, and a source coupled to ground;
- c) a second transistor having a gate coupled to a second input via a second inverter, a drain coupled to said gate of said first transistor, and a source coupled to ground;
- d) means including a third transistor having a drain coupled to said base of said bipolar transistor, a source coupled to said output node, and a gate coupled to said second input via said second inverter for coupling said base of said bipolar transistor to said output node when said second input is in a first voltage state;
- e) a fourth transistor having a drain coupled to said base of said bipolar transistor, a source coupled to said first input, and a gate coupled to said gate of said third transistor, wherein when said second input is in said first voltage state, said third transistor couples said base of said bipolar transistor to said output node, wherein when said first input is in said first voltage state and said second input is in said second voltage state, said base of said bipolar transistor assumes a voltage equal to said first voltage state plus a threshold voltage of said fourth transistor at which said fourth transistor is turned off.

9. The circuit of claim 8, wherein said first, second, and third transistors are N-channel MOS transistors and said fourth transistor is a P-channel MOS transistor.



10. The circuit of claim 9, wherein said coupling means further comprises a fifth transistor coupled in parallel with said third transistor, wherein said fifth transistor has a gate coupled to said second input, wherein said fifth transistor is a P-channel MOS transistor.

11. The circuit of claim 8, wherein said first voltage state is a logical low voltage and said second voltage state is a logical high voltage.

12. The circuit of claim 8, wherein said first input is a data input and said second input is a control input.

13. A BiCMOS inverting tri-state buffer circuit, comprising:

a) a bipolar transistor having a base, a collector coupled to a power supply, and an emitter coupled to an output of the circuit;

b) a first transistor having a gate coupled to a first input, a drain coupled to said output node, and a source coupled to ground;

c) a second transistor having a gate coupled to a second input via a first inverter, a drain coupled to said gate of said first transistor, and a source coupled to ground;

d) means having a third transistor having a drain coupled to said base of said bipolar transistor, a source coupled to said output node, and a gate coupled to said second input via said first inverter for coupling said base of said bipolar transistor to said output node when said second input is in a first voltage state;

e) a fourth transistor having a drain coupled to said base of said bipolar transistor, a source coupled to said first input via a second inverter, and a gate coupled to said gate of said third transistor, wherein when said second input is in said first voltage state, said third transistor couples said base of said bipolar transistor to said output node, wherein when said first input is in a second voltage state and said second input is in said second voltage state, said base of said bipolar transistor assumes a voltage equal to said first voltage state



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plus a threshold voltage of said fourth transistor at which said fourth transistor is turned off.

14. The circuit of claim 13, wherein said first, second, and third transistor are N-channel MOS transistors and said fourth transistor is a P-channel MOS transistor.

15. The circuit of claim 13, wherein said first voltage state is a logical low voltage and said second voltage state is a logical high voltage.

16. The circuit of claim 13, wherein said first input is a data input and said second input is a control input.

17. The circuit of claim 14, wherein said coupling means further comprises a fifth transistor coupled in parallel with said third transistor, wherein said fifth transistor has a gate coupled to said second input, wherein said fifth transistor is a P-channel MOS transistor.

18. A BICMOS circuit, substantially as hereinbefore described with reference to the accompanying drawings.