

The invention relates to a process and a device for synchronising digital information signals as described in the preamble of Claims 1 and 10.

In the transmission of information items, signals are taken from an information source and fed to a transducer by which the signals are converted into electrical signals. The electrical signals are passed on to a transmitting device by which the signals are modulated. Via a data transmission channel the modulated signals are fed to a receiving device. In the receiving device the signals are demodulated and fed to a transducer which renders the data perceptible to an information sink. In the case of the transmission of digital signals, at the receiving end the digital signals are processed in the transducer by a decoder.

A transmission process of this kind has been described in the "NTZ" Edition 36 (1983) No. 11. Here, with the assistance of phase shift keying, the signals are transmitted from a satellite to a receiver and are decoded in the receiver. Data words in an error-correctable code and synchronising words are transmitted. In the synchronisation, when successive synchronising words have been recognised a switch-over is made from a build-up process to continuous operation in a steady state. In a time window the error rate of the synchronising word is checked. In dependence upon the error rate of the synchronising word, it is decided whether a new build-up process must be initiated to find a synchronising word in another time period. "Tuning" is to be understood in that the error rate of the synchronising word is allowed to remain at such a level that only in the case of no longer correctable transmission errors or total failure is a new build-up process started. This is disadvantageous inasmuch as a relationship must be established between disturbed synchronising words and disturbed data words, and this relationship must be tuned in such manner that the error rate in the synchronising word is assessed as being too high only when the decoding of the data word also does not result in utilizable signals.

The aim of the invention is to improve upon the synchronising process; in particular synchronising words are to be spared, the effective time for data words is to be extended and the signal-to-noise ratio is to be increased.

This aim is fulfilled by the measure described in Claim 1. Advantageous further developments of the invention are described in sub-claims.

Since disturbances are uniformly distributed in the disturbed data transmission channel, synchronising words and data words are disturbed to the same extent. If the data

words are transmitted in a code which automatically corrects the data words, this correction is a gauge of the disturbance in the data transmission channel. The number of corrections, i.e. the number of correctable bits in a data word, is thus a gauge of the existence of a disturbance in a data transmission channel. If a correction of the data words cannot be carried out over a relatively long period of time, the data transmission channel can be described as totally out of order.

The invention exploits this recognition and for the assessment of the disturbance in a data transmission channel considers not only a disturbed synchronising word but at the same time the correctable data word. A joint evaluation of error rates in the synchronising word and in the data word thus leads to an improved decision criterion regarding a disturbance in the data transmission channel. At the same time, the time required to recognise a disturbance can be reduced.

For the further explanation of the invention, exemplary embodiments will be described in detail in the following making reference to drawings wherein:

Figure 1 is a diagram of an information transmission system;

Figure 2 illustrates data sequences in an information transmission system;

Figure 3 is a diagram of a circuit for the recognition of synchronising words;

Figure 4 is a diagram of a second circuit for the recognition of synchronising words;

Figure 5 is a diagram of a monitoring circuit for synchronisation;

Figure 6 is a diagram of a circuit for carrying out concealments;

Figure 7 is a block circuit diagram for the recognition of synchronising words and

Figure 8 is a circuit for changing over between the build-up process and the steady state.

Figure 1 illustrates an information source 1, a transducer 2, a transmitting device 3, a data transmission channel 4, a disturbance 5, a receiving device 6, a transducer 7, a decoder 8 for data words, a detector 9 for synchronising words, a monitoring unit 10 for the synchronisation, and an information sink 11. In the transducer 7 data sequences are fed to the decoder 8 for data words and to the detector 9 for synchronising words. In the build-up process the detector 9 searches for synchronising words. If the detector 9 recognises synchronising words several times in succession in a given time frame, a switch-over is made to a steady state. In the steady state both the decoder 8 for data words and the

detector 9 for synchronising words monitor the synchronisation. The monitoring unit 10 evaluates both the error rate of the data words and the error rate of the synchronising words. If the receiving device 6 is a 4-PSK demodulator, two subsidiary frames (channel A, channel B), referred to in the following as sub-frames, are produced, where both channels A, B lead to the decoder 8 and both channels A, B lead to the detector 9.

Figure 2 illustrates data sequences comprising synchronising words 21, 22, 51 and 52 and data words 23-50. A total of 16 programmes I-XVI with a left-hand and a right-hand channel L, R are provided. The data words 23-30 and 37-44 contain the MSBs (most significant bits) of sample values. Parity bits (comparison bits) for error correction are accommodated in the data words 31, 32, additional information items, including a scale factor, are accommodated in the data words 33, 34, and the LSBs (least significant bits) of sample values are accommodated in the data words 35, 36. The scale factor is a code which indicates whether leading zeros are omitted in a data word 23-30, 37-44. The two channels A and B are obtained as sub-frames from a main frame by demodulation in a PSK-demodulator. Each of the two sub-frames (channel A, channel B) comprises a synchronising word containing 11 bits. The BCH-redundancy 31, 32 (BCH = Bose Chaudhuri Hocquenghem) is a plurality of parity bits which, when necessary, corrects the preceding data words 23, 25, 27, 29 and 24, 26, 28, 30. This BCH-code at the same time indicates within limits that fault correction is no longer possible. In this case a concealment is carried out. "Concealment" is to be understood as the use of substitute values for faultily transmitted sample values. If a plurality of (more than three) faulty sample values are transmitted in succession, in the event that synchronising values also occur in adulterated form, the data transmission channel can be described as out of order and therefore a new build-up process must be started.

Figure 3 illustrates two buffer stores 61, 62, two matrices 63, 64, an AND-gate 65, a shift register 66, a NAND-gate 67, a clock input 68 for a clock signal TF (clock signal for the window for a synchronising word) and an output 69. The data sequences of channel A and channel B are fed through the buffer stores 61, 62. The matrices 63, 64 connected to the buffer stores 61, 62 recognise the synchronising words. The matrices 63, 64 recognise the synchronising words even when these contain one faulty bit. In the case of one recognition of two parallel synchronising words in the two sub-frames channel A and channel B, a flag bit (status bit) is set in the shift register 66. In the steady state the shift register 66 is started via the input 68 by the clock signal TF, and thus the flag bit is set, whenever the recognition of a synchronising word is

expected. The number of outputs Q1 - Q4 indicates how many parallel synchronising words must be absent in succession before synchronisation is indicated as being no longer present, via the NAND gate 67, at the output 69.

Figure 4 illustrates a further example of the recognition of synchronising words. The theoretical value of a synchronising word is loaded into a shift register 71. Synchronising words incoming via the channels A and B are intermediately stored in the buffer stores 61 and 62. In comparators 72 and 73, the synchronising words are compared bit by bit with the theoretical value. Faulty bits are added in a NAND-gate 74, and counted in an error counter 75. The number of errors is interrogated via a NOR-gate 76. The interrogation is triggered via the input ABFN (interrogation - errors in negative logic) following the analysis of the last synchronising word bit. The output QSY (output synchronising word) indicates whether synchronising words have been recognised. The synchronising words are considered as having been recognised when a predetermined number of faulty bits, e.g. 2, is not exceeded.

Figure 5 illustrates an OR-gate 81 via which flag bits are set in a shift register (66). A flag bit is set when a synchronising word has been recognised or when a data word has been recognised as being error-free or as containing correctable errors. Only in the event of the absence of a synchronising word or in the case of a synchronising word containing a plurality of errors and a permanent error in the data word, is the flag bit not set. The permanent errors in the data word are recognised by the circuit 83 for error correction. The permanent errors are reported via a negator 82 to the OR-gate 81.

Figure 6 illustrates an error correcting circuit 83, buffer stores 84, 85 and 86, a mean value circuit 87, a change-over switch 88, a circuit breaker 89, data word lines 90-95 and control lines 96 and 97. Consecutive data words ATW $n + 1$, n and $n - 1$ (sample values $n + 1$, n and $n - 1$) are intermediately stored in the buffer stores 84-86. If the sample value n is recognised by the error correcting circuit as being error-free or error-correctable, the sample value n is fed via the data word line 90 and the change-over switch 88 to the output ATW'. If a sample value n is recognised as being no longer correctable, a mean value of the preceding sample value $n - 1$ and the following value $n + 1$ is formed in the circuit 87, and this mean value is fed via the change-over switch 88 to the output ATW'. If a plurality of sample values are recognised in succession as being uncorrectable, the last value to have been recognised as error-free, which is intermediately stored in the buffer store 86, must not be erased. The control line 97 controls the circuit breaker 89 in such manner that in the case of a plurality of consecutive, uncorrectable sample values, no

uncorrectable sample value is fed into the buffer store 86 and the last, still utilizable value remains in the buffer store 86. If a plurality of uncorrectable sample values occur in succession, via the line 91 and the change-over switch 88 the last utilizable sample value is fed to the output ATW' until an error-free or correctable value appears. The last utilizable sample value stored in the buffer store 86, and the first following error-free or correctable value are used to form a mean value in the circuit 87 which is fed to the output ATW'. The new, error-free value is the next value to be fed to the output ATW'. The control lines 96 and 97 control the change-over switch 88.

A table shows the operation of the circuit illustrated in Figure 3 (C = correct, I = incorrect).

1.BF	X.BF	ATWn+1	ATWn	ATWn-1	ATW
No	No	C	C	C	ATWn
No	No	I	C	C	ATWn
Yes	No	C	I	C	$(ATWn+1 + ATWn-1) \times 1/2$
No	No	I	C	I	ATWn
No	Yes	I	I	C	ATWn-1
Yes	No	C	I	C	$(ATWn+1 + ATWn-1) \times 1/2$
No	No	C	C	I	ATWn

In line 1 of the Table, when the sample values ATWn+1, ATWn and ATWn-1 are error-free or corrected in the buffer stores 84-86, the same value ATWn is fed to the output ATW'. In this case the control lines 96 and 97 (1.BF and X.BF) are set at low. In the 2nd line, the sample value ATWn is again fed to the output ATW', although the sample value ATWn+1 is uncorrectable. If, as shown in line 3, a sample value ATWn with an uncorrectable error is intermediately stored in the buffer store 85, but error-free or corrected values are intermediately stored in the buffer stores 84 and 86, the mean value formed from the sample values ATWn+1 and ATWn-1 is fed to the output ATW'. Line 4 shows that an error-free or corrected sample value present in the buffer store 85 is fed to the output ATW' even when the buffer stores 84 and 86 contain uncorrectable values. Line 5 shows that the last utilizable sample value ATWn-1 is retained in the buffer store 86 and is fed to the output ATW' when uncorrectable values arrive in the buffer stores 84 and 85. Lines 3 and 6 are identical. Line 7 shows that when an error-free or corrected data word is present in the buffer store 85, the switch 89 must be reset.

In the case of 4-PSK demodulation, two parallel bits are obtained in respect of each transmitted information

unit. These two parallel bits are divided between the channels A and B. In the PSK demodulation, phase errors occur which lead to a double error in the case of differential demodulation. "Double error" is to be understood as the incorrect decoding of two consecutive bits. In the case of faulty demodulation, an error in the channel A automatically leads to a further error in the channel A or an error in the channel B. Therefore in the build-up process it is advantageous, for the recognition of synchronising words, not to check a respective synchronising word in each sub-frame, but to check synchronising halfwords.

Figure 7 is a block circuit diagram of the synchronising word recognition. Via the channels A and B buffer stores 61 and 62 are loaded with synchronising words. Synchronising halfwords are recognised/searched for in matrix arrangements 101 and 102. This procedure is referred to as search procedure. The matrix arrangement 101 checks the first 10 or 12 bits of the two parallel synchronising words, and the matrix arrangement 102 checks the last 10 or 12 bits of the two synchronising words (1 synchronising word = 11 bits, 1 synchronising halfword = 5 or 6 bits, 2 parallel synchronising words = 22 bits, 2 parallel synchronising halfwords = 10 or 12 bits). During the build-up process, two synchronising halfwords are sufficient to switch on a frame bit counter 105 via a switch 103. Advantageously, via a change-over switch 104 the frame bit counter 105 instigates an error check of the currently received synchronising words. The error checking procedure using the shift register 71, the comparators 72, 73, the OR-gate 74 and the error counter 75 has already been described with reference to Figure 4. The frame bit counter 105 and the switches 103 and 104 cooperate in such manner that during the build-up process synchronising halfwords are recognised and a switch-over is made to the circuit components 71-75 for the recognition of synchronising words. A switch-over is made to the steady state following the recognition of a synchronising halfword and following the recognition of two consecutive, parallel synchronising words. In the steady state, the result of the checking of synchronising halfwords in the matrix arrangements 101, 102 is dispensed with. If a synchronising word is expected, the frame bit counter 105 loads the theoretical value into the shift register and at the end of a synchronising word feeds the result of the check from the counter 75 via the line ABPN to the output QSY. At the same time the frame bit counter carries out descrambling. I.a., as a result of the synchronising difficulty in the receiver, which triggers an uninterrupted series of zeros or an uninterrupted series of ones, scrambling is carried out in such manner that sufficient changes from zeros to ones and from ones to zeros are always available to ensure clock synchronisation at the receiving end. For this purpose a descrambler is provided

at the receiving end and a scrambler is provided at the transmitting end.

Figure 8 illustrates the shift register 66, a NOR-gate 67, an input 68 for a signal TF, an output 69 for a signal SSU (search for synchronising word), inputs for signals QSY and Stop and the negative BF signal, an OR-gate 81, negators 111 and 112, NOR-gates 113 and 114, a D-FF (delay-flip-flop) 115, an AND-gate 116 and an output SA. Via the input SI, flag bits are fed into the shift register 66. These flag bits indicate whether synchronisation is present. In the steady state the AND-gate 116 is released via the stop-input and a flag bit can be set via the OR-gate 81 when a data word is present in error-free or error-corrected form or when two parallel synchronising words are recognised. In the build-up process the AND-gate is disabled by the stop-input, and the data word is not allowed synchronisation. In the steady state, with the assistance of serial flag-bits the outputs Q1 to Q4 indicate the status of the synchronisation of the current main frame and of three preceding main frames. If no synchronisation is detected in four main frames in succession, a new search for a synchronising word is triggered via the NOR-gate 67 and the output 69 with the signal SSU.

At the beginning of the search process, via the clock input the NOR-gate 67 sets the D-FF 115 at $Q = \log 1$. In the build-up process, via the NOR-gate 114 two recognised, consecutive synchronising words set the D-FF (delay-flip-flop) 115, which indicates the build-up process or steady state) to the steady state. This would be termed as a successful window check. If, in the search procedure, the first two parallel synchronising words are not followed by any second parallel synchronising words during the first window check, the NOR-gate 113 responds, resets the shift register 66 and triggers a new search procedure.

Claims

1. A process for the synchronisation of digital information signals in a receiver (6, 7), in particular for satellite broadcasting, wherein synchronising words (21, 22, 51, 52) and data words (23 - 50) are transmitted in regular time (main frame) periods, wherein the synchronising words and/or data words possess a uniform code word length and an error-correcting code (BCH) is used for the data word transmission, wherein in a build-up process a search procedure is started to find the synchronising words and wherein in a steady state a change-over is made to synchronisation monitoring, characterised in that the synchronisation monitoring jointly analyzes a check of the synchronising words (21, 22, 51, 52) and a check of the error rate of transmitted data words (23 - 50), that in the steady state a change-over is made to resynchronisation when a data word can no longer be corrected and a plurality of consecutive synchronising words are recognised as being incorrect, and that in the search procedure to rapidly find a synchronising word preferably only parts of a synchronising word, e.g. synchronising halfwords, are checked.
2. A process as claimed in Claim 1, characterised in that the steady state is maintained when a limited number of errors are present in the synchronising words (21, 22, 51, 52).
3. A process as claimed in Claim 1, characterised in that the steady state is maintained when a limited number of consecutive synchronising words (21, 22, 51, 52) are absent.
4. A process as claimed in Claim 1, characterised in that the steady state is maintained when a limited number of consecutive synchronising words (21, 22, 51, 52) possess a limited number of errors and/or are absent.
5. A process as claimed in one or more of the preceding claims, characterised in that the steady state is maintained when one or more uncorrectable data words (23 - 50) are received.
6. A process as claimed in Claim 5, characterised in that one or more concealments (Figure 6) are performed for one or more uncorrectable data words (23 - 50).
7. A process as claimed in one or more of the preceding claims, characterised in that a change-over is made



from the build-up process into the steady state when two or more synchronising words (21, 22, 51, 52) are found consecutively in regular time periods.

8. A process as claimed in one or more of the preceding claims, characterised in that a change-over is made from the build-up process into the steady state when the synchronising words (21, 22, 51, 52) and/or error-free or error-correctable data words (23 - 50) are received once or several times in succession.
9. A process as claimed in Claim 7 or 8, characterised in that a limited number of errors are permitted in the synchronising words (21, 22, 51, 52).
10. A device for the synchronisation of digital information signals in a receiver (6, 7), in particular for satellite broadcasting, wherein synchronising words (21, 22, 51, 52) and data words (23 - 50) are transmitted in regular time (main frame) periods, wherein the synchronising words and/or data words possess a uniform code word length and an error-correcting code (BCH) is used for the data word transmission, wherein in a build-up process a search procedure is started to find the synchronising words and wherein in a steady state a change-over is made to synchronisation monitoring, characterised in that the device comprises a synchronisation monitoring unit (10) for checking the synchronising words (21, 22, 51, 52) with a synchronising word detector (9) and with a data word decoder (8) for checking the error rate of transmitted data words (23 - 50), that the synchronising word detector (9) comprises a circuit (61, 62, 63, 64, 65; 101, 102, 103) for recognising the synchronising words, and that in the steady state a change-over is made to resynchronisation when a data word can no longer be corrected and a plurality of consecutive synchronising words are recognised as incorrect in the decoder (9).
11. A device as claimed in Claim 10, characterised in that a shift register (66) stores the state of error rates of the synchronising words and/or data words in the last n time periods (main frame).
12. A device as claimed in Claim 10 or 11, characterised in that a circuit (83) is provided for the error correction.
13. A device as claimed in Claim 12, characterised in that the circuit (83) controls a circuit (84 - 89) for the formation of concealments.



14. A device as claimed in one or more of Claims 10 to 13, characterised in that a flip-flop (115) stores the build-up process state or the steady state.
15. A device as claimed in one or more of Claims 10 to 14, characterised in that a frame bit counter (105) is provided which counts the number of bits in the frames.
16. A device as claimed in one or more of Claims 10 to 15, characterised in that the frame bit counter (105) carries out descrambling.

