CLAIMS.

1. A silicon photonic integrated chip (PIC) device (10), comprising:
   (a) a silicon-on-insulator, SOI, substrate (11) serving as a platform for fabricating said device (10);
   (b) at least one optical waveguide disposed on said SOI substrate for guiding light waves, wherein one or more device components are fabricated on said SOI substrate (11) or said optical waveguide;
   (c) a suspended edge coupler (12) for coupling said light waves between said waveguide and an optical fiber; and
   (d) at least one protective film (13) protecting the device (10) from one or more external environmental conditions,

   characterized in that:
   - said suspended edge coupler (12) includes at least one edge facet (12a), trench (12b) and/or lateral cavity (12c),
   - said protective film (13) covers an exposed surface of said edge facet (12a), trench (12b) and/or lateral cavity (12c), such that a cross section of said protective film (13) conforms to that of said exposed surface (14) of said edge facet (12a), trench (12b) and/or lateral cavity (12c)
   - said protective film (13) is formed of an electrically insulative composition comprising at least one of silicon nitride and silicon oxynitride, and
   - a thickness of said protective film (13) is within a range of 10 – 100 nanometers.

2. The device (10) as claimed in claim 1, wherein said protective film (13) is disposed on said device (10) by a plasma enhanced chemical vapor deposition (PECVD) process.

3. The device (10) as claimed in claim 1, comprises one or more electrical contacts on said exposed surface (14), wherein said protective film (13) includes an opening for exposing each electrical contact.

4. The device (10) as claimed in claim 3, wherein said electrical contacts include bondpads.

5. The device (10) as claimed in claim 3, wherein said protective film (13) is etchable to form said opening.

6. The device (10) as claimed in claim 5, wherein a mask is provided to define one or more portions to be etched to form said opening.

7. The device (10) as claimed in claim 5, wherein an anisotropic composition is provided to facilitate etching of said protective film (13).

8. The device (10) as claimed in claim 1, wherein said etching is blanket etching.

9. The device (10) as claimed in claim 1, wherein an angle of a sidewall of said edge facet (12a) and/or said trench (12b) with respect to said SOI substrate (11) is within 87 - 90°.

10. A method (20) for fabricating a silicon photonic integrated chip (PIC) device, comprising the steps of:

(a) disposing at least one optical waveguide on a silicon-on-insulator, SOI, substrate for guiding light waves (21);

(b) forming one or more device components on said SOI substrate or said waveguide (22);

(c) forming a suspended edge coupler for coupling said light waves between said waveguide and an optical fiber (23); and

(d) disposing at least one protective film for protecting said device from one or more external environmental conditions (24),

characterized in that:

– said suspended edge coupler is formed with at least one edge facet, lateral cavity and/or trench,

– said protective film is disposed on an exposed surface of said silicon PIC device, such that a cross section of an upper surface of said protective film conforms to that of said exposed surface,

– said protective film is formed of an electrically insulative composition comprising at least one of silicon nitride and silicon oxynitride, and

– a thickness of said protective film is within a range of 10 – 100 nanometers.

11. The method (20) as claimed in claim 10, wherein said protective film is disposed on said device by a plasma enhanced chemical vapor deposition (PECVD) process.

12. The method (20) as claimed in claim 10, further comprising the steps of:
disposing one or more electrical contacts on said exposed surface and etching an opening through said protective film for exposing each electrical contact.

13. The method (20) as claimed in claim 12, further comprising the step of masking said protective film to define one or more portions to be etched to form said opening, before said etching step.

14. The method (20) as claimed in claim 12, wherein said etching step is blanket etching.

15. The method (20) as claimed in claim 10, wherein an angle of a sidewall of said edge facet and/or said trench with respect to said SOI substrate is within 87 - 90°.