STRESSED DIELECTRIC LAYER WITH STABLE STRESS

ABSTRACT

An integrated circuit is provided having a substrate and a transistor in an active region of the substrate. The substrate also has an isolation region having a dielectric material. In one embodiment, a pre-metal dielectric layer is disposed over the substrate and the transistor. At least one of the isolation region or the pre-metal dielectric layer includes a O_3 TEOS oxide having a stress retaining dopant. The O_3 TEOS oxide induces a stress in a channel region of the transistor.

Fig. 1