

FIG. 1A

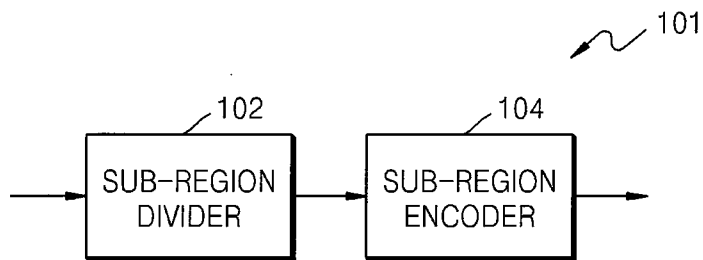


FIG. 1B

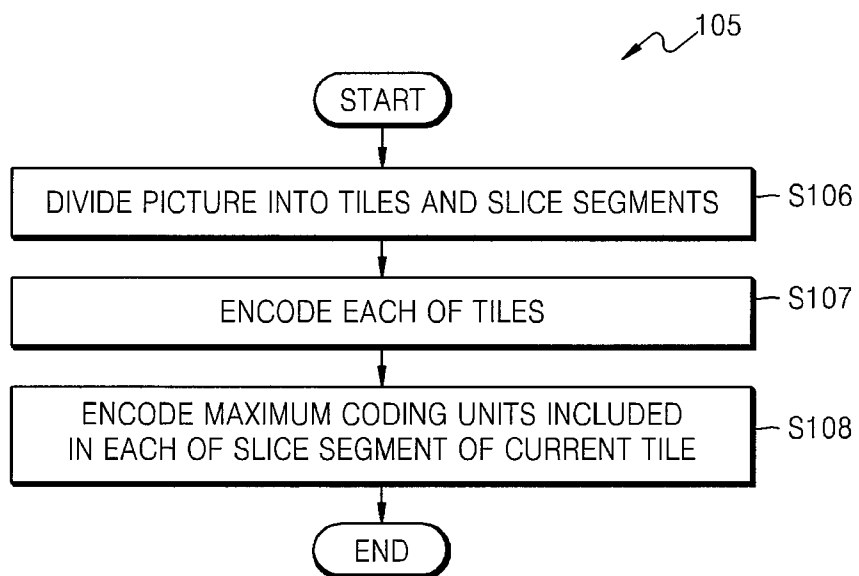


FIG. 1C

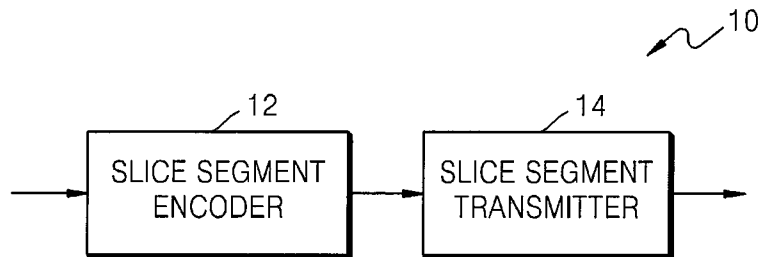


FIG. 1D

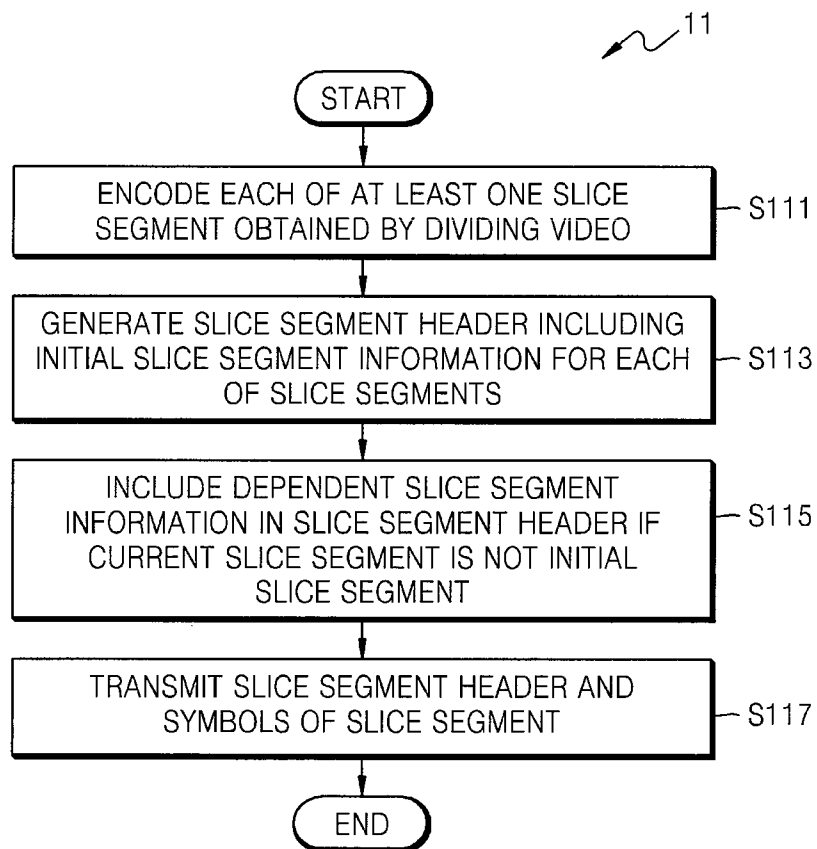


FIG. 2A

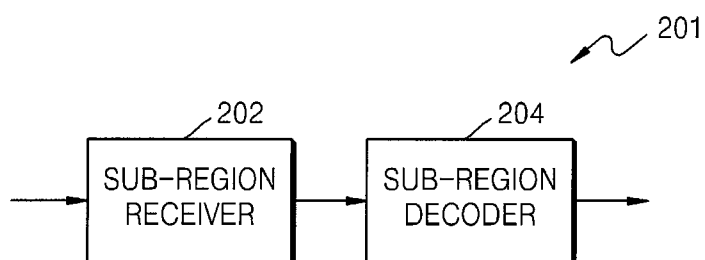


FIG. 2B

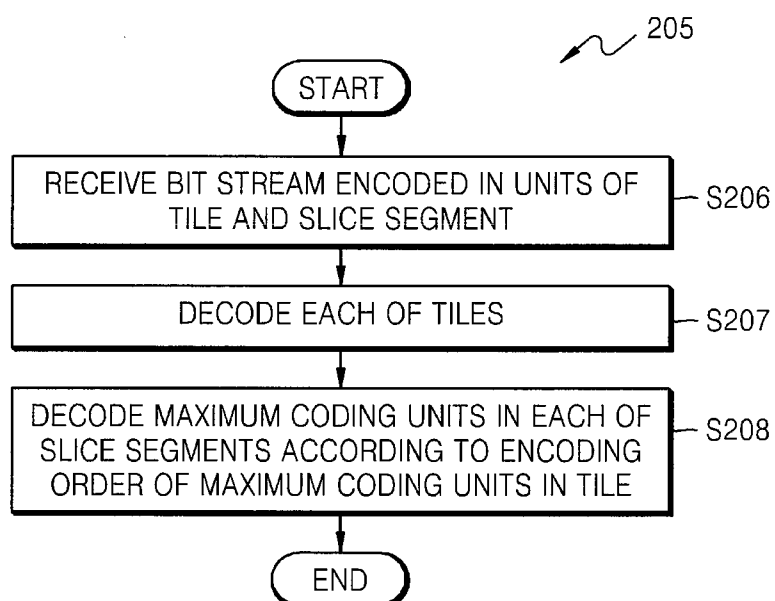


FIG. 2C

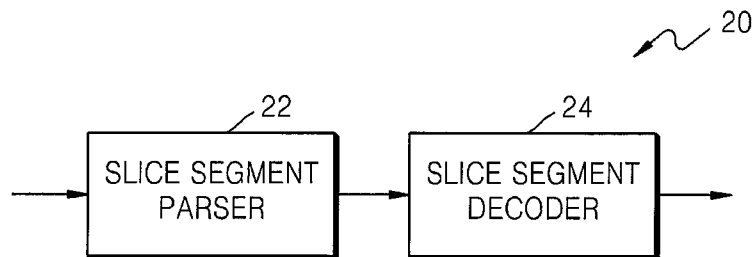


FIG. 2D

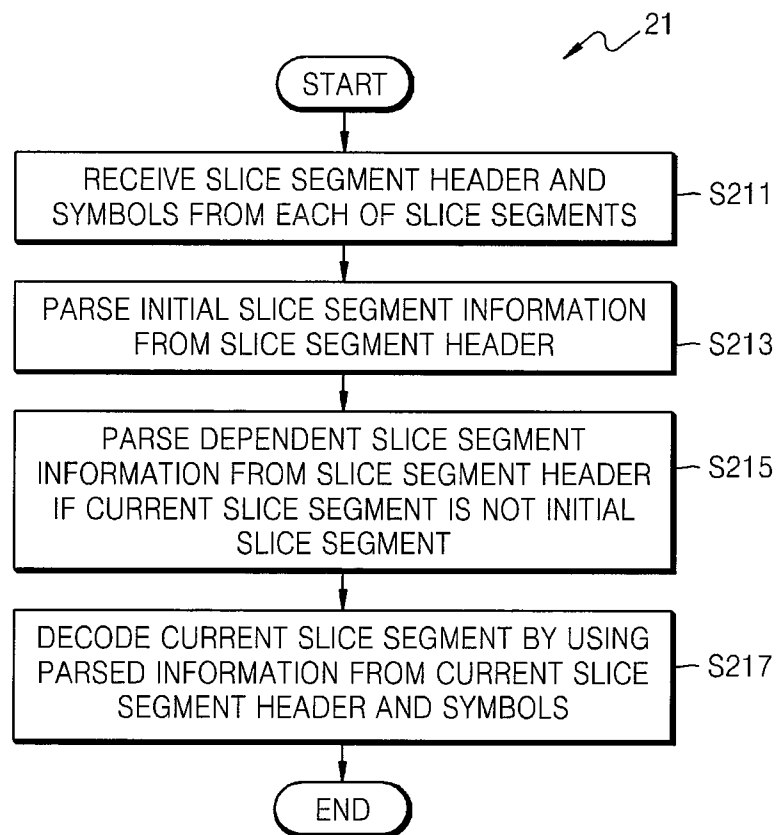


FIG. 3

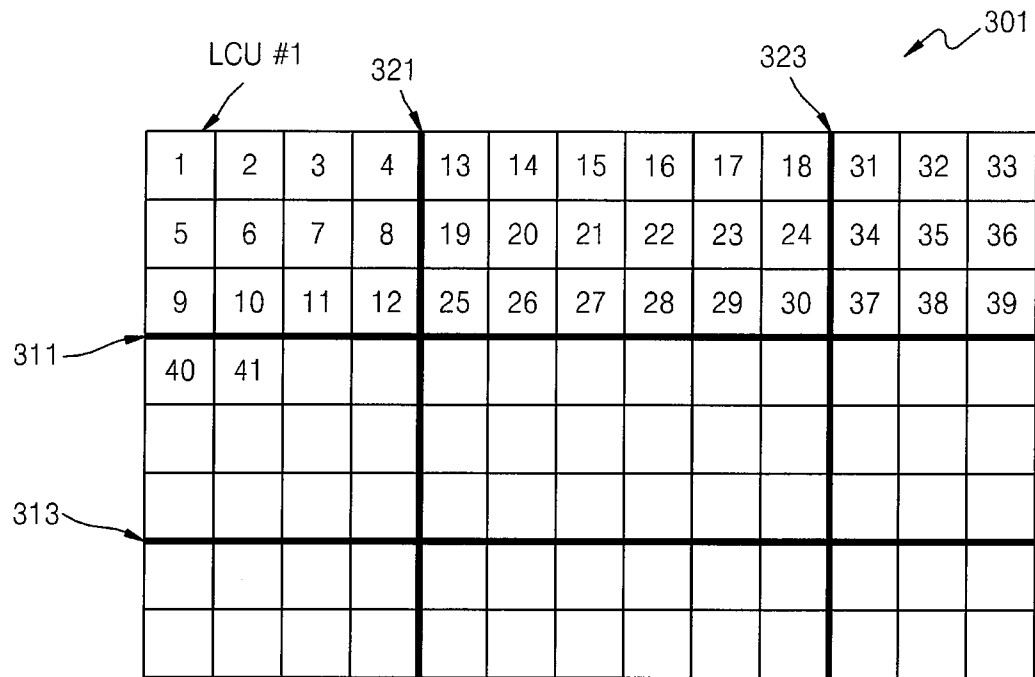


FIG. 4

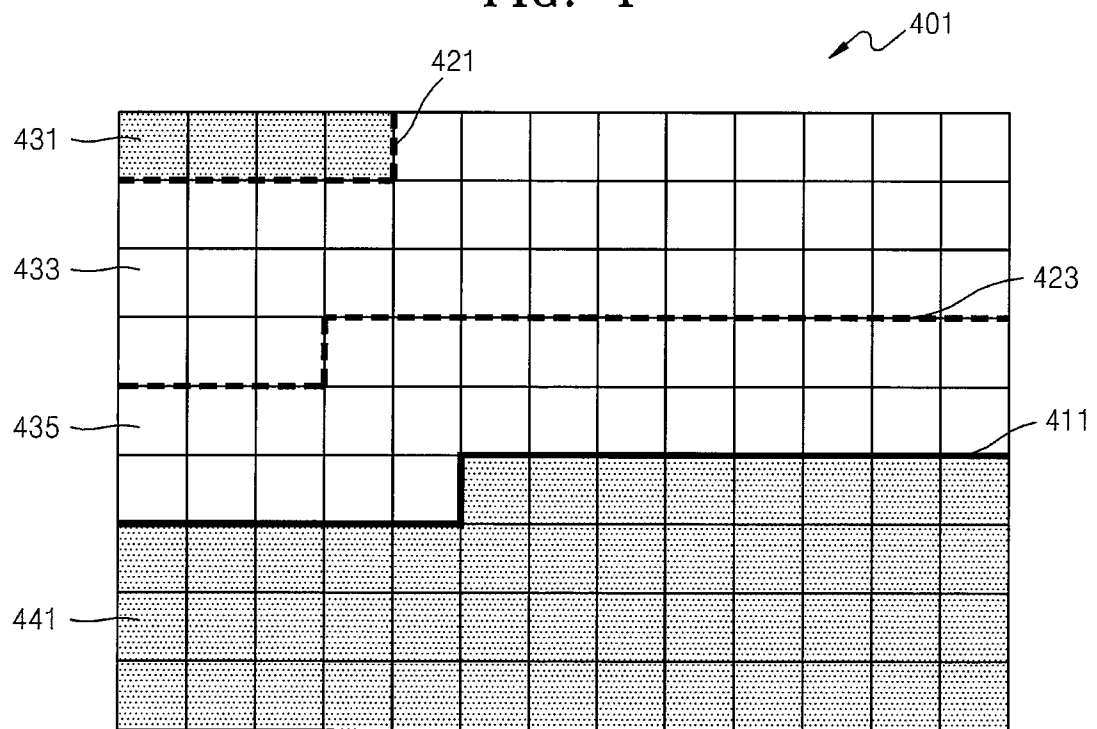


Diagram illustrating a tiled architecture (50) divided into three tiles: Tile #1, Tile #2, and Tile #3. Tile #1 is a 4x4 grid of cells, numbered 1 to 32. The grid is divided into four 2x2 blocks. The first block (cells 1-4, 5-8, 9-12, 13-16) is labeled 'LCU #1' and '51'. The second block (cells 17-20, 21-24, 25-28, 29-32) is labeled '52'. The third block (cells 33-36, 37-40, 41-44, 45-48) is labeled '53'. The fourth block (cells 49-52, 53-56, 57-60, 61-64) is labeled '54'. The entire grid is labeled '50'.

Diagram 525 illustrates a 2x2 grid of tiles. The top-left tile is labeled "Tile #1" and contains "SLICE SEGMENT 0" and "SLICE SEGMENT 1". The top-right tile is labeled "Tile #2" and contains "SLICE SEGMENT 1" and "SLICE SEGMENT 2". The bottom-left tile is labeled "TILE #3" and contains "SLICE SEGMENT 3" and "SLICE SEGMENT 4". The bottom-right tile is labeled "TILE #4" and contains "SLICE SEGMENT 5" and "SLICE SEGMENT 6". Solid lines represent slice segment boundaries, and dashed lines represent tile boundaries.

FIG. 6A

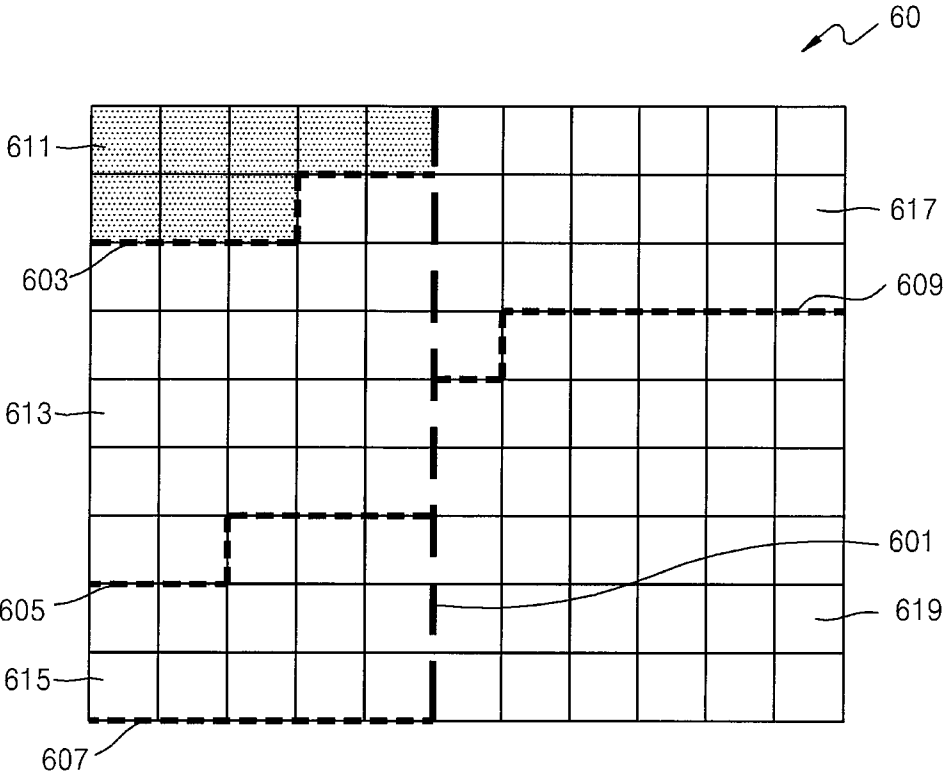


FIG. 6B

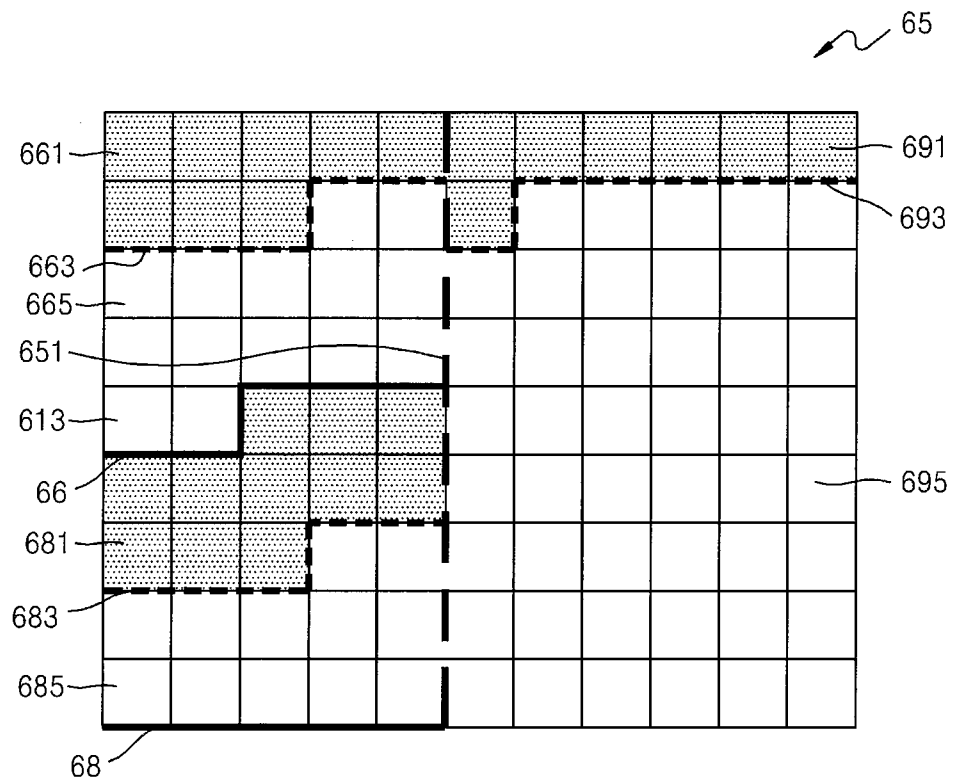


FIG. 7

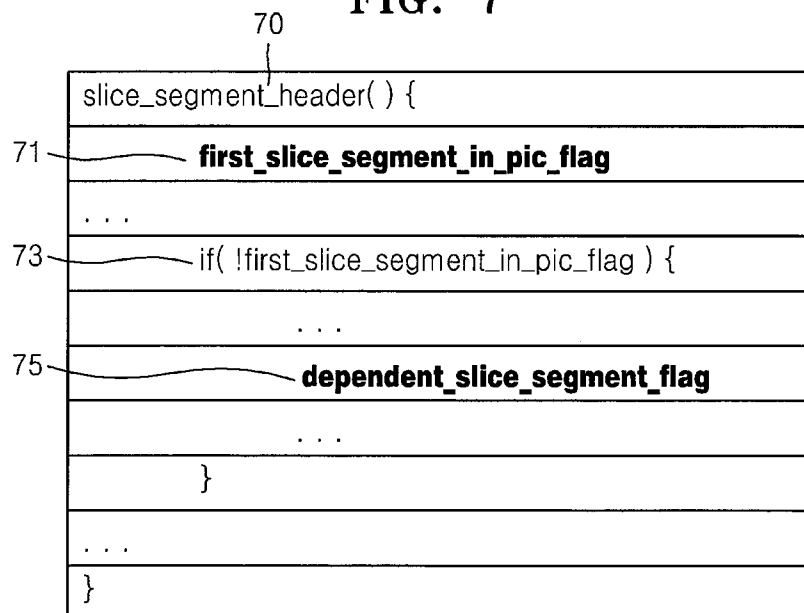


FIG. 8

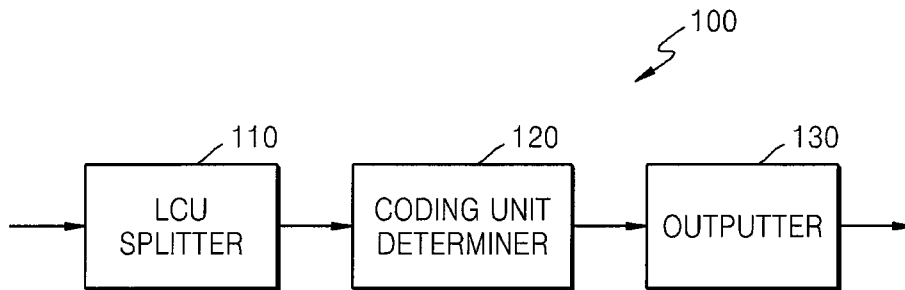


FIG. 9

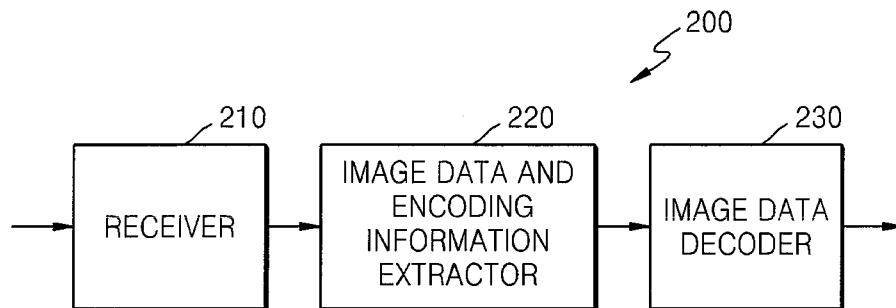


FIG. 10

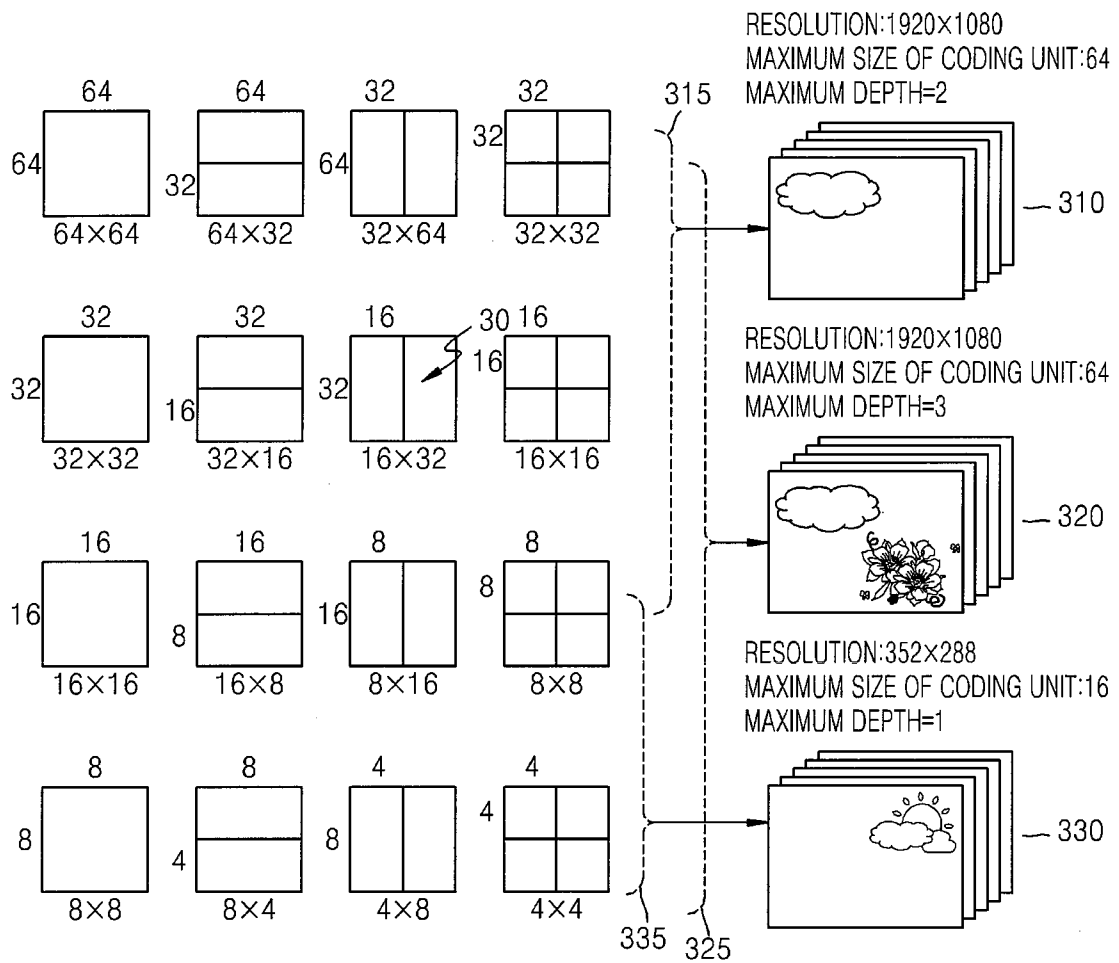


FIG. 11

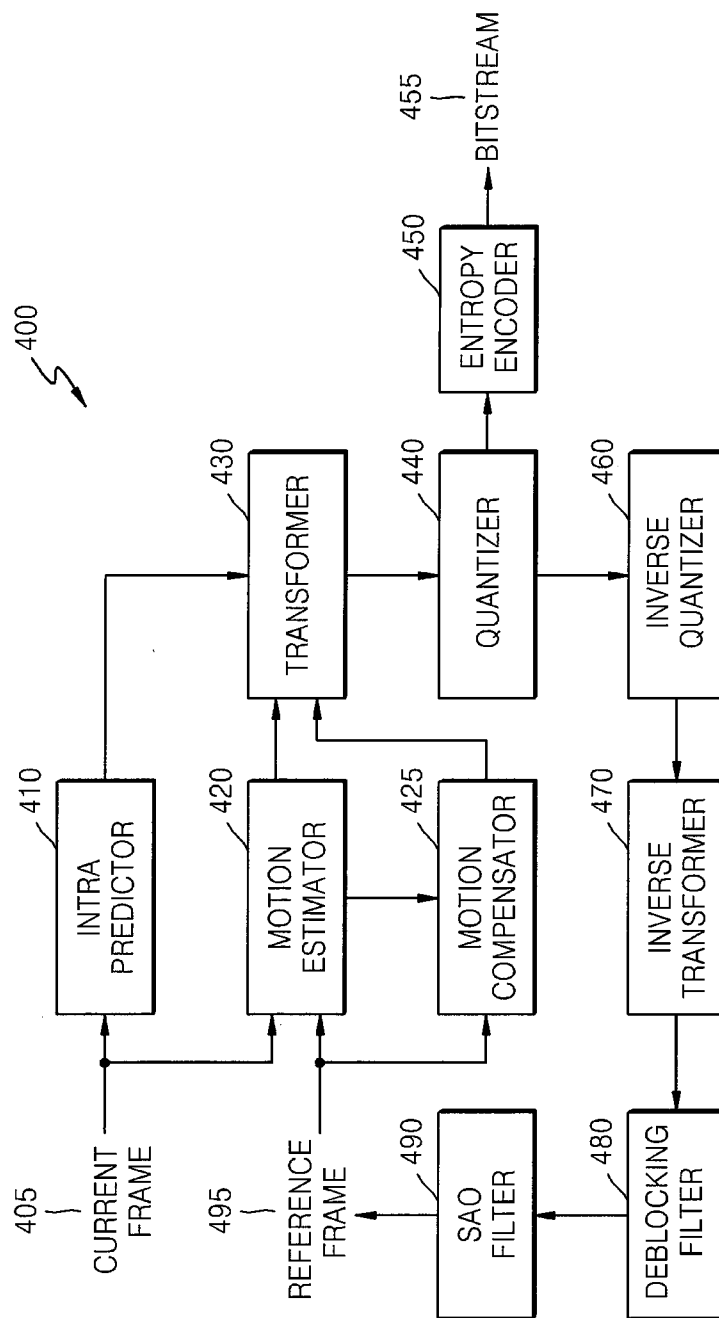


FIG. 12

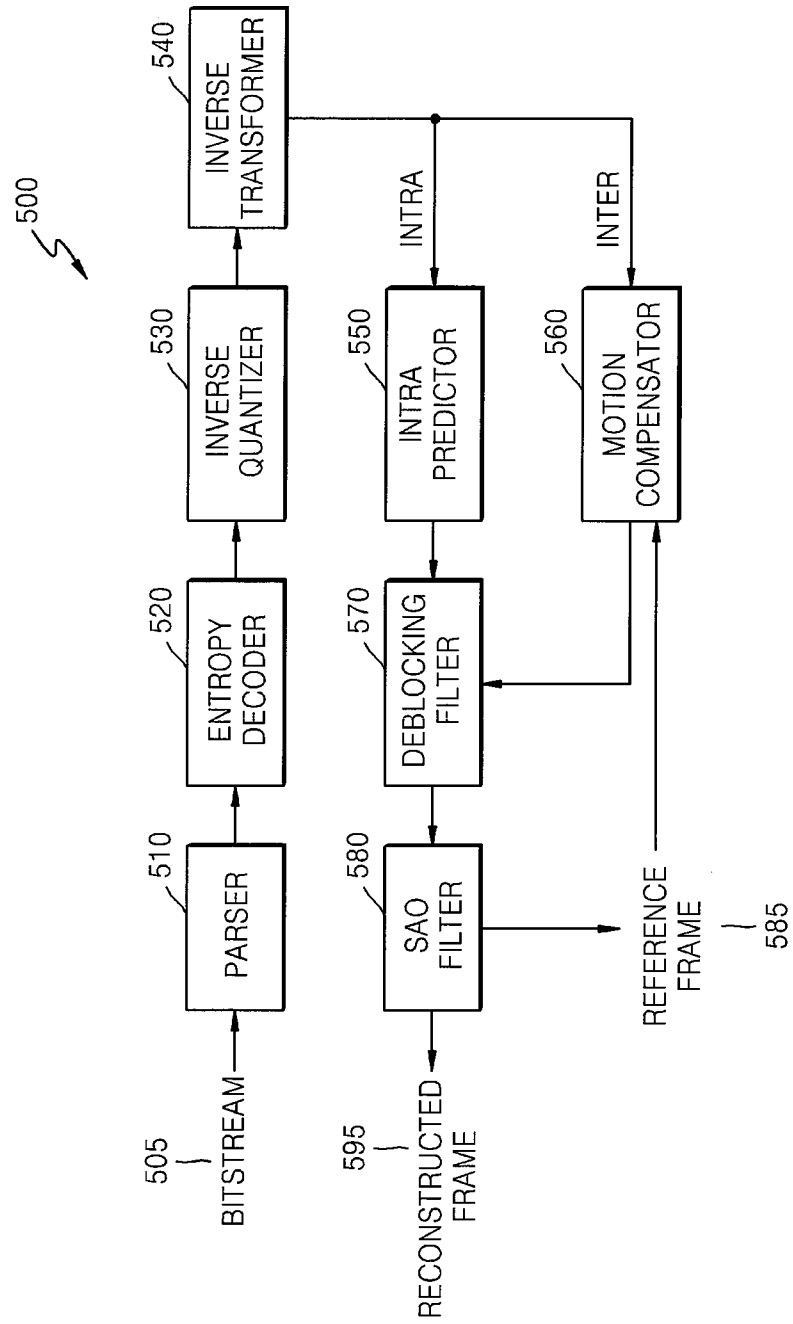


FIG. 13

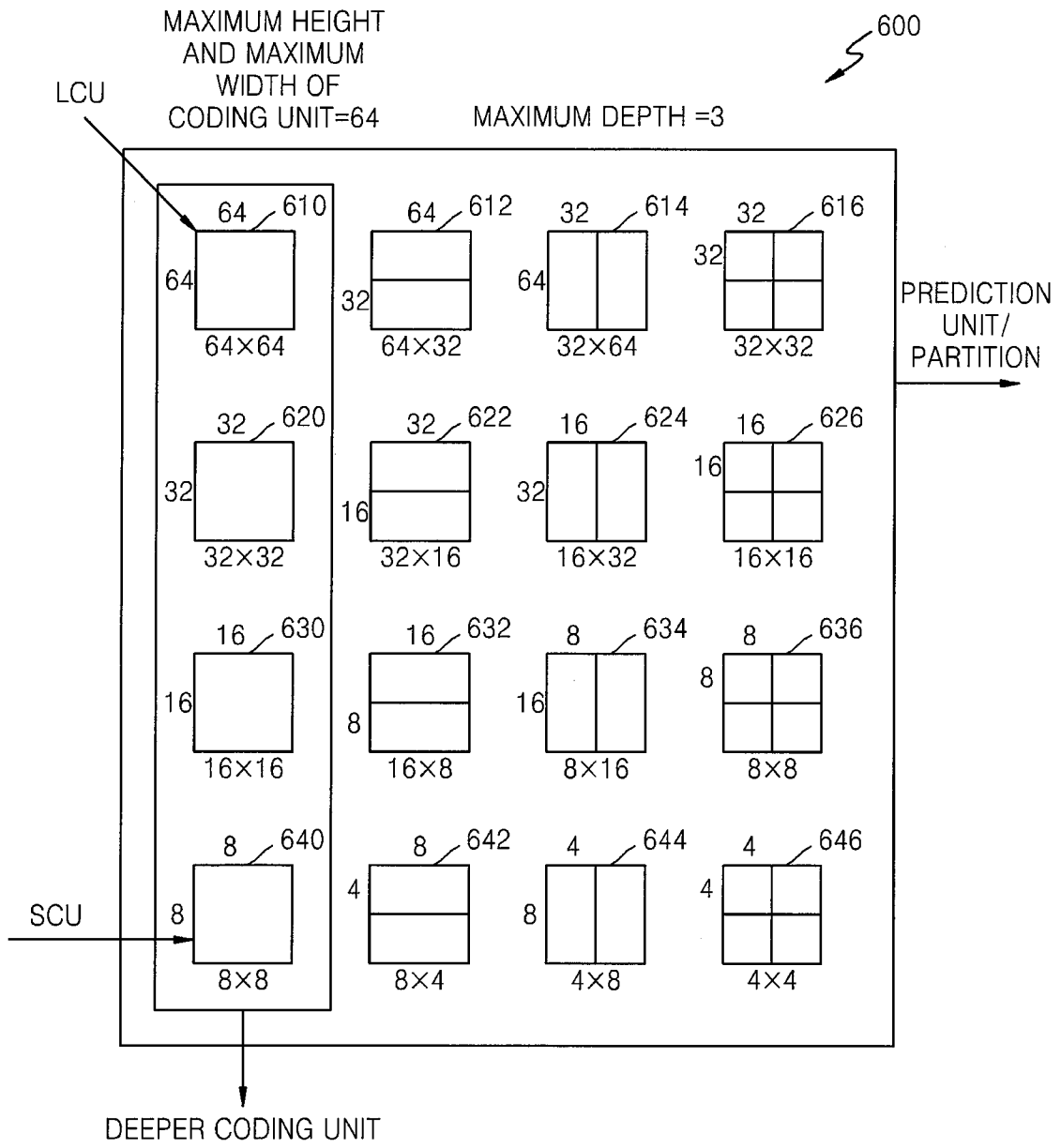


FIG. 14

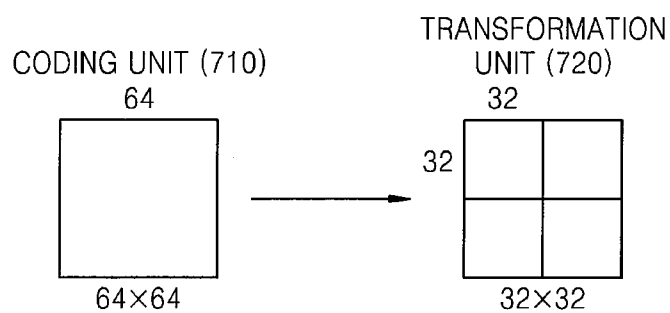


FIG. 15

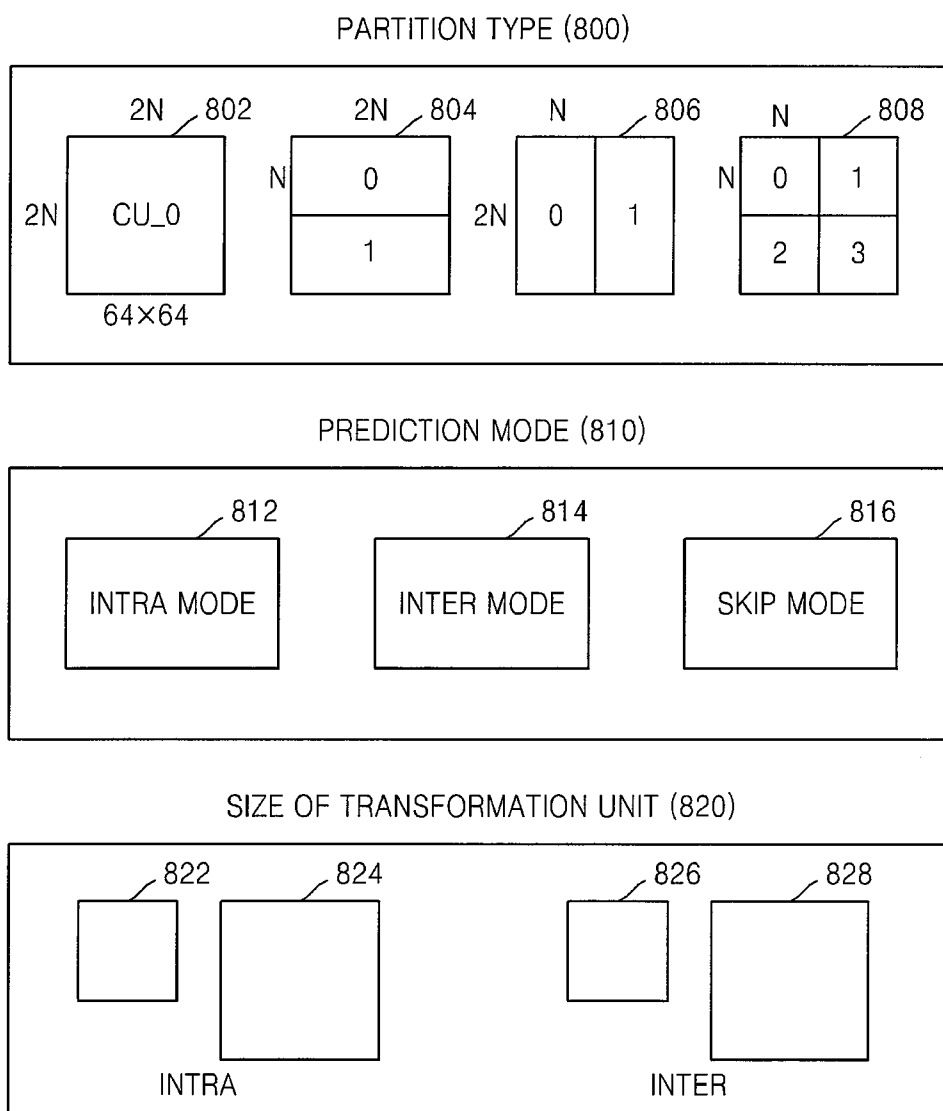


FIG. 16

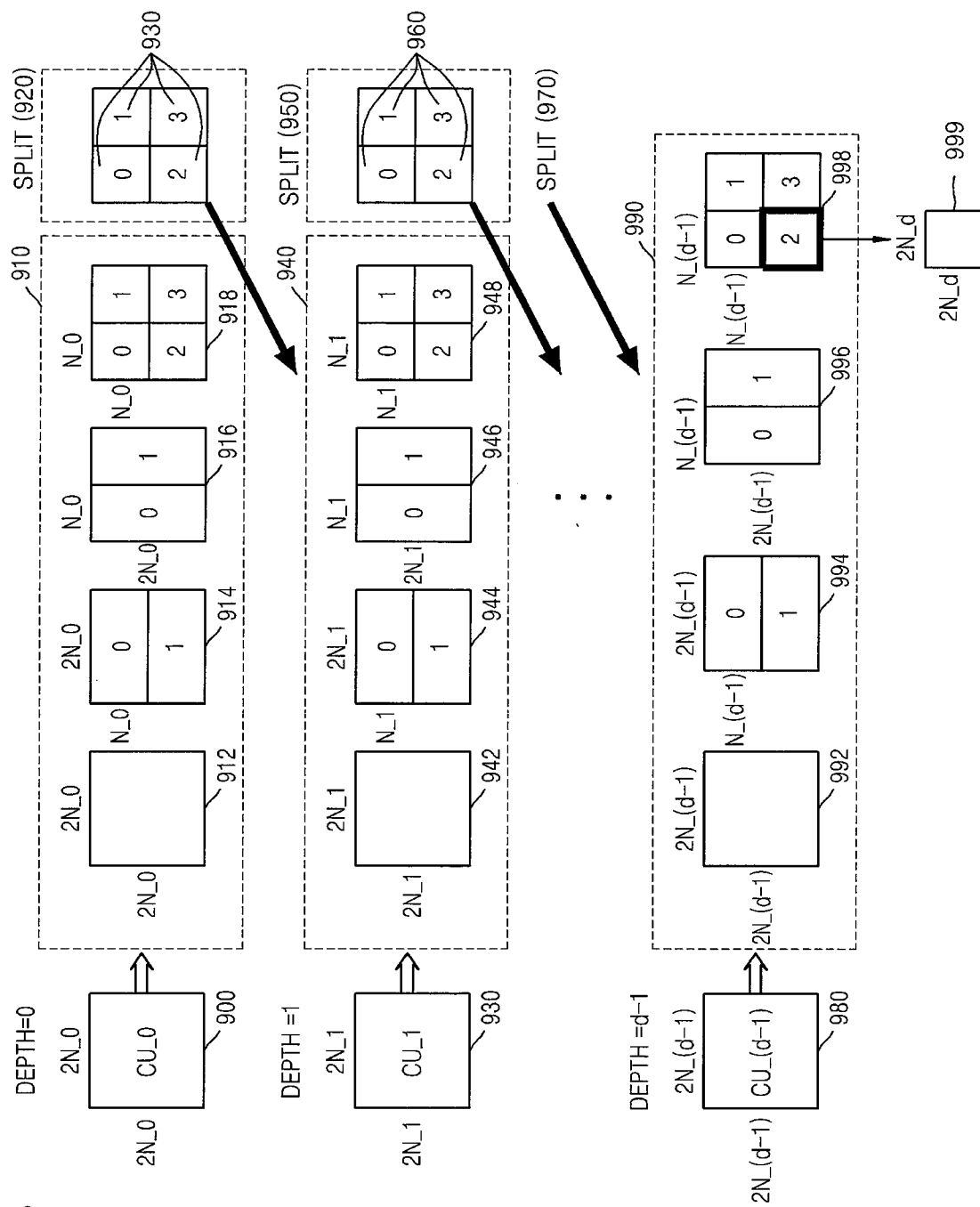
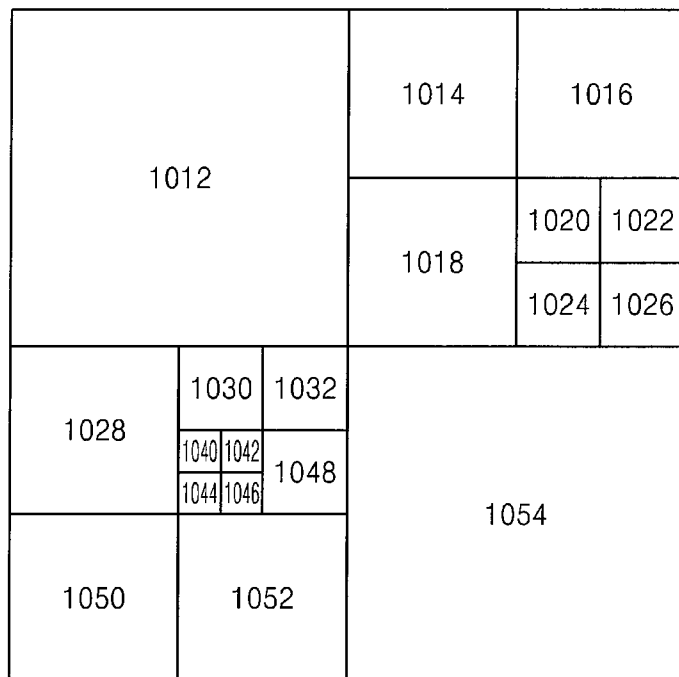


FIG. 17



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FIG. 18

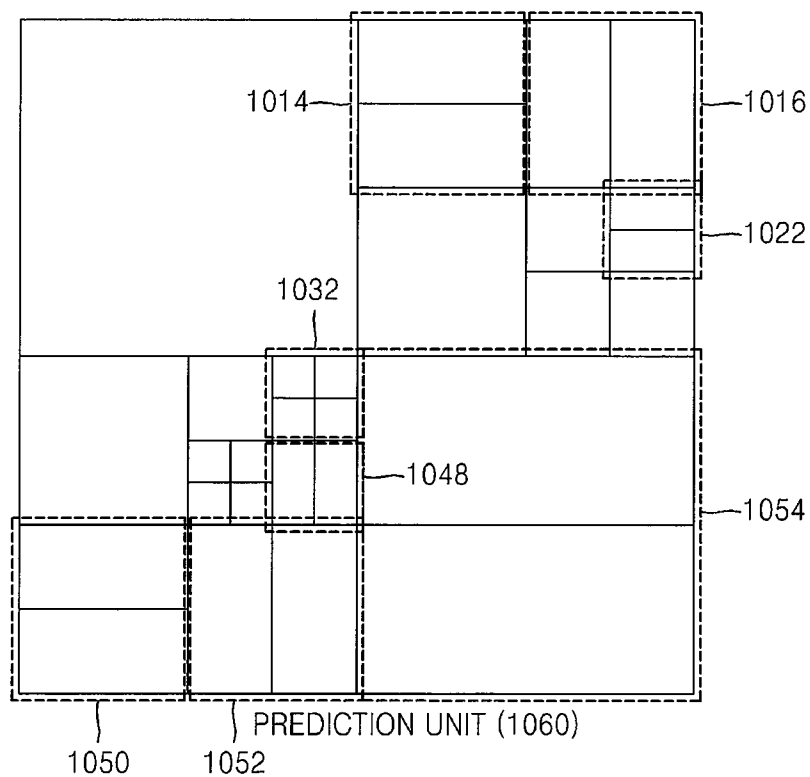


FIG. 19

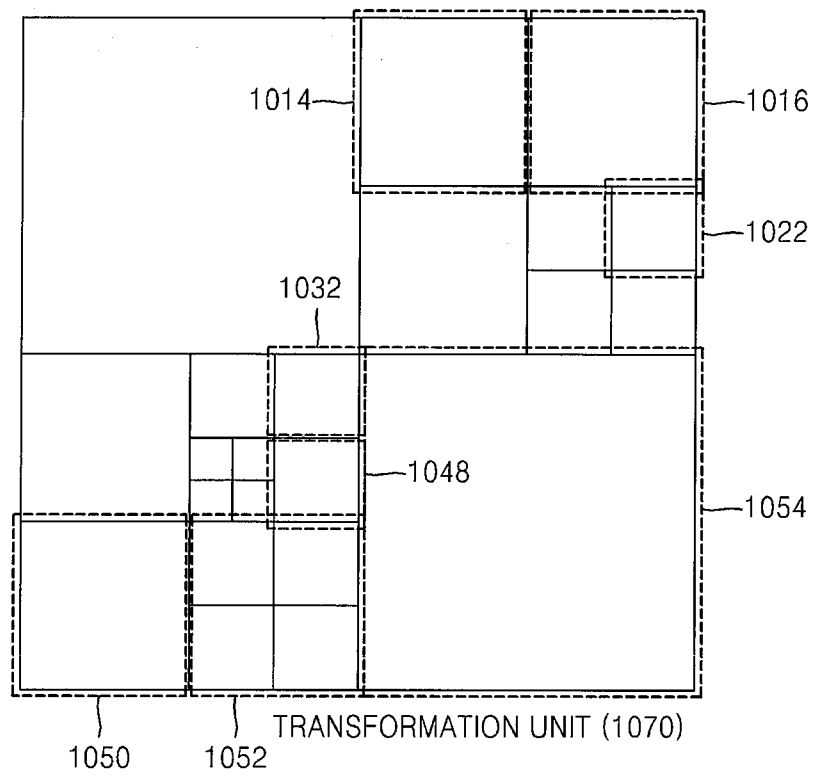


FIG. 20

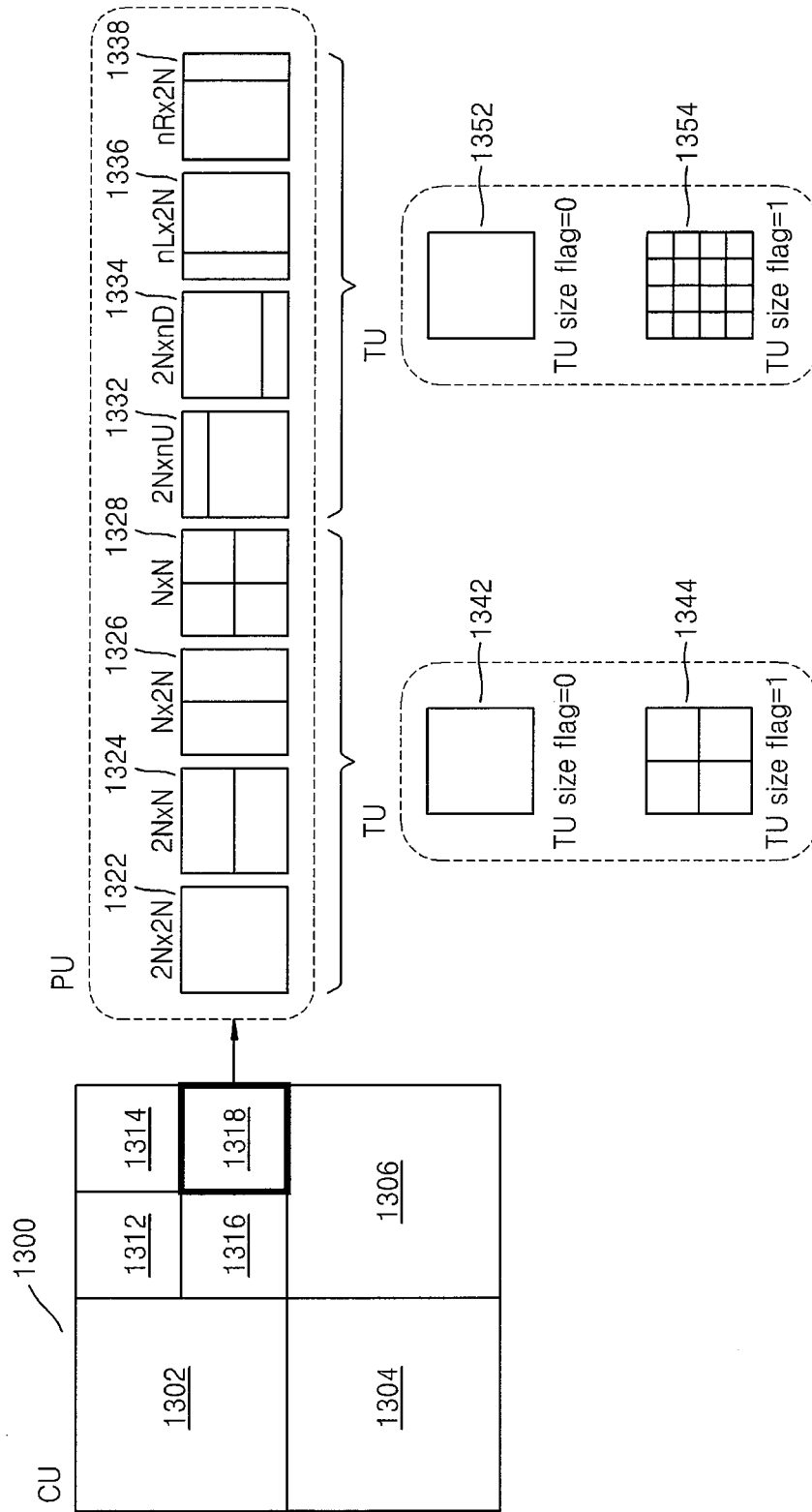


FIG. 21

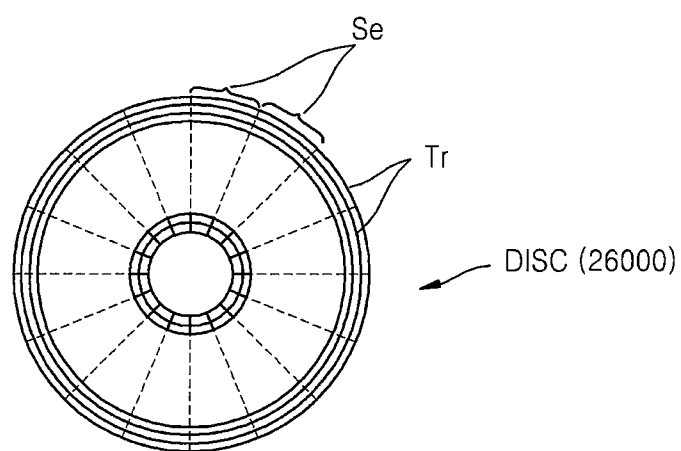


FIG. 22

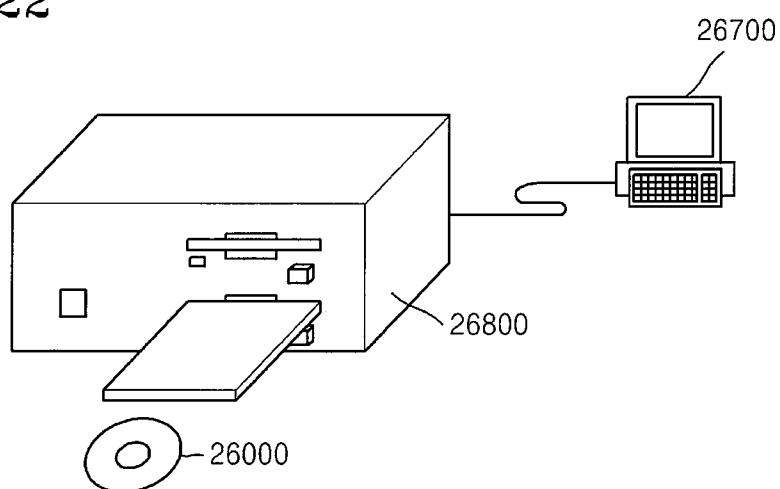


FIG. 23

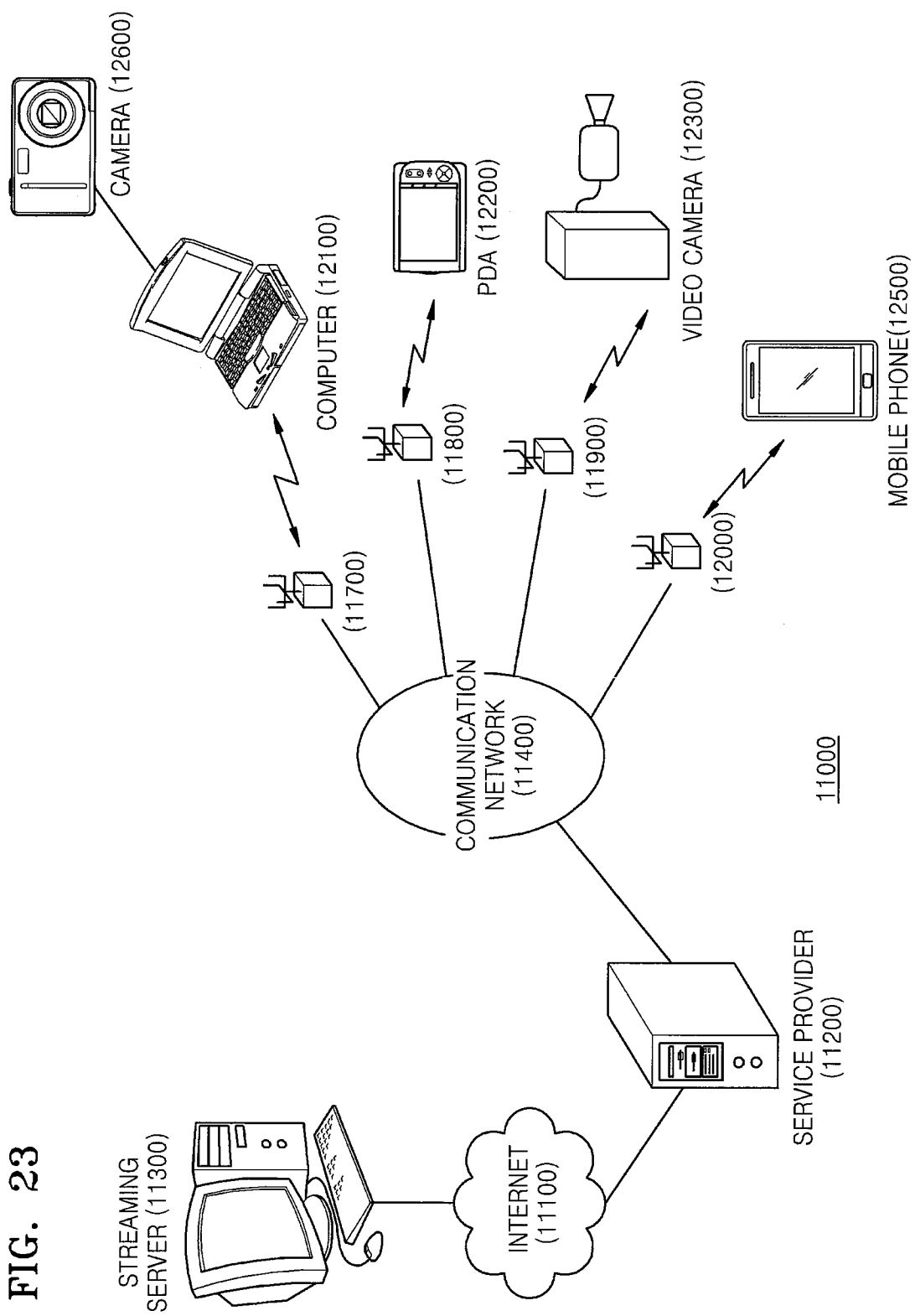


FIG. 24

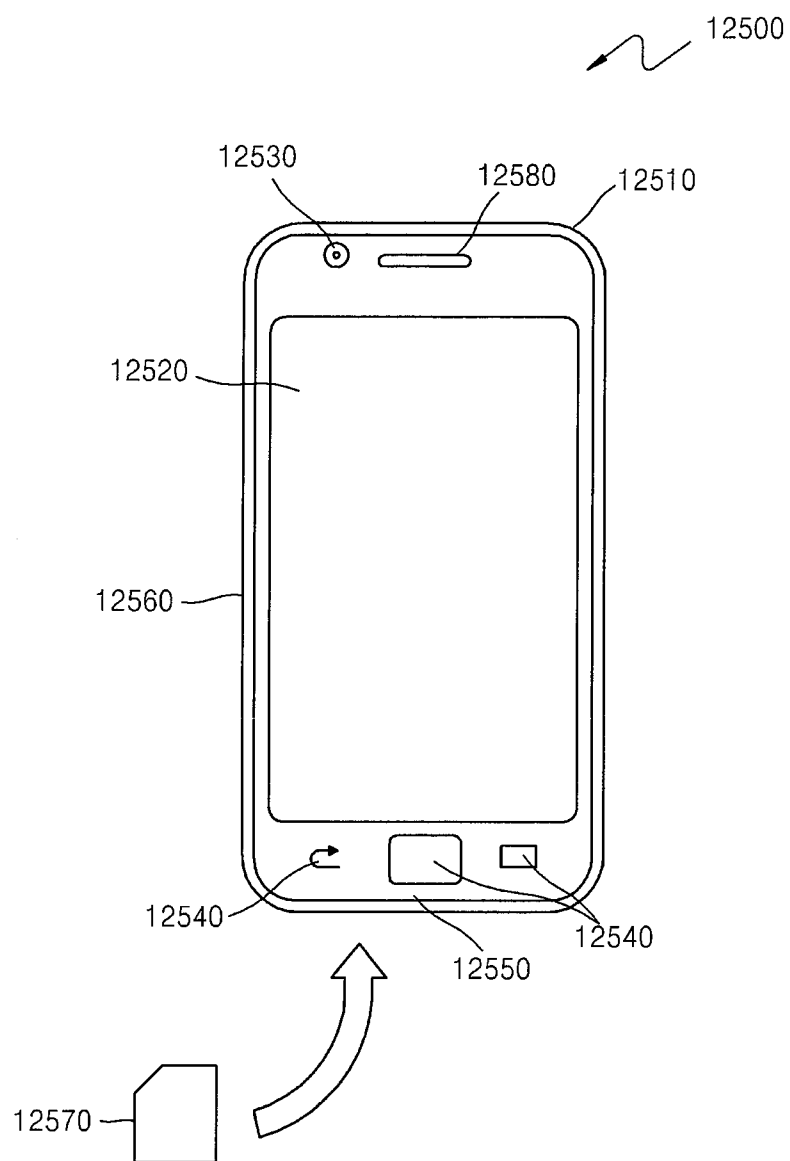


FIG. 25

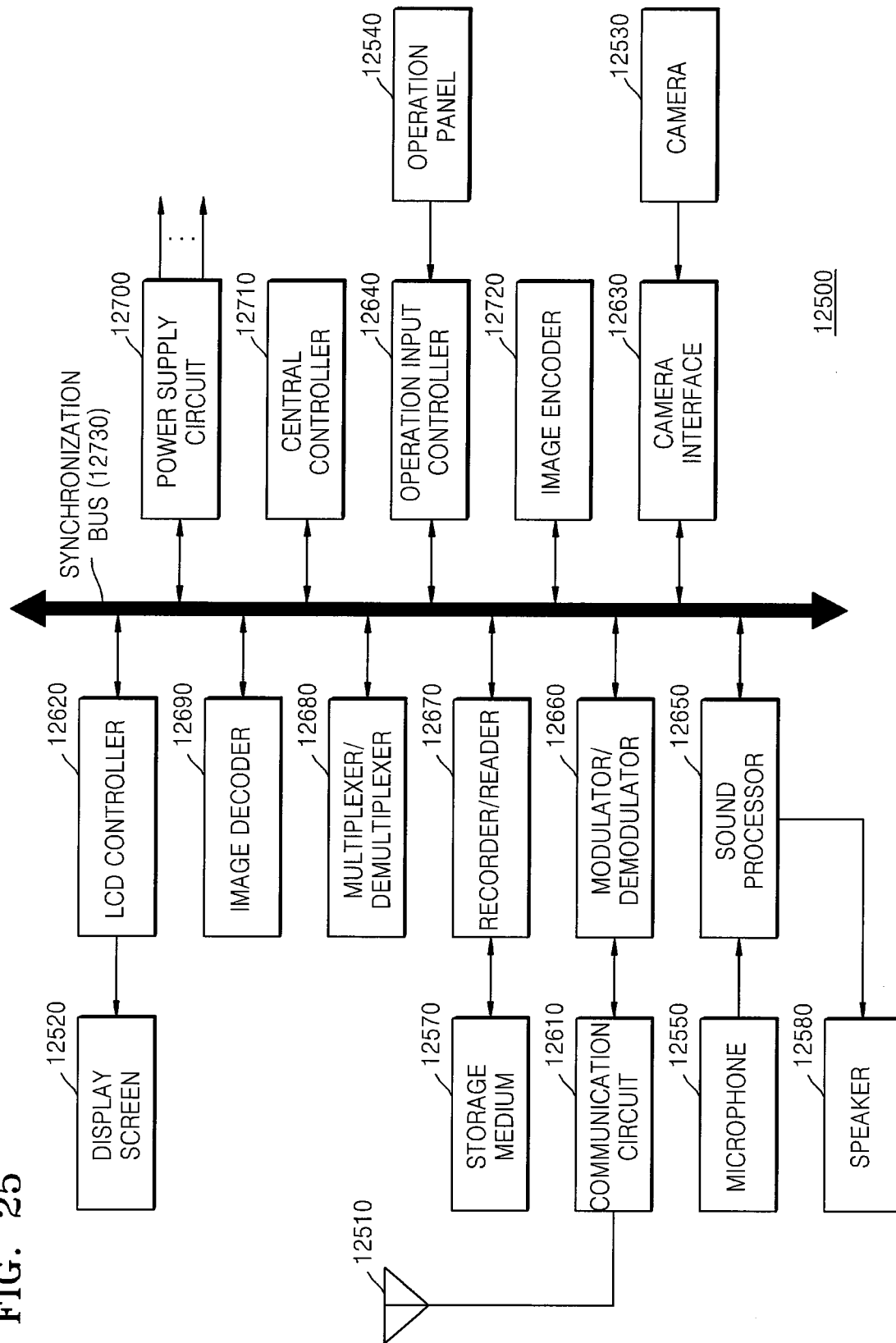


FIG. 26

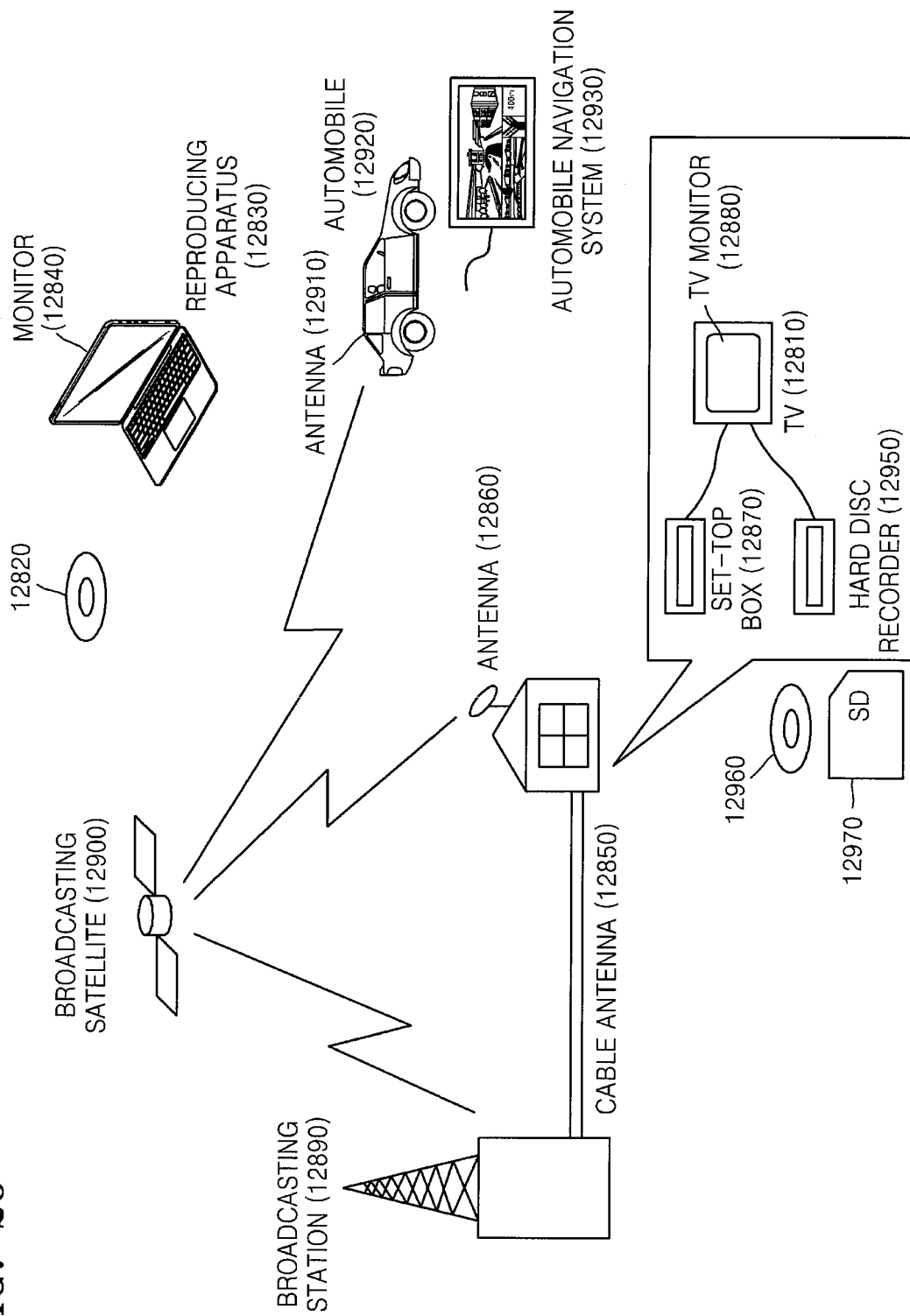


FIG. 27

