Patent Claims

1. A method for manufacturing a device, said method comprising:

carrying out a correction step comprising manufacturing a spacer wafer, the spacer wafer including a multitude of regions in a plane, each of which has a respective vertical extension perpendicular to the plane;

said spacer wafer comprising a first layer and a second layer which are made of different materials and which are vertically stacked one upon the other, each of said first layer and said second layer having a shape of a contiguous disk extending throughout each said multitude of regions;

wherein the manufacturing comprises, after an initial formation of the spacer wafer, decreasing a length of respective ones of said vertical extensions in a plurality of said multitude of regions so as to compensate at least partially for manufacturing irregularities in another device when the spacer wafer is combined with the other device, the spacer wafer being distinct from the other device, wherein said decreasing said vertical extension comprises carrying out a first processing step and carrying out subsequently to said first processing step a second processing step different from said first processing step in at least one aspect, and wherein said vertical extension is decreased both in said first processing step and in said second processing step, and

wherein said decreasing the length is accomplished by removal of material from said second layer only.

2. The method according to claim 1, wherein said first processing step differs from said second processing step in an applied processing technique.

3. The method according to claim 1, wherein said first processing step differs from said second processing step in a tool used in the respective processing step.

4. The method according to claim 1, wherein said first processing step differs from said second processing step in at least one processing parameter used in the respective processing step.

5. The method according to claim 1, the method comprising decreasing said vertical extension in said plurality of said multitude of regions by removing material in said plurality of said multitude of regions.

6. The method according to claim 1, wherein said first processing step is carried out at a higher rate of removal of material from said plurality of said multitude of regions than said second processing step.

7. The method according to claim 1, wherein said decreasing said vertical extension is accomplished using cutting or machining.

8. The method according to claim 7, wherein said cutting or machining is individually applied to each of said plurality of regions.

9. The method according to claim 1, wherein said decreasing said vertical extension is accomplished using milling or using a milling tool.

10. The method according to claim 9, wherein said milling or said milling tool is individually applied to each of said plurality of regions.

11. The method according to claim 1, wherein said decreasing said vertical extension is accomplished using laser ablating.

12. The method according to claim 11, wherein said laser ablating is individually applied to each of said plurality of regions.

13. The method according to claim 1, wherein said device being manufactured is an optical device.

14. The method according to claim 1, wherein said manufacturing irregularities comprise a deviation from a nominal value of an optical property of said other device.

15. The method according to claim 1, wherein said spacer wafer is manufactured using replication, wherein a replication master used in said replication is designed for at least partially compensating for said manufacturing irregularities.

16. The method according to claim 1 wherein the other device is another wafer.

17. The method of claim 1 wherein each of the first and second processing steps includes at least one of removing material from the spacer wafer or adding material to the spacer wafer.

18. The method of claim 2 wherein each of the first and second processing steps includes at least one of removing material from the spacer wafer or adding material to the spacer wafer.

19. The method of claim 3 wherein each of the first and second processing steps includes removing material from the spacer wafer.

20. A method for manufacturing a device, said method comprising:

performing a correction step comprising manufacturing a spacer wafer, said spacer wafer including a multitude of regions defining a multitude of corresponding channels that are parallel to one another, each of the channels having a respective length defined by an extension of a respective one of the regions in a direction parallel to the channels;

said spacer wafer comprising a first layer and a second layer which are made of different materials and which are vertically stacked one upon the other, each of said first layer and said second layer having a shape of a contiguous disk extending throughout each of said multitude of regions;

wherein the manufacturing comprises, after an initial formation of the spacer wafer, decreasing a length of respective ones of said extensions in a plurality of said multitude of said regions so as to compensate at least partially for manufacturing variations in one or more other devices when the spacer wafer is combined with the one or more other devices, the spacer wafer being distinct from the one or more other devices, wherein said decreasing comprises performing, in each of said plurality of said multitude of said regions, a first processing step and subsequently performing a second processing step that differs from the first processing step in at least one aspect and

wherein said decreasing the length is accomplished by removal of material from said second layer only.

21. The method of claim 20 wherein the first processing step differs from the second processing step in one or more of: an applied processing technique, a tool used in the respective processing step, or a processing parameter used in the respective processing step.

22. The method of claim 20 wherein each of the first and second processing steps includes removing material from the spacer wafer.

23. A method for manufacturing a device, said method comprising:

performing a correction step comprising manufacturing a spacer wafer, said spacer wafer including a multitude of regions defining a multitude of corresponding channels that are parallel to one another, each of the channels having a respective length defined by an extension of a respective one of the regions in a direction parallel to the channels;

said spacer wafer comprising a first layer and a second layer which are made of different materials and which are vertically stacked one upon the other, each of said first layer and said second layer having a shape of a contiguous disk extending throughout each of said multitude of regions;

wherein the manufacturing comprises, after an initial formation of the spacer wafer, decreasing a length of respective ones of said extensions in a plurality of said multitude of said regions so as to compensate at least partially for manufacturing variations in one or more other devices when the spacer wafer is combined with the one or more other devices, the spacer wafer being distinct from the one or more other devices, wherein said decreasing comprises performing, in each of said plurality of said multitude of said regions, a first processing step and subsequently performing a second processing step that differs from the first processing step in at least one aspect, and

wherein said decreasing the length is accomplished by removal of material from said second layer only;

the method further comprising attaching the spacer wafer to another wafer comprising the one or more other devices.

24. The method of claim 23 wherein each of the one or more other devices comprises at least one passive optical component.

25. The method of claim 24 wherein each of the passive optical components comprises a lens.

26. The method of claim 23 wherein the manufacturing comprises decreasing the length of said respective ones of said extensions in said plurality of said regions so as to compensate at least partially for manufacturing variations in a focal length of one or more of the other devices when the spacer wafer is combined with the one or more other devices.

27. The method of claim 23 wherein each of the first and second processing steps includes at least one of removing material from the spacer wafer or adding material to the spacer wafer.

28. The method of claim 1 wherein the first processing step is applied to sections of the spacer which are different from sections of the spacer wafer to which the second processing is applied.

29. The method of claim 1 wherein the first processing step is applied to first sections of the spacer wafer and the second processing step is applied to second sections of the spacer wafer, wherein the second sections are different from and comprised within the first sections.

30. The method of claim 1 wherein the device is a multi-channel device comprising a plurality of channels, and wherein the first processing step is applied simultaneously to the plurality of channels, and the second processing step subsequently is applied individually to each of the plurality of channels.

31. The method of claim 20 wherein the first processing step is applied to sections of the spacer wafer which are different from sections of the spacer wafer to which the second processing is applied.

32. The method of claim 20 wherein the first processing step is applied to first sections of the spacer wafer and the second processing step is applied to second sections of the spacer wafer, wherein the second sections are different from and comprised within the first sections.

33. The method of claim 20 wherein the device is a multi-channel device comprising a plurality of said multitude of corresponding channels, and wherein the first processing step is applied simultaneously to said plurality of said multitude of the corresponding

channels, and the second processing step subsequently is applied individually to each of said plurality of said multitude of corresponding channels.

34. The method of claim 23 wherein the first processing step is applied to sections of the spacer wafer different from sections of the spacer wafer to which the second processing is applied.

35. The method of claim 23 wherein the first processing step is applied to first sections of the spacer wafer and the second processing step is applied to second sections of the spacer wafer, wherein the second sections are different from and comprised within the first sections.

36. The method of claim 23 wherein the device is a multi-channel device comprising a plurality of said multitude of corresponding channels, and wherein the first processing step is applied simultaneously to said plurality of said multitude of corresponding channels, and the second processing step subsequently is applied individually to each of said plurality of said multitude of corresponding channels.

37. The method of claim 1 wherein said second layer is made of a polymer material, and said first layer is made of glass.

38. The method of claim 20 wherein said second layer is made of a polymer material, and said first layer is made of glass.

39. The method of claim 23 wherein said second layer is made of a polymer material, and said first layer is made of glass.