

The invention relates to a track post-control system for a magnetic tape unit with transverse track recording.

With magnetic tape units of the above-mentioned type the recording and the reading of the tracks preferably take place by means of a head wheel bearing the magnetic heads, which rotates transversely to the tape direction. In contrast to commercial video recorders operating by the helical scan method, magnetic tracks are recorded which run approximately perpendicular to the tape edges of the magnetic tape. Whereas with known methods, e.g. VHS, the content of a field can be stored in one helical scan, the small width of the magnetic tape available with transverse track recording means that only a fraction of a field can be accommodated on one track. For the storage of a field, therefore, several tracks have to be recorded successively in a time sequence. Each individual magnetic head therefore takes over a track with a number of lines derived from the particular mechanical characteristics of the unit. In playback mode the frames are read out in succession and composed in a connected television set to form a field. Deviations of various kinds, e.g. fluctuations in the tape speed, can lead to phase errors during the playback. These cause synchronisation faults in the television receiver, which become noticeable on the screen as unpleasant distortion of perpendicular edges present in a picture. Various circuits for the removal of such phase errors are known with known transverse track units, mainly of a professional nature. In transverse track units of the firm Ampex, for example, the composite colour signal to be played back passes through a voltage-controlled delay line, or in another version switchable delay lines which are controlled by detection of additionally recorded reference pulses or else by the colour subcarrier serving as reference. Although phase errors during the playback are thereby prevented, precise track post-control for optimum utilization of the recorded signals, or optimum crosstalk behaviour, is not achieved.

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Drum
 Another possible method of preventing phase errors is described in DE-PS 1085688, according to which a head drum with several heads is fitted with an auxiliary drum in parallel with it and with only one recording head, where both drums rotate on the same shaft. The auxiliary drum is displaced by the main drum to an axial distance such that it lies between two recorded transverse tracks. During playback the auxiliary head, when it approaches a recorded transverse track, emits a pulse which causes the tape to accelerate.

A method of track post-control is also known in which the magnetic head or heads are adjusted in height relative to the magnetic tape as a function of control signals recorded during the recording onto the magnetic tape, as described in "Grundig. Technische Informationen" 3-1980, No. 3, pp. 111-130. The height adjustment takes place by means of piezo-ceramic plates clamped to one side of the head drum and onto whose freely vibrating reed the video heads are fixed. By application of a control voltage the piezo-ceramic plates are deflected mechanically in such a way that the magnetic heads can follow the recorded transverse tracks.

There is also known from EP-A-40 066 a track post-controlled magnetic tape unit in which a pair of heads are passed simultaneously over 2 tracks. Control values are derived from the phase position of the scanned signals, which serve for the post-control of the heads in the axial direction of the head wheel or for variation of the tape speed.

The object of the invention is to devise a track post-control system for a magnetic tape unit with transverse recording, in which the direction of the phase errors for the individual magnetic heads is recognised during playback by means of horizontal synchronous pulses or other continuously recorded pulses and this leads to post-control of the position of the head wheel relative to the recorded magnetic track. It is intended to achieve both optimum track post-control with minimum crosstalk and also optimum phase correction.

This object is achieved by the invention described in claim 1. Advantageous developments of the invention are described in the sub-claims.

The directional evaluation of the phase errors is made possible in principle by the azimuth angles of the magnetic heads arranged on the head wheel. For example, if a track recorded with a predetermined azimuth angle is scanned exactly symmetrically by a magnetic head with the same azimuth angle, no phase difference with respect to a reference pulse sequence will be recognised with pulse sequences recurring in the individual lines, e.g. horizontal pulses. If the track does not lie symmetrically relative to the scanning head, on the other hand, time differences will be obtained, i.e. phase errors in comparison with a reference pulse sequence. These phase errors have different signs for identical offset of the track relative to the scanning magnetic head. The polarity arises from the symmetrically alternating azimuth angles of the magnetic heads. In one case the horizontal pulse is with offset in the direction of the previously written track scanned by a magnetic head later in time and with offset from the following written track earlier in time, while in the case where the following magnetic track has identical offset the magnetic head with symmetrically different azimuth angle reads out the polarity of the phase differences exactly in reverse. It can therefore be seen that the greater the azimuth angle of the magnetic heads is, the greater are also the phase jumps, i.e. the time differences with scanning near the track centre. It is also possible, however, e.g. if the individual magnetic heads are not adjusted with complete precision, to deliberately read out near to the track centre, in order thereby to avoid phase errors.

In a recognition circuit the size and direction of the phase differences for the individual magnetic heads are detected for each head rotation and fed to a memory. At the next head rotation the previously stored values are read out and fed to an electro-mechanical converter in the form of control voltages for the adjustment of the head wheel individually for each magnetic head. The adjustment takes the form of an approximate adaptation to the particular written track by outputting

afresh at each head rotation the correction variables subdivided into steps. Only if the phase errors are so small that they are no longer detected within a predetermined window is adjustment of the head discontinued; the latter is post-controlled with the stored end value corresponding to its deviation.

A further problem also arises in the case of units with transverse track recording in which the content of a field is recorded on several adjacent magnetic tracks, namely in the reproduction of stills. This problem can also be solved by the post-control, according to the invention, of the head wheel, if with the magnetic tape stationary the head wheel, in addition to the phase error correction, is also moved by a ramp generator in a recurring sequence across the magnetic tracks containing a field or picture.

In a preferred embodiment of the invention, tracks with a content of 25 television lines per track are recorded with a width of the magnetic tape of 8 mm. The scanning speed is some 4 m per sec. The number of the magnetic heads comes according to the choice of the angle of wrap to $2n = 6$ ($60^\circ - 80^\circ$) or $2n = 8$ for an angle of wrap obtained by means of the curvature of $45^\circ - 60^\circ$.

The invention will be explained in detail by means of an exemplifying embodiment in the drawings, where

- Figure 1 illustrates the distortions of vertical lines appearing on the screen of a television set with incomplete track post-control.
- Figure 2 is a block diagram of a possible embodiment for a track post-control circuit.
- Figures 3 and 4 are flow diagrams of this apparatus in normal playback mode or in still or search mode.
- Figure 5 shows time and signal-shape diagrams at inputs and outputs of various component parts of the circuit shown in Figure 2.

Figure 1 shows the visible effect of phase errors at track transition points from one magnetic track to the next due to incomplete track post-control. In the interval of 25 lines, which are scanned by each magnetic head, synchronisation errors can be recognised on the screen. 6 vertical lines (VI) - V6 are represented, which are distorted in opposite directions. The direction of the phase errors and hence also of the distortions arises from the azimuth angle of the individual magnetic heads, which are arranged symmetrically offset from one other.

VI
9/11

In region A the played back signal of head 1 can be distinguished, in region B that of head 2 and in region C that of head 3. The figure is intended to illustrate that a viewer cannot be expected to accept image reproduction by transverse track units without track post-control.

Figure 2 shows a specimen circuit diagram of a track post-control system for a transverse-track magnetic tape unit. The track post-control, as described in German Patent Application

DE-A 3421183, is intended to take place by the rotating head wheel 18 being displaceable in the direction of its rotating axis 18 in playback mode. This displacement is effected by an electro-mechanical convertor 15 which is controlled by an electronic circuit consisting of the following main groups:

A recognition circuit 10 in which size and phase position represented time-wise in a row of recurring pulses, e.g. horizontal sync pulses, are compared with a reference pulse source. The items of information obtained in this circuit are fed to the inputs 12 and 13 of the following correction circuit 11, in which the recognised phase errors are assigned to the individual magnetic heads in the error direction recognition stage 33. The correction circuit 11 also contains a memory arrangement 39 with an input storage 40, a transfer stage 42 and an output storage 41. By interim storage of the control data required for the post-control of the head wheel an exact adjustment in time between output of control voltages and the respective position of the rotating head wheel 18 can be achieved. These control voltages are fed at the output 14 of the correction circuit 11 via an integrator 16 to the electro-mechanical converter 15 for the post-control of the head wheel 18. The function of the individual circuit components listed in the circuit diagram is as follows:

The restored horizontal sync pulses HS are fed to the input 1 of the recognition circuit 10 during playback. From here these pulses pass to a first input of a phase comparison stage 2 whose output is connected to a first RC low pass filter 3 with relatively small time constant T_3 ($R_3 \times C_3$). The output of the first RC low pass filter 3 is connected on the one hand to the input of a second RC low pass filter 4 with high time constant T_4 ($R_4 \times C_4$) and on the other to two polarity separation stages 6 and 7. The first stage 6 allows only pulses of positive polarity to pass through, while the second stage 7 allows only negative pulses through. The output of the second low pass filter 4 is connected to the frequency control input of a voltage-controlled oscillator 5 with variable frequency (VCO), the output of which is connected to the second input of the phase comparison stage 2. The phase comparison stage 2 forms together with the 2 cascaded low pass filters 3 and 4 and the voltage-controlled oscillator 5 a known phase-locking loop (PLL) which generates an oscillator wave whose frequency is identical to the frequency of the reproduced horizontal sync pulses HS.

The output A of the first low pass filter or timer 3, which possesses a small time constant T_3 , consequently emits pulse-shaped items of information on short-time phase changes whose sign corresponds to the direction of the phase difference between the oscillator wave and the respective in-coming horizontal sync pulses.

These pulses are fed to parallel-connected inputs of two polarity separation stages 6 and 7 which have the task of processing the in-coming pulses according to their sign, i.e. the one separation stage responds only to positive pulses and the other only to negative pulses. The outputs of the polarity

separation stages 6 and 7 are connected to the trigger inputs of two monostable flip-flops 8 and 9 which operate as pulse shaping stages. The phase differences at their trigger inputs set the flip-flops 8 and 9 into their active state, so that they emit rectangular pulses of equal polarity and predetermined duration. The duration of the pulses is substantially less than one track duration (1.6 ms). The outputs (Q) of the monostable flip-flops 8 and 9 are connected to the inputs 12 and 13 of an error direction recognition stage 33 in the phase correction circuit 11. This phase correction circuit 11 comprises a further input 17 which is connected from the output of a pulse generator connected mechanically to the rotating shaft of the head wheel 18. This pulse generator can e.g. by electro-magnetic or opto-electronic means be designed so that it emits a pulse whenever a new magnetic head touches the magnetic tape. It therefore supplies to the input 17 six pulses per rotation of the head wheel 18. In addition the pulse which corresponds to the tape contact position of the first head K1 must be designed so that this head can be recognised, e.g. by a greater width of the pulse. In this way it becomes possible for the other heads (K2 to K6) also to be identified, in order to achieve a correct assignment of the azimuth angle of these heads to the memory of the phase errors for the purpose of correct track post-control. Each memory element therefore contains before the end of a head rotation the sign of the phase error of the head corresponding to it. During the next rotation of the head wheel 18 the stored data are outputted as a correction signal and passed to the converter 15. This preferably takes place about one half track duration (800 μ s) before tape contact of the head whose axial position has to be corrected.

The head wheel 18 is then displaced axially at each rotation until the amplitude of the phase errors is sufficiently small that the response or trigger threshold of the monostable flip-flops 8 and 9 is fallen short of.

To enable the phase errors to be assigned to the individual heads of the head wheel, the correction circuit 11 possesses a detector counter 19 whose first input 20 is connected to the pulse generator input 17. This detector counter 19 has a decoding stage which decodes e.g. the width-coded pulse of the first head K1 and supplies a corresponding pulse to a first output 21. In addition the detector counter supplies to a second output 22 pulses which are delayed by a half track duration (800 μ s) compared with the pulses supplied by the pulse generator. The detector counter 19 has in addition a first ring counter stage which comprises a reset input 23 and a counting or clock input 24. The reset input 23 is connected to the decoding output 21 and the clock input 24 to the input 20. The first ring counter stage has a further 6 first parallel outputs 25 which are switched one after the other for a whole track duration (1 600 μ s) to "high". In addition the detector counter 19 has a second ring counter stage whose reset input 26 is connected to the second decoding output 27 which supplies reset pulses one half track duration before the width-decoded pulses. The ring counter input 28 of the second ring counter stage is fed from the second output 22 and has six second

parallel outputs 29 which are switched successively to "high" one half track duration earlier than the first parallel outputs 25. In addition the first input 17 connected to the pulse generator feeds the control or toggle input T of a bistable flip-flop 30 whose setting input S is connected to the first decoding output 21 or else whose resetting input R is connected to the second decoding output 27, so that it can be synchronised at each rotation to the correct phase position. The output Q of the flip-flop 30 is connected on the one hand to a head switching control output 31 and on the other to an input 32 of an error direction recognition stage 33. The output signal at this output Q is a rectangular signal (head switching signal) whose period is twice the time of one track duration (1 600 μ s).

A high level of the output Q indicates the tape-head contact of an odd-numbered head (K1, K3, K5) with positive azimuthal offset, a low level L stands for the head contact of an even-numbered head (K2, K4, K6) with negative azimuthal offset (or vice-versa).

The second output 22 of the detector counter 19, which supplies pulses delayed by half a track duration, is connected by the output 34 to the resetting inputs R of the monostable flip-flops 8 and 9, so that the outputs Q supply pulses of half a track duration (800 μ s). These outputs Q are connected to the inputs 12 and 13 of the circuit 11 or to the inputs of the error direction recognition stage 33.

The error direction recognition circuit 33 therefore receives on the one hand pulses which correspond to the polarity of the phase jumps measured by the PLL loop and on the other at the input 32 the rectangular signal which corresponds to the azimuth angle of the head currently making contact with the tape. The track error direction can therefore be determined by correlation of these data. This means that the circuit 33 can supply at its output 37 three different signals. The first signal corresponds to a track post-run (negative error), the second to track equality (zero error) and the third to a track pre-run (positive error). This can be expressed either by means of digital words with two binary digits (bits) or a tri-state technique. The design can take the form e.g. of two inverters, 4 AND gates and 2 OR gates, which can also be combined, such as integrated double AND-OR-INVERT gates of the TTL 7451 type.

The outputs 37 of the track error direction recognition circuit 33 are connected to the data inputs 38 of a double memory unit 39. The latter consists of an input storage 40, an output storage 41 and a controllable data transfer stage 42. The address inputs 43 of the input storage 40 are connected to the first parallel outputs 25 of the detector counter 19, so that the error direction data are written successively into the storage cells (2 bit) of the input storage 40 corresponding to the number of heads (in this case 6). The data transfer stage 42 connects during a short time span the data outputs of these storage cells to the data inputs of the corresponding number of storage positions of the output storage 41. The data of the input storage 40 are thus transferred serially into the output

storage 41. This transfer takes place by means of the reset pulse of the second ring counter stage at the output 27 of the detector counter 19, i.e. of the occurring inverted signal of the output 22. The output 27 is for this purpose connected to the input 44 of the storage assembly 39.

The address inputs 45 of the output storage 41 are connected to the 6 parallel outputs 29 of the detector counter 19, so that the data contents of all its 6 storage cells appear successively on its 2 data outputs 46 and 47. These data contents are outputted delayed by $5 \frac{1}{2}$ track durations with respect to the recognition procedure, so that the correction procedure takes place $\frac{1}{2}$ track duration before the next recognition procedure of the same head. The result of this next recognition procedure can thus take account of the correction result of the preceding recognition procedure of the same head. The data outputs 46 and 47 of the output storage 41 are connected to control inputs of two electronic switches 48 and 49 connected in series. The first switch 48 connects the mid-point 50 to a positive voltage source 51 (- UB) and the second switch 49 connects the mid-point 50 to - UB. The mid-point is also connected to an input of an analog/adder stage 52, the other input of which is connected to the output of a ramp or saw-tooth generator 53. The generator 53 is used for stills mode or image search run. The output of the adder stage 52 is connected by the control output 14 to the input of the integrator 16. The integrator 16 connected to the output of the adder stage 52 plays the role of an analog store which maintains the pulse voltage delivered at the mid-point 50 of the switches 48 and 49.

The ramp generator 53, which supplies saw-tooth-shaped output signals, is switched on and off by an operating mode selection stage 54. The input of this stage 54 is connected to the input 55 of the circuit 11 and is fed with an operating mode control signal. This signal is either pulse-type (the operating mode selection stage 54 then contains a bistable flip-flop) or binary, i.e. transmitted by two levels (H, L).

During stills mode the ramp generator 53 feeds the electro-mechanical converter 15 via the adder stage 52 and integrator 16 with a saw-tooth-shaped voltage curve by means of which a linear-in-time movement of the head drum 18 along the stationary magnetic tape is produced. This linear head drum movement lasts for example slightly more than one frame, i.e. covers some 12 - 15 track durations. Limitation of the displacement of the head to 12 tracks means that slightly less than one frame is reproduced. It is critical for the reproduction of a still that the signal contain a standard image flyback sync signal. To achieve this, the magnetic tape is transported by the capstan drive until the magnetic head K1 recognises on a track an image flyback sync signal. Only then is the magnetic tape stopped. A further output 56 of the ramp generator 53 causes fade-out of the video signal during the return of the head drum.

Figure 3 shows a flow diagram of the apparatus according to Figure 2 in normal playback mode.

The track post-control starts with the head 1 whose tape contact is marked by a broad pulse. After head 1 has read the first horizontal sync pulse, the latter is compared with the phase of the oscillator wave. The comparison serves to determine whether there is a phase error the degree of which lies above a permitted limit value. If this is the case, one of the monostable flip-flops (8, 9) emits a pulse from which the direction, i.e. the sign of the detected phase error, is determined.

The size of the phase error then no longer plays a role, because the storage and the correction take place by quantity. In each head rotation cycle only a predetermined quantity of correction signals is added to the previous ones and stored for each head. If the direction has been determined, the predetermined quantity is stored as a unit with its sign and the measurement passes to the next head. If no phase error is present with the first head K1, this state is stored. Phase error recognition for head 2 then follows. Finally it is enquired whether all the heads K1 to K6 have passed through the cycle. If this is not the case, the phase error determination with subsequent sign direction determination is continued and the new values stored. This procedure is repeated until all 6 heads K1 to K6 have passed through the cycle. If this is the case, the stored correction values with their signs are supplied to the electro-mechanical converter 15 in the next cycle and a new phase error measurement cycle follows in the manner described above until the phase error detectors no longer emit a detectable signal and therefore fall below the trigger threshold of the monostable flip-flops 8, 9. From this point in time the correction values last stored remain critical for the axial displacement of the head wheel. If new faults or breakdowns occur during the reproduction, the procedure described is repeated again from the beginning until the desired end result, namely perfect reproduction of the recorded video signal, is achieved.

Figure 4 shows a simplified flow diagram for stills or search run mode. If stills mode is selected, it is established whether a vertical sync pulse is present on the track which is read by head 1. If this is not the case, the magnetic tape is transported further until head 1 has found a vertical synchronous signal pulse. If this is the case, the capstan axis is held in position. The ramp or saw-tooth-shaped signal is then applied.

The head wheel reads some 16 - 20 successive tracks while it is moved by the electro-mechanical converter past the stationary tape at uniform speed for a period of some 32 ms (20 tracks per 1.6 ms). The return to the stored initial position occupies some 3 - 5 track durations of 1.6 ms each, in which time the video signal must be scanned.

With search run the tape speed must be determined and the speed V of the advancement or retraction of the head wheel added thereto, i.e. the slope of the saw-tooth-shaped signal must be modified with the value of the tape speed.

Figure 5 gives an overview of flow diagrams and signal shapes

from the circuit diagram of Figure 2.

Figure 5A shows the signal shape of the voltage at the output of the first timer 3A, which because of the azimuthal offset can have different directions for identical track errors. On the intervention of the second K2 a negative phase jump is displayed, while with head 3 a positive phase jump is discernible. For example, the time elapsing between the last line sync pulse which has been read by head 1 and the first line sync pulse of head 2 can be some 62 μ s. In the transition from head 2 to head 3 a positive phase error is obtained, which corresponds e.g. to a time of 66 μ s. In Figures 5B and 5C are seen the pulses supplied by the polarity separation and limitation stages 6 and 7, which pass to the trigger inputs T of the monostable flip-flops 8 and 9. Figure 5D shows the reset pulses supplied by the output 22 of the detector counter 19 to the reset inputs R of the flip-flops 8 and 9 in order to reset them before the heads are switched. They are offset by half a track duration with respect to the pulses supplied by the head wheel pulse generator.

Figures 5E and 5F therefore show pulses at the input of the error direction recognition stage 33, which show phase errors, with 5E indicating a positive and 5F a negative phase error. The pulses have identical amplitude for identical pulse duration, which corresponds to half (800 μ s) of a track duration ($TS = 25 H = 1\ 600\ \mu$ s).

In Figure 5G is shown the pulse train supplied by the pulse generator of the head drum to the input 17 of the circuit 11, where on tape contact of the first head (K1) a pulse I coded in its width (T_k) is supplied.

In Figure 5H is shown the rectangular-shaped head switching control signal (V_{s1}) emitted by the bistable flip-flop 30, which is also fed to the error direction recognition stage 33 at the input 32 for correlation purposes.

In Figures 5K and 5L are shown the output signals of the output storage 41, which occur at the outputs 47 and 46 and which serve to control the two switches 48 and 49. These signals V 47 and V 48 are delayed by the memory unit 39 by 5.5 track durations with respect to the phase error pulses occurring at the output A of the PLL loop, so that the correction is carried out during the following head rotation. The correction pulse after integration in the integration circuit 16 is shown in Figure 5M.

C L A I M S



1. Track post-controlled magnetic tape unit comprising at least 2 magnetic heads moving transversely to the tape direction and disposed on a rotating head wheel (18), the air gaps of the said heads having an azimuth angle which alternates symmetrically around a mean axis, the said heads being staggered at the head wheel periphery in such a way that the scanning of recorded signals of a magnetic track is performed by one head at a time and the position of the magnetic heads relative to the tape being controlled in dependence on an established phase error, characterised in that track control variables for the individual magnetic heads are derived from the direction and the size of phase errors (A) occurring in the scanned signal (HS1) after a change of track and are inputted into a memory (39), and that the control variables during the next head rotation are according to the number of heads outputted sequentially to a control device (15, 16) for adjustment of the head wheel (18) in the axial direction and/or a change in the tape speed.
2. Unit according to claim 1, characterised in that for the detection of phase errors a PLL circuit (2-5) is provided, to the input (1) of which there are supplied out of the playback signal continually repeating pulse trains, such as e.g. horizontal synchronous pulses (HS), and which is part of a detection circuit (10) to which is series-connected a correction circuit (11) which performs the storage and output of the control variables.
3. Unit according to claim 1, characterised in that for the adjustment of the head wheel (18) in the axial direction an electro-mechanical converter (15) is provided.
4. Unit according to claim 1, characterised in that the control variable for the adjustment of the head wheel (18) is supplied to the electro-mechanical converter (15) via an integrator (16).
5. Unit according to claim 1, characterised in that for stationary image reproduction with a stationary magnetic tape a saw-tooth-shaped control variable is fed additionally to the electro-mechanical converter (15).
6. Unit according to claim 1, characterised in that for image searching mode at increased tape speed a saw-tooth-shaped control variable is supplied additionally to the electro-mechanical converter (15).

7. Unit according to claim 2, characterised in that low-pass filters (3, 4) connected in series in the PLL circuit (2 - 5) are provided with a first time constant and a second, greater time constant, the first time constant being selected so that the phase shifts of the horizontal synchronous signal occurring during the head switchings at its output (A) are converted into short pulses.
8. Unit according to any one of claims 1, 2, 3, 4 and 7, characterised in that the output (A) of the first low-pass filter (3) is connected to the shunt-connected inputs of 2 polarity separation stages (6, 7), the outputs (C, B) of which each activate a monostable flip-flop (8, 9), which in the presence of phase errors supply output pulses of equal amplitude and equal duration.
9. Unit according to claim 8, characterised in that the duration of the output pulses of the monostable flip-flops (8, 9) is less than one track period, preferably half of one track period.
10. Unit according to any one of claims 1 - 9, characterised in that the head wheel is connected to a pulse generator which supplies a pulse at each tape-head contact of the individual magnetic heads, the pulse for the first head being distinguished from the pulses for the other magnetic heads, e.g. by its pulse length.
11. Unit according to claim 10, characterised in that the pulses derived from the pulse generator are evaluated in a detector (19) in such a way that the pulse for the tape-head contact of the first head can be used as a reset pulse.
12. Unit according to claim 11, characterised in that the pulse train emitted by the pulse generator is applied to the control input of a bistable toggle switch (30), the pulse evaluated by the detector (19) for the tape-head contact of the first magnetic head being supplied as a reset pulse to the toggle switch (30) so that the output (Q) of the toggle switch (30) supplies rectangular pulses which serve on the one hand at the output (31) of the circuit (11) as control signals for electronic switchings in the unit and on the other for correlating the polarity of the pulses derived from the phase errors with the azimuth angles of the individual magnetic heads in the error direction detection stage (33).



* C L H S *

13. Unit according to claim 12, characterised in that in the detector counter (19) the pulse train supplied by the pulse generator is converted into a pulse train delayed by half a track period, this pulse train being fed to the reset inputs of the monostable flip-flops (8, 9).
14. Unit according to claim 13, characterised in that the detector counter (19) is assigned a first ring counter and a second ring counter.
15. Unit according to claims 13 and 14, characterised in that the pulse train supplied by the pulse generator feeds the counting input of the first ring counter the parallel outputs (25) of which are connected to the address inputs (43) of an input storage (40), and that the pulse train delayed by half a track period feeds the counting input of the second ring counter the parallel outputs (29) of which are connected to the address inputs (25) of an output storage (41).
16. Unit according to claim 15, characterised in that the outputs of the error direction detection stage (33) are connected to the data inputs of the input storage (40) and that the data outputs of the input storage (40) are connected via a controlled data transfer stage (42) to the data outputs of the output storage (41).
17. Unit according to claim 16, characterised in that the output storage (41) comprises two outputs (46, 47) which are switched to "high" for track errors of opposite direction and which control two series-connected switches (48, 49) which are disposed between a voltage source (+ UB) and (- UB), and that the mid-point (50) of the switches is connected by the control output of the track post-control circuit (11) to the input of the integrating switch (16) and supplies correction signals to the converter (15).
18. Unit according to claims 5, 6 and 17, characterised in that the signals from the mid-point of the switches (50) are combined with the saw-tooth signals in an adder stage (52).

