

Description

The invention relates to a filter arrangement comprising a balanced amplifier having an inverting input, a non-inverting input, an inverting output and a non-inverting output, a first input terminal and a second input terminal, a first feedback circuit comprising a first capacitor and arranged between the non-inverting output and the inverting input, a second feedback circuit comprising a second capacitor substantially identical to the first capacitor and arranged between the inverting output and the non-inverting input, a transconductor circuit with variable transconductance comprising two inputs connected to the input terminals of the filter arrangement and two outputs coupled to the inverting and non-inverting inputs of the balanced amplifier.

Such a filter arrangement is known from United States Patent Specification 4,509,019. Said filter arrangement constitutes an integrator. Between the two input terminals and the two inputs of its amplifier two MOS resistors are arranged. The resistance values of these resistors can be adjusted by means of a control voltage applied to the gate electrode. This control voltage enables the RC-time constant of the resistor and the capacitor to be adjusted to the desired value.

A balanced input voltage is applied to the first input terminal and the second input terminal of the filter arrangement and a balanced output voltage is available on the inverting output and the non-inverting output of the amplifier. This output voltage is substantially exempt of even-order harmonic distortion, which is caused *inter alia* by non-linearities of the MOS resistors. This is because such distortions are cancelled as a result of the balanced drive and the symmetrical construction of the arrangement.

A drawback of this known arrangement is that the time constant of the arrangement is only adjustable over a comparatively small range, because the resistance values of the MOS transistors can be varied only over a comparatively small range.

Therefore, it is the object of the invention to provide a filter arrangement whose time constant can be adjusted over a comparatively wide range. In accordance with the invention a filter arrangement of the type defined in the opening paragraph is characterized in that the transconductor circuit comprises a plurality of active devices each having a control input terminal and first and second output terminals, the control input terminals of at least two of said active devices being connected to the inputs of the transconductor circuit, the first output terminals of the at least two active devices being connected together and the second output terminals being coupled respectively to the outputs of the transconductor circuit.

A transconductance circuit is a voltage-con-

trolled current source by means of which a balanced input voltage is converted into a balanced output current. The proportionality factor between the output current and the input voltage is given by the transconductance ($1/R$). Generally, this transconductance can be varied over a comparatively wide range, thus also enabling the time constant of the filter arrangement to be varied over a comparatively wide range.

A first embodiment of a filter arrangement in accordance with the invention is characterized in that a load circuit is arranged between the outputs of the transconductance circuit which load circuit comprises two current-source transistors whose collectors are connected to the outputs of the transconductance circuit and whose bases are connected to a common control input which is coupled to the junction point of two resistors arranged between the outputs of the transconductance circuit. The output currents of the transconductance circuits are fed directly to the inputs of the amplifier. The load circuit accurately defines the direct voltages on the outputs and ensures that only the signal currents are transferred to the outputs.

A second embodiment of the filter arrangement in accordance with the invention may be characterized in that the transconductance circuit comprises a differential amplifier with two transistors whose bases are connected to the input terminals, whose collectors are connected to the outputs of the transconductance circuit, and whose emitters are connected to a common current source whose current is variable. A differential amplifier is the simplest form of a transconductance circuit. The transconductance of such a circuit can be varied by varying the current supplied by the common emitter-current source. In such a transconductance circuit the signal currents increase as a linear function of the input voltage over a comparatively small range only, so that the transconductance is constant only over a comparatively small range of input voltages. A larger linear input voltage range of the transconductance circuit can be obtained in a third embodiment of a filter arrangement in accordance with the invention, characterized in that the transconductance circuit comprises two differential amplifiers each comprising two transistors which have unequal emitter areas and whose emitters are connected to a common current source whose current is variable, of which two differential amplifiers the bases are interconnected and the collectors of two transistors with different emitter areas are connected to each other to an output of the transconductance circuit. In the case of a suitable choice of the ratio between the emitter areas the linear range of this transconductor is substantially five times as large as that of a single differential amplifier.

An even larger linear range of the transconduc-

tance circuit can be obtained, if the filter arrangement in accordance with a fourth embodiment is characterized in that the transconductance circuit comprises a differential amplifier with two transistors, whose bases are connected to the input terminals, whose collectors are connected to the outputs of the transconductance circuit, and whose emitters are connected to a common current source whose current is variable, and in that a voltage divider is arranged between the bases of the two transistors and has its junction point connected to the bases of two transistors whose emitters are connected to the common current source and whose collectors are connected to the outputs of the transconductance circuit.

Instead of bipolar transistors the transconductance circuit may comprise field-effect transistors. In accordance with a fifth embodiment the transconductance circuit may then be characterized in that it comprises a first differential amplifier with two field-effect transistors whose source electrodes are connected to a first common current source and whose drain electrodes are connected to the outputs of the transconductance circuit, and a second differential amplifier arranged in parallel with said first differential amplifier and comprising two field-effect transistors whose source electrodes are connected to a second common current source and whose drain electrodes are cross-coupled to the drain electrodes of the field-effect transistors of the first differential amplifier.

A sixth embodiment of a filter arrangement in accordance with the invention is characterized in that the balanced amplifier comprises two transistors arranged as a differential pair, whose bases are coupled to the non-inverting input and the inverting input and whose collectors are connected to the inverting output and the non-inverting output of the amplifier, between which two outputs a load circuit is arranged comprising two current-source transistors whose collectors are connected to the inverting output and the non-inverting output of the amplifier and whose bases are connected to a common control input which is coupled to the junction point between two load resistors arranged between the outputs of the amplifier.

Generally, such a filter arrangement in accordance with the invention is utilized in circuits in which it is coupled to a second filter arrangement. In accordance with a further embodiment the input terminals of the second filter arrangement are connected to the tapplings provided on the load resistors of the load circuit of the amplifier of the first filter arrangement.

Embodiments of the invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which

Fig. 1 is a basic diagram of a filter arrangement

in accordance with the invention,

Fig. 2 shows a transconductance circuit for use in the arrangement shown in Fig. 1,

Fig. 3 shows another transconductance circuit for use in the arrangement of Fig. 1,

Fig. 4 shows yet another transconductance circuit for the arrangement of Fig. 1,

Fig. 5 shows an amplifier for use in the arrangement of Fig. 1, and

Fig. 6 shows two filter arrangements in accordance with the invention coupled to each other.

Fig. 1 shows the basic diagram of a filter arrangement in accordance with the invention. The filter arrangement comprises an amplifier 1 having a non-inverting input 2, an inverting input 3, an inverting output 4 and a non-inverting output 5. Further, the filter arrangement comprises a transconductance circuit 10, briefly referred to as transconductor. The simplest form of such a transconductor 10 is a differential amplifier comprising two transistors T_1 and T_2 whose bases are connected to the input terminals 6 and 7 of the filter arrangement and whose emitters are connected to an adjustable common current source I_1 . The collectors of these transistors constitute the outputs 11 and 12 of the transconductor and are connected to the inputs 2 and 3 of the amplifier 1. Between the outputs 11 and 12 of the transconductor 10 a load circuit is arranged, comprising two substantially identical resistors R_1 and R_2 , whose junction point is connected to the common base of two PNP transistors T_3 and T_4 by means of a diode, the emitters of said PNP transistors being connected to the positive power-supply terminal and the collectors to the outputs 11 and 12 of the transconductor.

It is to be noted that, instead of by means of a diode, the junction point between the resistors R_1 and R_2 may also be connected to the common base of the transistors T_3 and T_4 by means of a transistor whose control electrode is at a reference voltage of an operational amplifier of which one input is connected to the junction point between the resistors R_1 , R_2 and the other input is at a reference voltage.

By means of the resistors R_1 and R_2 and the diode D_1 the common base of the transistors T_3 and T_4 is driven in such a way that the transistors T_3 and T_4 supply the direct currents for the transistors T_1 and T_2 . The direct voltages on the outputs 11 and 12 of the transconductor are then equal to the positive power-supply voltage minus one diode voltage and one base-emitter voltage. As the direct voltages on the outputs 11 and 12 are equal no direct current will flow through the resistors R_1 and R_2 . A balanced input voltage is applied to the input terminals 6 and 7 of the filter arrangement. The transconductor 10 converts this input voltage into two signal currents of opposite phase which are

superimposed on the direct currents through the transistors T_1 and T_2 . The signal current through the resistors R_1 and R_2 is only very small because the negative-feedback amplifier 1 ensures that the signal voltage between inputs 2 and 3 is very low. The signal currents flowing into the collectors of the transistors T_1 and T_2 are applied almost fully to the capacitors C_1 and C_2 on account of the negative feedback of the amplifier 1. Consequently, an integrated balanced output voltage will appear on the outputs 4 and 5 of the amplifier 1. The even-order harmonic distortions caused by the nonlinearities of the arrangement substantially cancel each other owing to the symmetrical construction of the filter arrangement and the balanced drive. As a result of this, the range over which the output voltage increases as a linear function of the input voltage is comparatively large. The time constant of the arrangement is equal to the product of the capacitance of the capacitors C_1 and C_2 and the inverse of the transconductance of the transconductor 10. The transconductance of the transconductor can then be varied over a wide range by varying the current of the current source I_1 , so that a large range of time constants can be obtained.

Fig. 2 shows an example of a transconductor for use in the arrangement shown in Fig. 1. Identical parts bear the same reference numerals. It is to be noted that this transconductor is known per se from the article "Bipolar Integration of analog gyrator and laguerre type filters (transconductor-capacitor filters)" in Proceedings ECCTD '83, September 1983, pages 107-110. The transconductor 10 comprises a first differential amplifier which is constituted by two transistors T_5 and T_6 whose bases are connected to the input terminals 6 and 7, whose emitters are connected to a common current source I_1 , and whose collectors are connected to the outputs 11 and 12. The emitter area of the transistor T_5 is four times as large as that of the transistor T_6 . Further, the transconductor 10 comprises a second differential amplifier comprising two transistors T_7 and T_8 having their bases connected to the bases of the transistors T_5 and T_6 , their collectors to the collectors of the transistors T_5 and T_6 , and their emitters to the common current source I_2 which is identical to the current source I_1 . The transistor T_8 has an emitter area which is four times as large as that of the transistor T_7 . For this ratio between the emitter areas of the transistors the linear range of the transconductor 10 is found to be approximately five times as large as that of the transconductor shown in Fig. 1.

Fig. 3 shows another example of a transconductor for use in the arrangement shown in Fig. 1. It is to be noted that this transconductor is described in European Patent Application EP-A1-0 234 655,

published 02, 09, 87. The transconductor 10 comprises a differential amplifier, comprising two transistors whose bases are connected to the input terminals, whose emitters are connected to a common current source I_5 , and whose collectors are connected to the outputs 11 and 12 of the transconductor. A voltage divider comprising two substantially identical resistors R_3 and R_4 is arranged between the bases of the transistors T_{10} and T_{11} . The junction point between the resistors R_3 and R_4 is connected to the bases of two transistors T_{12} and T_{13} whose emitters are connected to the emitters of the transistors T_{10} and T_{11} and whose collectors are connected to the outputs 11 and 12. The emitter areas of these transistors T_{12} and T_{13} are twice as large as those of the transistors T_{10} and T_{11} . For this ratio between the emitter areas the linear voltage range of the transconductor is found to be approximately twice as large as that of the transconductor shown in Fig. 2.

For transconductors constructed by means of bipolar transistors the transconductance is generally proportional to the current of the supply-current source. By making this current programmable, for example in a binary manner, it is possible to construct programmable filters.

Fig. 4 shows another transconductor for use in the arrangement shown in Fig. 1. Identical parts bear the same reference numerals as in Fig. 2. This transconductor comprises MOS transistors instead of bipolar transistors. It is to be noted that this transconductor is known per se from the article "Analog Integrated Filters or Continuous Time Filters for LSI and VLSI", ESSCIRC Sept. '85, page 292. The transconductor 10 comprises a first differential amplifier comprising two MOS transistors T_5 and T_6 whose gates are connected to the input terminals 6 and 7, whose source electrodes are connected to a first current source I_2 , and whose drain electrodes are connected to the outputs 11 and 12. The transconductor 10 further comprises a second differential amplifier comprising two MOS transistors T_7 and T_8 whose source electrodes are connected to a second current source I_3 . The gate of the transistor T_7 is connected to that of the transistor T_5 and the gate of the transistor T_8 is connected to that of the transistor T_6 . The drain of the transistor T_7 is connected to the drain of the transistor T_6 and the drain of the transistor T_8 is connected to the drain of the transistor T_5 . The transistors T_5 , T_6 , T_7 and T_8 are identical to each other. This transconductor also has a comparatively large linear voltage range.

It is to be noted that instead of the transconductors shown other transconductors may be employed.

Fig. 5 shows a suitable example of an amplifier 1 for use in the filter arrangement shown in Fig. 1.

The amplifier 1 comprises a differential pair with the transistors T_{21} and T_{22} whose bases constitute the non-inverting input 2 and the inverting input 3, whose collectors are connected to the positive power-supply terminal, and whose emitters are connected to the bases of two transistors T_{25} and T_{26} arranged as a differential pair, whose collectors are cross-coupled to the bases and whose emitters are connected to a current source I_6 via a common resistor R_5 . Further, the amplifier comprises two transistors T_{23} and T_{24} arranged as a differential pair, whose bases are connected to the emitters of the transistors T_{21} and T_{22} and whose emitters are connected to the current source I_6 . The collectors of the transistors T_{23} and T_{24} constitute the inverting output 4 and the non-inverting output 5 of the amplifier. A load circuit is arranged between the outputs 4 and 5 and comprises a PNP transistor T_{26} whose emitter is connected to the positive power-supply terminal, whose collector is connected to the output 4, and whose base is connected to the base of a PNP transistor T_{28} whose emitter is connected to the positive power-supply terminal and whose collector is connected to the output 5. The common base of the transistors T_{27} and T_{28} is connected to the junction point between two identical resistors R_6 and R_7 via a diode D_2 , which resistors are arranged between the outputs 4 and 5. Instead of a diode D_2 it is possible to use a transistor whose base is at a reference voltage or an operational amplifier of which one input is connected to the junction point between the resistors R_6 and R_7 and of which the other input is at a reference voltage. It is to be noted that this amplifier is the subject of a Patent Application (PHN 11.936) filed simultaneously with the present Application. In this respect it is observed only that the balanced input voltage applied to the bases 2 and 3 is converted into a balanced current by the differential pair T_{21} , T_{22} , the differential pair T_{25} , T_{26} providing an increased slope of the arrangement. The differential pair T_{23} , T_{24} provides additional current gain, which gain is defined by the value of the resistor R_5 which determines the ratio between the bias currents of the differential pair T_{23} , T_{24} and the differential pair T_{25} , T_{26} . The load circuit ensures that the direct voltages on the outputs 4 and 5 remain accurately constant. The transistors T_{27} and T_{28} compensate for the bias currents of the transistors T_{23} and T_{24} , so that only signal currents appear on the outputs 4 and 5. Since the signal currents on the outputs 4 and 5 remain accurately balanced, no signal voltage will appear on the junction point between the resistors R_6 and R_7 . Therefore, the junction point constitutes a virtual signal earth.

Fig. 6 shows two filter arrangements in accordance with the invention coupled to each other.

Identical parts bear the same reference numerals as in Fig. 1, the parts of the second amplifier arrangement being primed. The amplifiers 1 and 1' each comprise a load circuit identical to the load circuit of the amplifier shown in Fig. 5, the only difference being that the load resistors R_6 and R_7 are tapped. The input terminals 5' and 7' of the second filter arrangement are connected to these tapplings of the first filter arrangement. The full signal voltage appears across the load resistors R_6 and R_7 . In order to prevent the transconductor 10' from being overdriven only a fraction of this voltage may be applied to the input terminals 6' and 7' of the second filter arrangement. It is to be noted that the input terminals of the second filter arrangement may also be cross-coupled to the outputs of the first amplifier arrangement.

The invention is not limited to the embodiments shown. Within the scope of the invention many variants are conceivable to those skilled in the art. For example, in each embodiment shown one transconductor is connected to the inputs of the amplifier. However, it is alternatively possible to connect a plurality of transconductors to the inputs of the amplifier, another balanced input signal being applied to each transconductor. In addition, it is possible to combine the load circuits of these transconductors. Moreover, it is obvious that the outputs of one or more similar filter arrangements may be connected directly to the inputs of an amplifier.

Claims

1. A filter arrangement comprising a balanced amplifier (1) having an inverting input (3), a non-inverting input (2), an inverting output (4) and a non-inverting output (5), a first input terminal (6) and a second input terminal (7), a first feedback circuit comprising a first capacitor (C_2) and arranged between the non-inverting output (5) and the inverting input (3), a second feedback circuit comprising a second capacitor (C_1) substantially identical to the first capacitor (C_2) and arranged between the inverting output (4) and the non-inverting input (2), a transconductor circuit (10) with variable transconductance comprising two inputs connected to the input terminals (6,7) of the filter arrangement and two outputs (11,12) coupled to the inverting (3) and non-inverting (2) inputs of the balanced amplifier (1), characterized in that the transconductor circuit (10) comprises a plurality of active devices (T_1, T_2) each having a control input terminal and first and second output terminals, the control input terminals of at least two of said active devices being connected to the inputs (6,7) of the transconductor circuit (10), the first output terminals of the at



The amplifier 1 comprises a differential pair with the transistors T_{21} and T_{22} whose bases constitute the non-inverting input 2 and the inverting input 3, whose collectors are connected to the positive power-supply terminal, and whose emitters are connected to the bases of two transistors T_{25} and T_{26} arranged as a differential pair, whose collectors are cross-coupled to the bases and whose emitters are connected to a current source I_6 via a common resistor R_5 . Further, the amplifier comprises two transistors T_{23} and T_{24} arranged as a differential pair, whose bases are connected to the emitters of the transistors T_{21} and T_{22} and whose emitters are connected to the current source I_6 . The collectors of the transistors T_{23} and T_{24} constitute the inverting output 4 and the non-inverting output 5 of the amplifier. A load circuit is arranged between the outputs 4 and 5 and comprises a PNP transistor T_{26} whose emitter is connected to the positive power-supply terminal, whose collector is connected to the output 4, and whose base is connected to the base of a PNP transistor T_{28} whose emitter is connected to the positive power-supply terminal and whose collector is connected to the output 5. The common base of the transistors T_{27} and T_{28} is connected to the junction point between two identical resistors R_6 and R_7 via a diode D_2 , which resistors are arranged between the outputs 4 and 5. Instead of a diode D_2 it is possible to use a transistor whose base is at a reference voltage or an operational amplifier of which one input is connected to the junction point between the resistors R_6 and R_7 and of which the other input is at a reference voltage. It is to be noted that this amplifier is the subject of a Patent Application (PHN 11.936) filed simultaneously with the present Application. In this respect it is observed only that the balanced input voltage applied to the bases 2 and 3 is converted into a balanced current by the differential pair T_{21} , T_{22} , the differential pair T_{25} , T_{26} providing an increased slope of the arrangement. The differential pair T_{23} , T_{24} provides additional current gain, which gain is defined by the value of the resistor R_5 which determines the ratio between the bias currents of the differential pair T_{23} , T_{24} and the differential pair T_{25} , T_{26} . The load circuit ensures that the direct voltages on the outputs 4 and 5 remain accurately constant. The transistors T_{27} and T_{28} compensate for the bias currents of the transistors T_{23} and T_{24} , so that only signal currents appear on the outputs 4 and 5. Since the signal currents on the outputs 4 and 5 remain accurately balanced, no signal voltage will appear on the junction point between the resistors R_6 and R_7 . Therefore, the junction point constitutes a virtual signal earth.

Fig. 6 shows two filter arrangements in accordance with the invention coupled to each other.

Identical parts bear the same reference numerals as in Fig. 1, the parts of the second amplifier arrangement being primed. The amplifiers 1 and 1' each comprise a load circuit identical to the load circuit of the amplifier shown in Fig. 5, the only difference being that the load resistors R_6 and R_7 are tapped. The input terminals 5' and 7' of the second filter arrangement are connected to these tapings of the first filter arrangement. The full signal voltage appears across the load resistors R_6 and R_7 . In order to prevent the transconductor 10' from being overdriven only a fraction of this voltage may be applied to the input terminals 6' and 7' of the second filter arrangement. It is to be noted that the input terminals of the second filter arrangement may also be cross-coupled to the outputs of the first amplifier arrangement.

The invention is not limited to the embodiments shown. Within the scope of the invention many variants are conceivable to those skilled in the art. For example, in each embodiment shown one transconductor is connected to the inputs of the amplifier. However, it is alternatively possible to connect a plurality of transconductors to the inputs of the amplifier, another balanced input signal being applied to each transconductor. In addition, it is possible to combine the load circuits of these transconductors. Moreover, it is obvious that the outputs of one or more similar filter arrangements may be connected directly to the inputs of an amplifier.

Claims

1. A filter arrangement comprising a balanced amplifier (1) having an inverting input (3), a non-inverting input (2), an inverting output (4) and a non-inverting output (5), a first input terminal (6) and a second input terminal (7), a first feedback circuit comprising a first capacitor (C_2) and arranged between the non-inverting output (5) and the inverting input (3), a second feedback circuit comprising a second capacitor (C_1) substantially identical to the first capacitor (C_2) and arranged between the inverting output (4) and the non-inverting input (2), a transconductor circuit (10) with variable transconductance comprising two inputs connected to the input terminals (6,7) of the filter arrangement and two outputs (11,12) coupled to the inverting (3) and non-inverting (2) inputs of the balanced amplifier (1), characterized in that the transconductor circuit (10) comprises a plurality of active devices (T_1, T_2) each having a control input terminal and first and second output terminals, the control input terminals of at least two of said active devices being connected to the inputs (6,7) of the transconductor circuit (10), the first output terminals of the at



least two active devices (T_1, T_2) being connected together and the second output terminals being coupled respectively to the outputs (11,12) of the transconductor circuit (10).

2. A filter arrangement as claimed in Claim 1, characterized in that a load circuit is arranged between the outputs (11,12) of the transconductor circuit (10), which load circuit comprises two current-source transistors (T_3, T_4) whose collectors are connected to the outputs (11,12) of the transconductance circuit (10) and whose bases are connected to a common control input which is coupled to the junction point of two resistors (R_1, R_2) arranged between the outputs of the transconductance circuit.

3. A filter arrangement as claimed in Claim 1 or 2, characterized in that the transconductance circuit comprises a differential amplifier with two transistors (T_1, T_2) whose bases are connected to the input terminals (6,7), whose collectors are connected to the outputs (11,12) of the transconductance circuit (10), and whose emitters are connected to a common current source (Y_1) whose current is variable.

4. A filter arrangement as claimed in Claim 3, characterized in that a voltage divider (R_3, R_4) is arranged between the bases of the two transistors (T_{10}, T_{11}) and has its junction point connected to the bases of two transistor (T_{12}, T_{13}) whose emitters are connected to the common current source (Y_5) and whose collectors are connected to the outputs (11,12) of the transconductance circuit.

A filter arrangement as claimed in Claim 1 or 2, characterized in that the transconductance circuit (10) comprises two differential amplifiers ($T_5, T_6; T_7, T_8$) each comprising two transistors which have unequal emitter areas and whose emitters are connected to a common current source ($Y_2; Y_3$) current is variable, of which two differential amplifiers the bases are interconnected and the collectors of two transistors with different emitter areas are connected to each other and to an output (11,12) of the transconductance circuit (10).

6. A filter arrangement as claimed in Claim 1 or 2, characterized in that the transconductance circuit comprises a first differential amplifier with two field-effect transistors (T_5, T_6) whose source electrodes are connected to a first common current source (Y_2) and whose drain electrodes are connected to the outputs (11,12) of the transconductance circuit, and a

second differential amplifier arranged in parallel with said first differential amplifier and comprising two field-effect transistors (T_7, T_8) whose source electrodes are connected to a second common current source (Y_3) and whose drain electrodes are cross-coupled to the drain electrodes of the field-effect transistors of the first differential amplifier.

7. A filter arrangement as claimed in Claim 1, 2, 3, 4, 5 or 6, characterized in that the balanced amplifier comprises two transistors (T_{21}, T_{22}) arranged as a differential pair, whose bases are coupled to the non-inverting input (2) and the inverting input (3) and whose collectors are connected to the inverting output (4) and the non-inverting output (5) of the amplifier, between which two outputs a load circuit is arranged comprising two current-source transistors (T_{27}, T_{28}) whose collectors are connected to the inverting output (4) and the non-inverting output (5) of the amplifier and whose bases are connected to a common control input which is coupled to the junction point between two load resistors (R_6, R_7) arranged between the outputs (4,5) of the amplifier.

8. A filter arrangement as claimed in Claim 7, characterized in that the filter arrangement is coupled to a second filter arrangement, the input terminal (6',7') of the second filter arrangement being connected to tappings provided on the load resistors of the load circuit of the amplifier of the first filter arrangement.

Revendications

1. Dispositif de filtrage comportant un amplificateur équilibré (1) muni d'une entrée inverseuse (3), d'une entrée non inverseuse (2), d'une sortie inverseuse (4) et d'une sortie non inverseuse (5), d'une première borne d'entrée (6) et d'une deuxième borne d'entrée (7), d'un premier circuit de couplage à réaction comportant un premier condensateur (C_2) et disposé entre la sortie non inverseuse (5) et l'entrée inverseuse (3), d'un deuxième circuit de couplage à réaction comportant un deuxième condensateur (C_1) qui est pratiquement identique au premier condensateur (C_2) et disposé entre la sortie inverseuse (4) et l'entrée non inverseuse (2), d'un circuit de conductance de transfert variable (10) muni de deux entrées connectées aux bornes d'entrée (6, 7) du dispositif de filtrage et de deux sorties (11, 12) couplées aux entrées inverseuse (3) et non inverseuse (2) de l'amplificateur équilibré (1), caractérisé en ce que le circuit de conductance de trans-



fert (10) comporte plusieurs dispositifs actifs (T_1 , T_2) qui présentent chacun une borne d'entrée de commande et des première et deuxième bornes de sortie, les bornes d'entrée de commande d'au moins deux desdits dispositifs actifs étant connectées aux entrées (6,7) du circuit de conductance de transfert (10), les premières bornes de sortie d'au moins deux dispositifs actifs (T_1 , T_2) étant interconnectées et les deuxième bornes de sortie étant couplées respectivement aux sorties (11, 12) du circuit de conductance de transfert (10).

2. Dispositif de filtrage selon la revendication 1, caractérisé en ce qu'un circuit de charge est disposé entre les sorties (11, 12) du circuit de conductance de transfert (10), lequel circuit de charge comporte deux transistors sources de courant (T_3 , T_4) dont les collecteurs sont connectés aux sorties (11, 12) du circuit de conductance de transfert (10) et dont les bases sont connectées à une entrée de commande commune qui est couplée au point de jonction de deux résistances (R_1 , R_2) disposées entre les sorties du circuit de conductance de transfert (10).

3. Dispositif de filtrage selon la revendication 1 ou 2, caractérisé en ce que le circuit de conductance de transfert (10) comporte un amplificateur différentiel muni de deux transistors (T_1 , T_2) dont les bases sont connectées aux bornes d'entrée (6, 7), dont les collecteurs sont connectés aux sorties (11, 12) du circuit de conductance de transfert (10) et dont les émetteurs sont connectés à une source de courant commune (I) dont le courant est variable.

4. Dispositif de filtrage selon la revendication 3, caractérisé en ce qu'un diviseur de tension (R_3 , R_4) est disposé entre la base des deux transistors (T_{10} , T_{11}) et son point de jonction est connecté aux bases des deux transistors (T_{12} , T_{13}) dont les émetteurs sont connectés à la source de courant commune (I_5) et dont les collecteurs sont connectés aux sorties (11, 12) du circuit de conductance de transfert.

5. Dispositif de filtrage selon la revendication 1 ou 2, caractérisé en ce que le circuit de conductance de transfert (10) comporte deux amplificateurs différentiels (T_5 , T_6 ; T_7 , T_8) munis chacun de deux, transistors qui présentent des faces d'émetteur inégales et dont les émetteurs sont connectés à une source de courant commune (I_2 , I_3) dont le courant est variable, amplificateurs dont les bases des deux transistors sont interconnectées et les

collecteurs desdits deux transistors présentant des faces d'émetteur différentes sont interconnectés à une sortie du circuit de conductance de transfert (10).

6. Dispositif de filtrage selon la revendication 1 ou 2, caractérisé en ce que le circuit de conductance de transfert (10) comporte un premier amplificateur différentiel muni de deux transistors à effet de champ (T_5 , T_6) dont les électrodes de source sont connectées à une première source de courant commune (I_2) et dont les électrodes de drain sont connectées aux sorties (11, 12) du circuit de conductance de transfert, et d'un deuxième amplificateur différentiel monté en parallèle avec ledit premier amplificateur différentiel et muni de deux transistors à effet de champ (T_7 , T_8), dont les électrodes de source sont connectées à une deuxième source de courant commune (I_3) et dont les électrodes de drain sont couplées en croix aux électrodes de drain des transistors à effet de champ du premier amplificateur différentiel.

7. Dispositif de filtrage selon la revendication 1, 2, 3, 4, 5 ou 6, caractérisé en ce que l'amplificateur équilibré comporte deux transistors (T_{21} , T_{22}) montés en paire différentielle, dont les bases sont couplées à l'entrée non inverseuse (2) et à l'entrée inverseuse (3) et dont les collecteurs sont connectés à la sortie inverseuse (4) et la sortie non inverseuse (5) de l'amplificateur, sorties entre lesquelles est disposé un circuit de charge comportant deux transistors sources de courant (T_{27} , T_{28}) dont les collecteurs sont connectés à la sortie inverseuse (4) et la sortie non inverseuse (5) de l'amplificateur et dont les bases sont connectées à une entrée de commande commune qui est couplée au point de jonction entre deux résistances de charge (R_6 , R_7) disposées entre les sorties (4, 5) de l'amplificateur.

8. Dispositif de filtrage selon la revendication 7, caractérisé en ce que le dispositif de filtrage est couplé à un deuxième dispositif de filtrage, les bornes d'entrée (6, 7) du deuxième dispositif de filtrage étant connectées aux prises prévues sur les résistances de charge du circuit de charge de l'amplificateur du premier dispositif de filtrage.

Patentansprüche

1. Filteranordnung, die einen Gegentaktverstärker (1) mit einem invertierenden Eingang (3), einem nichtinvertierenden Eingang (2), einem in-



- vertierenden Ausgang (4) und einem nichtinvertierenden Ausgang (5), eine erste Eingangsklemme (6) und eine zweite Eingangsklemme (7), eine erste Rückkoppelschaltung mit einem ersten Kondensator (C_2), der zwischen dem nichtinvertierenden Ausgang (5) und dem invertierenden Eingang (3) angeordnet ist, eine zweite Rückkoppelschaltung mit einem zweiten Kondensator (C_1), der im wesentlichen gleich dem ersten Kondensator (C_2) ist und zwischen dem invertierenden Ausgang (4) und dem nichtinvertierenden Eingang (2) angeordnet ist, eine Durchgangsleitwertschaltung (10) mit änderbarem Durchgangsleitwert mit zwei Eingängen, die an die Eingangsklemmen (6,7) der Filteranordnung angeschlossen sind, und mit zwei Ausgängen (11, 12), die mit den invertierenden (3) und den nichtinvertierenden (2) Eingängen des Gegentaktverstärkers (1) gekoppelt sind, dadurch gekennzeichnet, daß die Durchgangsleitwertschaltung (10) eine Anzahl aktiver Einrichtungen (T_1, T_2) mit einer Steuereingangsklemme und ersten und zweiten Ausgangsklemmen enthält, wobei die Steuereingangsklemmen von wenigstens zwei der aktiven Einrichtungen mit den Eingängen (6, 7) der Durchgangsleitwertschaltung (10) verbunden sind, die ersten Ausgangsklemmen der wenigstens zwei aktiven Einrichtungen (T_1, T_2) zusammengeschaltet und die zweiten Ausgangsklemmen mit den betreffenden Ausgängen (11, 12) der Durchgangsleitwertschaltung (10) gekoppelt sind.
2. Filteranordnung nach Anspruch 1, dadurch gekennzeichnet, daß zwischen den Ausgängen (11, 12) der Durchgangsleitwertschaltung (10) ein Verbraucherkreis angeordnet ist, der zwei Stromquellentransistoren (T_3, T_4) umfaßt, deren Kollektoren an die Ausgänge (11, 12) der Durchgangsleitwertschaltung (10) liegen und deren Basen an einen gemeinsamen Steuereingang angeschlossen sind, der mit dem Knotenpunkt von zwei Widerständen (R_1, R_2) zwischen den Ausgängen der Durchgangsleitwertschaltung gekoppelt ist.
3. Filteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Durchgangsleitwertschaltung (10) einen Differenzverstärker mit zwei Transistoren (T_1, T_2) enthält, deren Basen mit den Eingangsklemmen (6, 7) verbunden sind, deren Kollektoren mit den Ausgängen (11, 12) der Durchgangsleitwertschaltung (10) und deren Emitter mit einer gemeinsamen Stromquelle (I_1) verbunden sind, deren Strom einstellbar ist.
4. Filteranordnung nach Anspruch 3, dadurch gekennzeichnet, daß ein Spannungsteiler (R_3, R_4) zwischen den Basen der zwei Transistoren (T_{10}, T_{11}) angeordnet und mit seinem Knotenpunkt an die Basen von zwei Transistoren (T_{12}, T_{13}) angeschlossen ist, deren Emitter mit der gemeinsamen Stromquelle (I_5) und deren Kollektoren mit den Ausgängen (11, 12) der Durchgangsleitwertschaltung verbunden sind.
5. Filteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Durchgangsleitwertschaltung (10) zwei Differenzverstärker ($T_5, T_6; T_7, T_8$) mit je zwei Transistoren enthält, die ungleiche Emittergebiete besitzen und deren Emitter mit einer gemeinsamen Stromquelle ($I_2; I_3$) verbunden sind, deren Strom variabel ist, wobei die Basen der zwei Differenzverstärker miteinander und die Kollektoren von zwei Transistoren mit verschiedenen Emittergebieten miteinander und mit einem Ausgang (11, 12) der Durchgangsleitwertschaltung verbunden sind.
6. Filteranordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Durchgangsleitwertschaltung (10) einen ersten Differenzverstärker mit zwei Feldeffekttransistoren (T_5, T_6) enthält, deren Quellenelektroden an eine erste gemeinsame Stromquelle (I_2) und deren Abzugselektroden an die Ausgänge (11, 12) der Durchgangsleitwertschaltung angeschlossen sind, und ein zweiter Differenzverstärker parallel zum ersten Differenzverstärker angeordnet ist und zwei Feldeffekttransistoren (T_7, T_8) besitzt, deren Quellenelektroden an eine zweite gemeinsame Stromquelle (I_3) angeschlossen sind und deren Abzugselektroden kreuzweise mit den Abzugselektroden der Feldeffekttransistoren des ersten Differenzverstärkers verbunden sind.
7. Filteranordnung nach Anspruch 1, 2, 3, 4, 5 oder 6, dadurch gekennzeichnet, daß der Gegentaktverstärker zwei als Differenzpaar geschaltete Transistoren (T_{21}, T_{22}) enthält, deren Basen mit dem nichtinvertierenden Eingang (2) und dem invertierenden Eingang (3) verbunden sind und deren Kollektoren mit dem invertierenden Ausgang (4) und dem nichtinvertierenden Ausgang (5) des Verstärkers verbunden sind, und zwischen diesen zwei Ausgängen ein Verbraucherkreis mit zwei Stromquellentransistoren (T_{27}, T_{28}) angeordnet ist, deren Kollektoren mit dem invertierenden Ausgang (4) und dem nichtinvertierenden Ausgang (5) des Verstärkers und deren Basen mit einem gemein-



samen Steuereingang verbunden sind, der mit dem Knotenpunkt zwischen zwei Belastungswiderständen (R_6 , R_7) gekoppelt ist, die zwischen den Ausgängen (4,5) des Verstärkers angeordnet sind.

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8. Filteranordnung nach Anspruch 7, dadurch gekennzeichnet, daß die Filteranordnung mit einer zweiten Filteranordnung gekoppelt ist, wobei die Eingangsklemmen (6', 7') der zweiten Filteranordnung an Anzapfungen auf den Belastungswiderständen des Verbraucherkreises des Verstärkers der ersten Filteranordnung angeschlossen sind.

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