

LIST OF REFERENCE MARKS

- 101: video camera recorder
- 102: timing signal generation circuit
- 5 103: synchronizing signal separation circuit
- 104: first gate circuit
- 105: delay circuit
- 106: second delay circuit
- 107: liquid crystal display unit
- 10 102a: A/D converter
- 102b: pattern-matching circuit
- 102c: synchronizing signal generation circuit
- 102d: memory control circuit
- 102e: FIFO memory
- 15 102f: system clock generation circuit
- 111: AND circuit
- 112: delay circuit
- 113: NOR circuit
- 114: inverter
- 20 121: latch circuit
- 122: AND gate
- 123: free-running counter
- 124: FIFO memory
- 131: field memory
- 25 132: first control circuit
- 133: second control circuit

134: control circuit
132a: horizontal-vertical synchronizing signal
separation circuit
132b: horizontal synchronizing signal count circuit
5 132c: enable signal generation circuit
132d: write clock generation circuit
133a: counter circuit
133b: read enable generation circuit
133c: control signal generation circuit for liquid
10 crystal display unit

SPECIFICATION

A Liquid Crystal Display Device

TECHNICAL FIELD

5 The present invention relates to a liquid crystal display device, such as used in a liquid crystal television. In the present invention, particularly, a character displaying method is improved in a liquid crystal viewfinder of a portable video camera recorder
10 (below, video camera) in which video signals are digitized. Further, on the steps of digitizing the video signals and of storing them into a memory, the character displaying method is improved at the steps of a special playback, such as a cue playback, a review playback, and
15 a still playback. Still further, when digitizing the video signal, pseudo vertical synchronizing signals are occurred due to noises which are mixed with a vertical synchronizing signal, and flash actions are also occurred due to change of an actual voltage caused by the pseudo
20 vertical synchronizing signals. The present invention aims to reduce the flash action so that it is possible to improve the quality of the display.

BACKGROUND ART

25 Recently, a portable and compact liquid crystal TV having a liquid crystal display has been spread in accordance with the development of the liquid crystal technique. Further, portable video cameras having liquid crystal viewfinder are widely utilized for consumer use, industrial use, etc.

30 In general, in the character display in the liquid crystal viewfinder of the liquid crystal video camera, the insertion position of the characters on the display is determined by the synchronizing signal separated from the video signal. The display of the various character
35 information is usually performed at the time of picture recording in which the timing of the synchronizing signal is determined.

The reason that the character display is only performed at the time of the picture recording is that since the synchronizing signals are disturbed by noises, the insertion of the character becomes difficult at the special playback, such as the cue playback, the review playback, the still playback, and the playback including much noises, except for the picture recording and a normal playback.

On the other hand, in a recent technique, in a type of the video camera using digitalized video signals, such as the portable video camera having the liquid crystal viewfinder, the various character information, such as a time indication and a tape running indication can be displayed on the viewfinder by synchronizing the character display with the timing signal of the liquid display.

However, in the method of synchronizing the character display with the timing signal of the liquid display, since the video signal is separated synchronously by using a reference clock of a control circuit of the liquid crystal display device and the video signal obtained is digitized, an error occurs during one clock interval at the maximum. Accordingly, when the video signal having character information, such as time indication, is recorded by using the digitized timing signal, a phase shift, i.e., a jitter occurs during one clock interval at the maximum.

Further, conventionally, in the liquid crystal viewfinder of the video camera, a shift of generation time of the synchronizing signal, which occurs just after the noise occurs at the switching time of a rotating head in the special playback, is processed as a reset signal regardless of an amount of shift so that the operation for a horizontal direction is restarted. That is, in the liquid crystal viewfinder of the portable video camera using a so-called first-in first-out memory (i.e., FIFO memory), a shift of generation time of the synchronizing

signal, which occurs just after the noise occurs at the switching time of a rotating head in the special playback, is processed as the reset signal regardless of an amount of shift so that the reset operation is
5 executed before completion of a write operation for one horizontal line to the FIFO memory.

In the above method, the device operates just as a position which the reset operation is performed is just left end of the normal image, all data after this
10 position are shifted to the horizontal direction so that the positions of the image which noises are mixed are also shifted horizontally. In the above state, for example, the noises are mixed in twice on the display and twice shifts also occurs on the image corresponding to
15 the noises. In order to solve this problem, the display is performed in such a manner that the first horizontal synchronizing signal in which the position is shifted is ignored and the character information is synchronized with the next synchronizing signal.

Further, when displaying the characters on the liquid crystal viewfinder by using the above type which ignores the horizontal synchronizing signal, the problem occurs that the positions of the character are shifted to the vertical position in correspondence to the number of
20 horizontal synchronizing signals ignored. As explained below, the displayed image becomes the shorten image for the vertical direction since the horizontal synchronizing signal is ignored. That is, the following problems occur that the position of the characters which are actually
25 displayed is shifted to upward direction as to the number of horizontal synchronizing signals ignored, and there is an area which the image does not exist on the most low portion of the display.

Still further, in a conventional liquid crystal
35 viewfinder, the pseudo vertical synchronizing signal, which occurs due to an erroneous operation caused by noises at the special playback in the synchronous

separation circuit, is processed as the reset signal in a scanning electrode drive circuit. Accordingly, a scanning electrode for the new vertical direction is selected. On the other hand, there are two methods for the operation of the scanning electrode drive circuit of the liquid crystal display unit when the vertical synchronizing signal is input to a position different to previous one. That is, the first method follows the scanning electrode signal which is previously selected in the vertical direction, and generates the scanning electrode signal. The second method stops the generation of the scanning electrode signal on a way of selecting operation to the vertical direction, and starts the new selecting operation for the scanning electrode.

In the first display method, since the method follows the scanning electrode selecting signal which previously operates toward the vertical direction to occur this signal, two selecting intervals exist in the field. Further, in this case, an effective voltage is risen in comparison with a normal state which one selecting interval exists within one field, and the transmittivity of the liquid crystal is risen in the field interval in which two selecting intervals exist. Accordingly, the flash action which the image becomes bright in a moment occurs on the display.

In the second display method, since the method stops the generation of the scanning electrode signal on the way of selecting operation toward the vertical direction, and starts the selecting operation toward the vertical direction, the effective voltage of the liquid crystal display unit is fallen in the position after the generation of the scanning electrode selecting signal is stopped and the flash action which the image becomes bright in a moment occurs on the display.

DISCLOSURE OF THE INVENTION

The first object of the present invention is to provide a synchronizing method of a character display in

which the character information having no phase shift and jitter is inserted into the video signal at the normal playback, and various information can be displayed during the special playback. The second object of the present invention is to provide a display method which can prevent drop-out of the number of the scanning lines and eliminate the shift of the character display. The third object of the present invention is to provide a display method of a liquid crystal television which can eliminate the flash action of the image on the display.

A liquid crystal display device according to the present invention includes: a timing signal generation unit for receiving a video signal from the a video camera; a synchronizing separation unit for generating a synchronizing signal based on the video signal; a first gate unit for receiving a timing signal from the timing signal generation unit and the synchronizing signal, executing a logical product (AND operation) and outputting the result; a delay unit for delaying an output of the first gate unit; a second gate unit for receiving the timing signal and a delay signal from the delay unit, executing a logical sum (OR operation) and outputting the result; and a liquid crystal display unit for receiving a video data from the timing signal generation unit, and displaying the same; wherein the timing signal generation unit executes a pattern-matching process of the synchronizing signal and generates the timing signal; and the second gate unit feeds the timing signal or delay signal back to the video camera as the synchronizing signal for the character display.

As an embodiment, the timing signal generation unit includes an A/D converter for receiving the video signal and converting it to the digital value; a pattern-matching circuit for receiving synchronizing signal and executing the pattern-matching process; a synchronizing signal generation circuit for generating the timing signal in accordance with the pattern-matching process;

and a first-in first-out memory (FIFO memory) for temporarily writing the digitized video signal and reading the same in accordance with the timing signal and a system clock.

5 As another embodiment, the timing signal generation unit includes a latch circuit for temporarily latching the synchronizing signal; a free-running counter for counting a write clock of the FIFO memory, outputting an enable signal at a predetermined count value, and
10 outputting a self-reset signal to the latch circuit; an AND gate for executing the AND operation between the output of the latch circuit and the enable signal, and outputting the reset signal to the free-running counter circuit; and a first-in first-out memory for temporarily
15 storing the video signal in accordance with the read and write operation controlled by the enable signal or the reset signal.

 As still another embodiment, the timing signal generation unit includes a field memory for temporarily
20 storing the video signal; a first control circuit for receiving the synchronizing signal, and generating a first control signal to the field memory; and a second control circuit for starting in response to a
 predetermined start signal and generating the second and
25 third control signal; wherein the period for writing the video signal into the field memory in response to the first control signal is asynchronous with the period for reading the data from the field memory in response to the
 second control signal and displaying the read data on the
30 liquid crystal display unit in response to the third control signal.

 As still another embodiment, the first control circuit includes a horizontal-vertical synchronizing signal separation circuit for separating the
35 synchronizing signal into the horizontal synchronizing signal and the vertical synchronizing signal; a horizontal synchronizing signal count circuit for

counting the horizontal synchronizing signal; a write clock generation circuit for generating a write clock in accordance with the counted value of the horizontal synchronizing signal counter circuit; and an enable signal generation circuit for generating the enable signal in accordance with the counted value; wherein the outputs of the write clock generation circuit and the enable signal generation circuit are input to the field memory as the first control signal.

As still another embodiment, the second control circuit includes: a counter circuit for counting the clock from the system clock; a read enable generation circuit for outputting the second control signal to the field memory in accordance with the counted value of the counter circuit; and a control signal generation circuit for the liquid crystal display unit for outputting the third control signal to the liquid crystal display unit in accordance with the counted value.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an essential block diagram of a liquid crystal display device according to the present invention;

Fig. 2 is a signal timing chart for the picture recording and the normal playback in the structure of Fig. 1;

Fig. 3 is a signal timing chart for the special playback in the structure of Fig. 1;

Fig. 4 is a circuit diagram of a gate circuit and a delay circuit in the structure of Fig. 1;

Fig. 5 is a detailed block diagram of a timing signal generation circuit in the structure of Fig. 1;

Fig. 6 is another essential structural view of a timing signal generation circuit in the structure of Fig. 1;

Fig. 7 is an explanatory view of a display image for the special playback according to the present invention;

Fig. 8 is an explanatory view of the display image

for the normal playback;

Fig. 9 is an explanatory view of the display image of the reset operation for the special playback;

5 Fig. 10 is an explanatory view of the display image in which the drop-out portions of the scanning line are shorten in the special playback;

Fig. 11A is a timing chart for the normal operation;

10 Fig. 11B is a timing chart explaining an erroneous operation when noises are mixed for the horizontal direction;

Fig. 12 is another block diagram of the timing signal generation circuit in the structure of Fig. 1;

Fig. 13 is a detailed block diagram of the first and second control circuits in the structure of Fig. 12;

15 Fig. 14 is a block diagram of a conventional art corresponding to the structure of Fig. 12;

Fig. 15 is a timing chart explaining a flash action caused by a pseudo vertical synchronizing signal; and

20 Fig. 16 is an explanatory view of a pseudo vertical synchronizing signal.

Best Mode for Carrying out the Invention

An embodiment of the present invention will be explained with respect to the drawings below. Figure 1 is an essential block diagram of a liquid crystal display device according to the present invention. Figure 2 is a
25 signal timing chart for the picture recording and the normal playback in the structure of Fig. 1. Figure 3 is a signal timing chart for the special playback in the structure of Fig. 1. Figure 4 is a circuit diagram of a
30 gate circuit and a delay circuit in the structure of Fig. 1.

In Fig. 1, reference number 101 denotes a video camera, 102 denotes a timing signal generation circuit, 103 denotes a synchronizing separation circuit,
35 104 denotes a first gate circuit, 105 denotes a delay circuit, 106 denotes a second gate circuit, and 107 denotes a liquid crystal display unit. The video

signal VD from the video camera 101 is input to the timing signal generation circuit 102 and the synchronizing separation circuit 103, and a synchronizing signal SY is output from the synchronizing separation circuit 103. On the other hand, when the timing signal generation circuit 102 receives the synchronizing signal SY, it outputs a timing signal TM, which is based on the synchronizing signal SY as a kind of control signals which displays on the liquid crystal display unit 107, to the second gate circuit 106, for example, an OR circuit.

The timing signal TM is controlled by the timing generation circuit 102 so as to become the same period and pulse width as the timing of the synchronizing signal SY. In this case, as shown by the synchronizing signal SY and the timing signal TM of Fig. 2, the small delay caused by circuit elements occurs. A pattern-matching operation is executed in the timing signal generation circuit 102. For example, if the synchronizing signal SY is dropped out in the special playback, the timing signal TM is generated from a free-running counter provided in the timing signal generation circuit 102, and is always output in the constant interval and controlled so as to eliminate signals caused by noises which are mixed therein. To utilize the switching time of the synchronizing signal SY when the timing signal TM is output, the AND operation is performed between the synchronizing signal SY and the timing signal TM in the first gate circuit 104, for example, the AND circuit, and the output AO is input to the delay circuit 105 during the AND operation.

The delay circuit 106 delays the AND output AO so as to delay over the switching position of the timing signal TM, and outputs the delay signal DL to the second gate circuit 106. The second gate circuit 106 generates the synchronizing signal CSY for the character display in accordance with the timing signal TM and the delay signal DL, and outputs to the video camera 101. In the present

invention, character signals are generated based on the timing of a trailing edge of the synchronizing signal CSY for the character display.

5 In Fig. 2, the synchronous signal SY is the signal which is output from the synchronizing separation circuit based on the video signal VD, the timing signal TM is the signal which is output from the timing generation circuit, the AND output AO is the signal which is output from the AND circuit based on the AND operation between
10 the synchronizing signal SY and the timing signal TM, the delay signal DL is the signal which is delayed from the AND output AO, and the synchronizing signal CSY for the character display is the signal which is output based on the delay signal DL and the timing signal TM. The
15 synchronizing signal CSY for the character display is input to the video camera, and utilized as the synchronizing signal for the character display. In the drawing, the leading/trailing portions circled show the switching timing of various signals, and the arrows in
20 the drawing show that the timing of the source of the arrow generates the timing of the destination of the arrow.

In Fig. 3, each signal corresponds to the signal shown in Fig. 2. In this example, the synchronizing
25 signal SY is dropped-out as shown in the drawing. Since the timing of the synchronizing signal is not changed, the AND output AO and the delay signal DL are not shown in the drawing. The timing signal TM from the timing generation circuit is input to the OR circuit and
30 generates the synchronizing signal CSY for the character display.

In Fig. 4, the AND circuit 111 corresponds to the first gate circuit 104, and is formed of resistors and capacitors. The delay circuit 112 corresponds to the
35 delay circuit 105, and the NOR circuit 113 corresponds to the second gate circuit 106. The inverter 114 is provided for inverting the output of the NOR circuit, and

is formed of the OR circuit including the NOR circuit therein. Further, IN1 denotes an input terminal of the synchronizing signal SY, IN2 denotes an input terminal of the timing signal TM, and OU1 denotes an output terminal of the synchronizing signal for the character display. The explanation of the NOR circuit and the OR circuit is omitted because these circuit are well known.

Figure 5 is a detailed block diagram of a timing signal generation circuit in the structure of Fig. 1. As shown in the drawing, the video signal VD is converted to the digital signal by the A/D converter 102a, and the digital signal is stored in the FIFO memory 102e. On the other hand, a synchronizing signal, which is generated in the synchronizing separation circuit 103 based on the video signal, is input to the pattern-matching circuit 102b, and used as the synchronizing signal for the known pattern-matching circuit 102b. The output of the pattern matching circuit 102b is input to the synchronizing signal generation circuit 102c and generates the timing signal TM. Further, the output of the synchronizing signal generation circuit 102c is input to the memory control circuit 102d, and controls the write to the FIFO memory 102e and the read therefrom. The system clock 102f generates a clock which controls the operation of these circuits.

According to the first aspect of the present invention, it is possible to provide a synchronizing method of a character display in which character information having no phase shift and jitter can be inserted into the video signal at normal playback, and various information can be displayed during the special playback.

An embodiment of another aspect of the present invention will be explained with reference to the drawings. Figure 6 is another essential structural view of a timing signal generation circuit in the structure of Fig. 1, Figure 7 is an explanatory view of a display

image during the special playback according to the present invention, Figure 8 is an explanatory view of the display image during normal playback, Figure 9 is an explanatory view of the display image at the reset operation of the special playback, and Figure 10 is an explanatory view of the display image in which the drop-out portion of the scanning lines are shorten during the special playback.

5 In Figure 6, the synchronizing signal SY obtained from the video signal VD is input to the latch circuit 121. Once latched signal is input to the gate circuit 122. The free-running counter 123 counts the write clocks of the FIFO memory 124, and generates the self-reset signal SR at a predetermined count value. Further, the self-reset signal SR is input to the latch circuit 121. In this case, the self-reset signal SR corresponds to the timing signal TM of Figure 4.

10 When the write operation is not performed to the FIFO memory 124 which receives the video signal VD, the output of the gate circuit 122 acts as the reset signal RS of the free-running counter 123 so that the free-running counter 123 is reset, and the latch circuit 121 is also reset. YES/NO (executed/not executed) of the write operation to the FIFO memory 124 is controlled in accordance with the enable signal WE from the free-running counter 123.

20 During the write operation to the FIFO memory 124, when the synchronizing signal SY is input to the latch circuit 121, YES/NO (existence/non existence) of the input of the synchronizing signal is stored and held in the latch circuit 121. Since the gate circuit 122 is disconnected based on the enable signal WE to the FIFO memory 124, the reset signal is not input to the free-running counter 123 from the gate circuit 122.

30 Accordingly, since the output of the enable signal WE from the free-running counter 123 to the FIFO memory 124 continues, the FIFO memory 124 also continues the write

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operation of the video signal.

When the write operation to the FIFO memory 124 is completed, the gate circuit 122 is connected by the enable signal WE. When the synchronizing signal SY which is held in the latch circuit 121 is input to the gate circuit 122, the gate circuit 122 sends the reset signal RS to the free-running counter 123. The free-running counter 123 is reset by the reset signal. Accordingly, all above processes can be continued in the state that the synchronous signal is not ignored.

On the other hand, in the read operation from the FIFO memory 124, the data corresponding to the number of pixels within one horizontal period are read from the FIFO memory 124 regardless of YES/NO of the pseudo synchronizing signals caused by the noises and occurred in an optional timing within one horizontal period. The data are displayed on the liquid crystal display unit. In this case, the arrangement of the data in the FIFO memory 124 corresponds to the arrangement of the data which is displayed on the liquid crystal display unit.

Based on the above control, the image, which is provided just after noises occur in the special playback, is shifted in accordance with an amount of the shift at the position where the horizontal synchronizing signal exists. However, this shift is gradually revised and returned to the original position. At that time, since the horizontal synchronizing signal is not omitted, the shift is not occurred for the vertical direction as shown in Fig. 7. Further, since the write operation is not interrupted in the FIFO memory 124, the shift is not continued for the horizontal direction so that it is possible to obtain the normal position of the character display without the display which is shorten to the vertical direction as shown in Fig. 10.

Further, in Fig. 9, the shift is shown in the liquid crystal viewfinder of the video camera using the FIFO memory. In this case, the reset operation is started

from the shifted position of the synchronizing signal just after noises occur in the switch timing of the rotating head at the special playback, such as the cue playback, the review playback, and the still playback.

5 The explanation will be given with respect to Fig. 10 as follows. The horizontal synchronizing signal in which the generating position is shifted, is ignored in a state just after the noise occurs in the switch timing of the rotating head at the special playback.
10 Accordingly, the display is performed by synchronizing with the next synchronous signal. Figure 11A shows a timing chart at the normal operation, and Figure 11B shows a timing chart explaining an erroneous operation when noises are mixed in the horizontal direction. This
15 timing chart indicates the relationship of the signal timing among the video signal VD input to the synchronizing separation circuit 103 of Fig. 1, the synchronizing signal SY occurring from the synchronizing separation circuit 103 based on the video signal VD, and
20 the enable signal WE (see, Fig. 6) performing a control to store the video signal VD into the FIFO memory 124.

 In the drawing, the video signal VD is the video signal at the normal operation, and the synchronizing signal SY is generated based on the video signal. As
25 shown in Fig. 1, the synchronizing signal SY is input to the timing signal generation circuit 102 so that the control signal CS1 is generated as the enable signal of the field memory 131.

 Further, Figure 11B shows the disturbance of the
30 synchronizing signal SY when noises are mixed during the special replay. The waveform of the video signal VD at the special playback is entirely different from the playback which contains noises. However, since the synchronizing signal, the enable signal and the
35 occurrence of the erroneous operation are given by the same explanations as above, only noises which are mixed in the signal are shown in this drawings. When the

noises are mixed, the synchronizing signal SY exists and the pseudo synchronizing signal PSY is generated as shown by the circles in Fig. 11B. In noises at the special playback, the synchronizing signal does not exist, and only the pseudo synchronizing signal PSY is generated. In both abnormal cases, the interval between the synchronizing signals is not constant as shown in the drawing.

To simplify the explanation, the video signal VD is formed of nine data. Further, the synchronizing signal is shown by "S", the pseudo synchronizing signal is shown by "P", the portion in which the data does not exist is expressed by "0", continuous signals are shown by ten numerals "0" to "9". The video signal VD at the normal operation can be expressed by "S0123456789, S0123456789,". Since the portions "0" in which the data does not exist are erased by the enable signal, the video signals VD are stored to the memory in the form of "123456789, 123456789, ...". These data trains are displayed on the liquid crystal unit which is formed of nine elements as follows.

123456789

123456789

:

:

It is assumed that one pulse of the noise is input to the device. The video signal VD becomes "S0123456789, S1234P6789, S0123456789, ...". As mentioned above, since the synchronizing signal S and the portion "0" in which the data does not exist are erased, the data train "123456789, 1234-6789, 123456789 ..." are stored in the memory. Similarly, this data train having nine data are displayed on the liquid crystal display unit as follows.

123456789

234578912

345678912

345678912

345678912

345678912

As is obvious from above, the data "1" which should be displayed on the left side, is shifted to the right side due to the noise which is mixed.

According to the present invention, if the pseudo synchronizing signals are mixed, the sampling operation on the memory is performed to the horizontal direction until nine data are completed. Accordingly, the shift of the data does not occur in the present invention. When the video tape is extended or the channel is changed, the normal synchronizing signal is shifted so that it is necessary to hold the record of the synchronizing signal in the sampling signals.

It is assumed that the video signals are shown by the train of "S0123456789, S0123P0000, S0123456789, S012345678, ...".

In the conventional art, the data train "123456789, 1230000, 123456789, 123456789, 123456789" are stored in the memory, and displayed as follows.

123456789

123000012

345678912

345678912

345678912

345678912

In the present invention, the data train "123456789, 123P00P00, S0123456789, S0123456789, S0123456789, ..." are stored in the memory, and displayed as follows.

123456789

123P00P00

0S0123456

789S01234

56789S012

3456789S0

123456789

123456789

123456789

As is obvious from above data train, the data train soon recovers after the noises are mixed therein.

5 Although the actual liquid crystal has 640 pixels in the horizontal direction, the explanation is omitted because the same explanation would be given for this large number of pixels.

10 As explained above, according to the second aspect of the present invention, it is possible to realize a liquid crystal viewfinder which can prevent the drop-out of the scanning lines and eliminate the shift of the position of the character display.

15 The third aspect of the present invention will be explained with respect to the drawings. Figure 12 is a block diagram according to an embodiment of the third aspect of the present invention. In Fig. 12, 131 denotes a field memory which corresponds to the FIFO memory. Further, the first control circuit 132 and the second control circuit 133 are included in the timing generation circuit explained above. The video signal VD is input to the field memory 131 in accordance with the control signal CS1 which is output from the first control circuit 132 controlled by the synchronizing signal SY. On the other hand, the second control circuit 133, for example, is started in response to the power-ON and driven asynchronously with the first control circuit 132. Further, the second control circuit 133 outputs the control signal CS2 to the field memory 131, and reads the content of the field memory in accordance with the read period regardless of the write period. The video data VDA is sent from the field memory 131 to the liquid crystal display unit 107. In this case, the video data VDA is synchronized with the control signal CS3 from the second control circuit 133.

35 Figure 13 is a detailed block diagram of the first and second control circuits shown in Fig. 12. In the first control circuit 132, the synchronizing signal SY is input to the horizontal-vertical synchronizing signal

separation circuit 132a, and the horizontal-vertical
synchronizing signal separation circuit 132a outputs the
horizontal synchronizing signal HSY and the vertical
synchronizing signal VSY to the horizontal synchronizing
signal count circuit 132b. One output of the horizontal
5 synchronizing signal count circuit 132b is sent to the
enable signal generation circuit 132c, the other output
is sent to the write clock generation circuit 132d. Both
outputs of the enable signal generation circuit 132c and
10 the write clock generation circuit 132d are sent to the
field memory 131 as the control signal CS1 in response to
the clock SC from the system clock 102f. The field
memory 131 receives the video signal VD.

Further, in the second control circuit 133, the
15 system clock SC is input to the counter circuit 133a.
The counted value of the counter circuit 133a is input to
the read enable generation circuit 133b, and further
input to the field memory 131 with the output of the read
enable generation circuit 133b as the control signal CS2.
20 Further, the counted value of the counter circuit 133a is
input to the control signal generation circuit 133c of
the liquid crystal display unit, and the output of the
control signal generation circuit 133c is input to the
liquid crystal display unit 107 as the control
25 signal CS3. Further, the read data DA from the field
memory 131 is input to the liquid crystal display
unit 107 in response to the control signal CS3.

Figure 14 is a block diagram of a conventional art
corresponding to Fig. 12. As shown in Figs. 12 and 14,
30 the video signal VD is input to the field memory 131 in
response to the control signal CS4 which is output from
control circuit 134 controlled by the synchronizing
signal SY, and is read in response to the read period
having a period which synchronizes with the write period
35 of the field memory 131. Further, the video signal is
sent to the liquid crystal display unit 107 which is
controlled by the control signal CS5 from the control

circuit 134. The control signal CS5 is synchronized with the synchronizing signal and the video data VDA which is read from the field memory 131.

5 In the above structure, in accordance with the video signal having noises and the noise which is occurred in the switch timing of the rotating head at the special playback of the video tape recorder, the synchronizing separation circuit 103 operates in error so that pseudo vertical synchronizing signal PSY is generated just as
10 the vertical synchronizing signal is input. As explained below, when the pseudo vertical synchronizing signal PSY is input to the control circuit 134 as the synchronizing signal SY, the reset signal RS of the scanning electrode drive circuit (not shown) is generated from the control
15 circuit 134 to the field memory 131. The write address of the field memory 131 is reset by the reset signal RS, and the write operation is started from the initial portion of the field memory. Since the display timing of the liquid crystal display unit 107 is synchronized with
20 the synchronizing signal SY, the display timing is reset in response to the input of the pseudo synchronizing signal PSY.

In actuality, since the display timing of the liquid crystal is synchronized with the timing of the
25 synchronizing signal SY, this synchronization is effective for the case of the vertical synchronizing signal which is input to the different position from the previous position, and for the case of the display of the video signal having the fluctuation of the field period
30 which occurs in the special playback of a video tape recorder.

On the other hand, in the circuit of the present invention shown in Fig. 12, the synchronizing separation circuit operates in error in response to the noise which
35 occurs in the switch timing of the rotating head at the special playback. Accordingly, the pseudo vertical synchronizing signal is generated just as the vertical

synchronizing signal is input.

When the pseudo vertical synchronizing signal is input to the first control circuit as the synchronizing signal SY, the reset signal of the scanning electrode drive circuit (not shown) is generated by the first control circuit, the write address of the field memory 131 is reset, and the write operation is started from the initial portion of the memory.

However, since the control signal CS2 for the read timing from the field memory is generated from the second control circuit 133 asynchronous with the control signal CS1 from the first control circuit 132, the display period of the liquid crystal display unit always becomes constant regardless of the write period of the field memory so that an effective voltage is not changed.

In this case, since the repetition period of the display in the liquid crystal display unit is the same period as that of the field memory, this repetition period is not synchronized with the video signal. Accordingly, the repetition period of the display in the liquid crystal display unit can be set to optional times.

In the documents JPA-1-233978 and JPA-3-84502, the inventor of the present invention discloses a liquid crystal display element having a liquid crystal which has a twist angle larger than 90 degrees (i.e., super twist nematic liquid crystal) between a pair of printed boards having the scanning electrode and the signal electrode in the opposite side. Further, it discloses a liquid crystal display device which utilizes the fact that the contrast becomes maximum in the case of twice repetition period in the display unit, in the display method of the liquid crystal television having the drive circuit for driving the display elements.

The present invention employs the period having twice and half based on the above principle. Further, in the case of the liquid crystal display unit which does not necessitate the display period larger than the period

of the video signal, the liquid crystal may be driven by the same operation as the field period of the video signal. In this case, the magnification of the period is not defined.

5 Figure 15 is a timing chart for explaining the flash action caused by the pseudo vertical synchronizing signal. The present drawing shows the cause of the flash action due to the pseudo synchronizing signals which occur due to the special playback and noises which are
10 mixed therein. In the drawing, the vertical synchronizing signal VSY shows the signal at the normal operation, and the pseudo vertical synchronizing signal PSY shows the output of the scanning electrode S1, S2, S3, ... when the signal PSY is mixed during the
15 interval T5. In the interval T5, the start signal is input to the scanning electrode drive circuit in response to the pseudo synchronizing signal PSY, and selection pulses are output to the scanning electrode in response to the number of the pseudo synchronizing signal PSY in
20 the interval T5. Accordingly, the effective voltage applied to the liquid crystal becomes higher in the interval of T5 compared with another period so that it is possible to operate the liquid crystal. This becomes the cause of the flash action.

25 Figure 16 is an explanatory view of the pseudo vertical synchronizing signal. When the pseudo synchronizing signal PSY is generated by the noise in the vertical synchronizing signal, a part of the video signal VD is dropped-out due to noises as shown by the dotted
30 circle. In the synchronizing separation circuit 103 which inputs the video signal VD, when the signal is matched to the conditions of the vertical synchronizing signal VSY, the signal is recognized as the vertical synchronizing signal so that the vertical synchronizing
35 pulse is generated.

As explained above, it is possible to prevent the pseudo synchronizing signal which occurs due to the

erroneous operation of the synchronizing separation circuit caused by noises, and the change of the effective voltage at the reset of the scanning electrode drive circuit which is caused by the pseudo vertical
5 synchronizing signal which occurs due to the erroneous operation of the synchronizing separation circuit at the special playback of the video tape recorder, and to prevent the flash action caused by the change of the effective voltage.

10 [Capability of Utilization in Industry]

In the liquid crystal display device, such as used in a liquid crystal television, the present invention improves the method of character display in the liquid crystal viewfinder of the portable camera in which the
15 video signal is digitized. Further, in the processes digitizing the video signal and storing them into the memory, the present invention improves the method of the character display at the special playback, such as the cue playback and the review playback. Still further, the
20 present invention can reduce the flash action which occurs due to the change of the effective voltage caused by the pseudo vertical synchronizing signal caused by the noises which are mixed in the vertical synchronizing signal when the video signal is digitized. Accordingly,
25 it is possible to improve the quality of the character display. Accordingly, the present invention can be widely utilized in the various industry.



CLAIMS

1. A liquid crystal display device comprising:

5 timing signal generation means for receiving a video signal and providing a video data output in response thereto;

synchronising separation means for generating a synchronising signal based on the video signal;

10 said timing signal generation means being arranged to execute a pattern matching process in respect of the synchronising signal, and to generate a timing signal in response to said matching process;

15 first logic gate means for receiving said timing signal and said synchronising signal, and outputting the logical product thereof;

delay means for providing a delayed output of the first logic gate means;

20 second logic gate means for receiving said timing signal and said delayed output, and outputting the logical sum thereof; and

a liquid crystal display unit for receiving said video data and displaying the same.

25 2. A liquid crystal display device according to claim 1, wherein the timing signal generation means comprises:

an A/D converter for receiving an analogue video signal and converting it to digital form;

30 a pattern matching circuit for receiving the synchronising signal and executing said pattern matching process;

a synchronising signal generation circuit for generating said timing signal in accordance with the pattern matching process;



and a first-in first-out (FIFO) memory for temporarily writing the digitised video signal and reading the same in accordance with the timing signal and a system clock, to provide said video data signal.

5

3. A liquid crystal display device according to claim 1 wherein the timing signal generation means comprises:

a latch circuit for temporarily latching the synchronising signal;

10

a free-running counter for counting a write clock of a FIFO memory, outputting an enable signal at a predetermined count value, and outputting a self-reset signal to the latch circuit;

15

an AND gate for executing the AND operation between the output of the latch circuit and the enable signal, and outputting the reset signal to the free-running counter circuit;

20

said first-in first-out memory being arranged for temporarily storing the video signal and reading it out as the video data signal in accordance with write and read operations controlled by the enable signal or the reset signal.

25

4. A liquid crystal display device according to claim 1, wherein the timing signal generation means comprises:

a field memory for temporarily storing the video signal and reading it out as said video data signal;

30

a first control circuit for receiving the synchronising signal, and generating a first control signal to the field memory; and

a second control circuit for starting in response to a predetermined start signal and generating second and third control signals;

35

and is arranged such that the period for writing the video signal into the field memory in response to the first



control signal is asynchronous with the period for reading the data from the field memory in response to the second control signal and displaying the read data on the liquid crystal display unit in response to the third control signal.

5. A liquid crystal display device according to claim 4, wherein the first control circuit comprises:

a horizontal-vertical synchronizing signal separating circuit for separating the synchronizing signal into a horizontal synchronizing signal and a vertical synchronizing signal;

a horizontal synchronizing signal count circuit for counting the horizontal synchronizing signal;

a write clock generation circuit for generating a write clock in accordance with the counted value of the horizontal signal count circuit; and

an enable signal generation circuit for generating an enable signal in accordance with the counted value;

wherein outputs of the write clock generation circuit and the enable signal generation circuit are input to the field memory as said first control signal.

6. A liquid crystal display device according to claim 4 or claim 5, wherein the second control circuit comprises:

a counter circuit for counting the clock from a system clock;

a read enable generation circuit for outputting the second control signal to the field memory in accordance with the counter value of the counter circuit; and

a control signal generation circuit for the liquid crystal display unit for outputting the third control signal to the liquid crystal display unit in accordance with the counted value.



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7. The combination of a video camera together with a liquid crystal display device as claimed in any preceding claim, wherein said video signal is provided by the camera, and the said logical sum is fed back to the video camera for use as a synchronous signal in providing a display of a character on the liquid crystal display.

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