

Description

The invention relates to a digital-to-analog converter for converting a one-bit coded signal into an analog signal, comprising an integrator for integrating current pulses of a first polarity when the coded signal has a first value and for integrating current pulses of a second polarity when the coded signal has a second value, which integrator comprises an operational amplifier having an inverting input, a non-inverting input which is coupled to a first terminal for a first reference voltage, and an output which is coupled to the inverting input at least by means of a first capacitor and a resistor, the converter further comprises at least a first switching network for generating the current pulses, which network is coupled to the inverting input of the amplifier and comprises a second capacitor.

Such a digital-to-analog converter is described in the article "Dual tone and modern frequency generator with on-chip filters and voltage reference" in "IEEE Journal of Solid-State Circuits", Vol. SC-19, No. 3, June 1984, pp. 379-388. The known converter comprises an integrator which integrates positive or negative current pulses depending on the value "1" or "0" of the 1-bit coded signal. The integrator thereto comprises an operational amplifier, whose output is connected to the inverting input by a first capacitor and a resistor and whose voltage at the output constitutes the analog output voltage. The current pulses are alternatively generated by means of a switched second capacitor. A positive current pulse can be produced by first discharging this capacitor and subsequently charging it by connecting one pole of the capacitor to a reference voltage and the other pole to the inverting input of the amplifier. A negative current pulse can be generated by first charging the capacitor by connecting one pole of the capacitor to the reference voltage and connecting the other pole to earth and subsequently discharging the capacitor by connecting said one pole to earth and the other pole to the inverting input of the amplifier.

However, a digital-to-analog converter employing this circuit arrangement presents the following problem. When the second capacitor is charged to generate a positive current pulse a comparatively large voltage transient is produced on the inverting input of the amplifier because the first capacitor and the second capacitor act as a voltage divider for the reference voltage. Moreover, the charging current of the capacitors, which has a comparatively high initial value, produces another voltage transient across the output resistance of the amplifier, which transient also appears on the inverting input and adds to the first-mentioned transient. As a result of the limited bandwidth of the amplifier the output of the amplifier cannot follow this voltage transient on the input. Therefore, despite the negative feedback the input signal of the amplifier may become so large that the input stage is overdriven. Consequently, the relationship between

the input voltage and the output voltage of the amplifier is no longer linear, which gives rise to distortion. This distortion causes intermodulation of the various frequency components of the analog output signal. A similar problem occurs for negative current pulse.

Therefore, it is the object of the invention to provide a digital-to-analog converter which has been equipped with at least one switched capacitance for generating the current pulses without causing distortion of the analog output signal.

A digital-to-analog converter of the type specified in the opening paragraph is characterized in that, a third capacitor is arranged between the inverting input of the amplifier and the first terminal, which third capacitor has a capacitance which is higher than that of the first capacitor and higher than that of the second capacitor. In the digital-to-analog converter in accordance with the invention the third capacitor enables distortion of the output signal to be reduced. The input of the amplifier constitutes a low-pass filter whose properties are mainly determined by the resistor, the third capacitor and the first capacitor. As a result of the Miller effect the effective capacitance of the first capacitor is seen at the input of the amplifier is higher by a factor equal to the gain of the amplifier than its real capacitance. The gain of the amplifier is high for low frequencies, so that the effective capacitance of the first capacitor (the so-called Miller capacitance) is higher than the capacitance of the third capacitor. The cut-off frequency of the filter is then dictated by the first capacitor and the third capacitor hardly does not influence the transfer characteristic of the filter. The gain of the amplifier is reduced for high frequencies so that the Miller capacitance is lower than the capacitance of the third capacitor. The cut-off frequency of the filter is then dictated by the third capacitor. This cut-off frequency is selected in such a way that high-frequency signals are attenuated. As a result of this, the voltage transients appearing on the inverting input of the amplifier are attenuated. For relatively low input voltages the relationship between the input voltage and the output voltage of the amplifier is linear, so that a very low distortion occurs.

In principle, the current pulses of the first polarity and those of the second polarity can be generated by means of one switching network. However, preferably these current pulses are generated by separate switching networks. The digital-to-analog converter may then be characterized in that the converter comprises a second switching network which is coupled to the inverting input of the amplifier and which comprises a fourth capacitor and in that the first switching network serves for generating current pulses of the first polarity and the second switching network serves for generating current pulses of the second polarity. If this is the case the first and the second switching network may be characterized further in that the switching network comprises a first switch and a second switch, for connecting

one pole of the second capacitor to the first terminal and to a second terminal for a second reference potential respectively, and a third switch and a fourth switch for connecting the other pole of the second capacitor to the first terminal and to the inverting input of the amplifier respectively, and in that the second switching network comprises a fifth switch and a sixth switch, for connecting one pole of the fourth capacitor to the first terminal and to the second terminal respectively, and a seventh switch and an eighth switch, for connecting the other pole of the fourth capacitor to the first terminal and to the inverting input of the amplifier respectively. The switches of the first switching network and the second switching network can be controlled in different ways to generate positive current pulses and negative current pulses. A suitable embodiment of the invention may be characterized in that the converter comprises clock means for closing the first switch, the third switch, the sixth switch and the seventh switch during a first clock period and for closing the second switch and the fifth switch during a second clock period and in that the converter comprises control means controlled by the one-bit coded signal for closing the fourth switch during the second clock period when the coded signal has the first value and for closing the eighth switch during the second clock period when the coded signal has the second value.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which

Fig. 1 shows a digital-to-analog converter in accordance with a first embodiment,

Fig. 2 shows the variation of the voltages on different points in the arrangement of Fig. 1 to explain the operation of the arrangement shown in Fig. 1, and

Fig. 3 shows a digital-to-analog converter in accordance with a second embodiment.

Fig. 1 shows a digital-to-analog converter in accordance with a first embodiment of the invention. The converter comprises an operational amplifier 1 having a non-inverting input which is connected to a point of fixed potential, in the present case earth, an inverting input 3, and an output 4. This output 4 is connected to the inverting input 3 by a capacitor C_1 . The amplifier 1 with the capacitor C_1 constitutes an integrator. A resistor R_1 is arranged in parallel with the capacitor C_1 to provide the d.c. feedback. It is to be noted that the resistor R_1 may be alternatively be a switched capacitance. Further, the inverting input 3 is connected to earth by a capacitor C_2 . Positive current pulses generated by a first switching network 10 and negative current pulses generated by a second switching network 20 can be applied to the inverting input 3. The switching network 10 comprises a capacitor C_3 , whose pole A can be connected to a reference voltage V_{ref} by means of a switch S_2 and to earth by means of a switch S_1 and whose other pole B can be connected to the inverting input 3 by means of a switch S_4 and to earth by means of switch S_3 . The

switching network 20 comprising a capacitor C_4 with poles C and D and comprising switches S_5 to S_8 may be of the same type as the switching network 10. The switches S_1 to S_8 may be transistors of any known type and may comprise, for example, p-channel field-effect transistors.

The switches S_1 , S_2 , S_3 , S_5 , S_6 and S_7 are controlled by clock means 30, shown schematically. The switches S_2 and S_5 are controlled by the clock signal CK, in such a way that if the clock signal CK is high the switches are in position 1 (closed) and if the clock signal CK is low these switches are in position 2 (open). The switches S_1 , S_3 , S_6 and S_7 are controlled by the clock signal $\overline{CK}$, in such a way that if the clock signal CK is high the switches are in position 2 (open) and if the clock signal CK is low they are in position 1 (closed).

The switches S_4 , S_8 , S_3 and S_7 are controlled by the 1-bit coded input signal I via control means, shown schematically. For one bit value, for example a logic 1, the switch S_4 is set to position 1 (closed) in the period in which the clock signal CK is high and to position 2 (open) in the period in which the clock signal CK is low, whilst the switch S_8 is constantly in position 2 (open). For the other bit value, a logic 0, the switch S_8 is set to position 1 (closed) in the periods in which the clock signal CK is high and to position 2 (open) in the periods in which the clock signal CK is low, whilst the switch S_4 is constantly in position 2 (open). The same signal as is applied to the switch S_4 is applied to the switch S_7 , and the same signal as is applied to the switch S_8 is applied to the switch S_3 .

The operation of the circuit arrangement will be described with reference to Fig. 2, which shows the digital input signal I comprising, in this order, two bits of the value "1" and two bits of the value "0", the clock signal CK, the control signals for the switches S_1 to S_8 , the voltage V_A on point A, the voltage V_B on point B, the voltage V_C on point C, the voltage V_D on point D, the voltage V_3 on the input 3, and the voltage V_4 on the output 4 of the amplifier 1.

In the interval $0-t_2$ the voltage of the input bit I is comparatively high, which corresponds to a logic 1 in the present example. During this interval the switch S_8 is open, so that the second switching network 20 is disconnected from the inverting input 3 of the amplifier 1. In the clock period $0-t_1$, in which the clock signal CK is high, the switches S_2 and S_4 are closed. When the switch S_2 is closed, point A is connected to the reference voltage V_{ref} , so that a positive voltage transient of a magnitude substantially equal to V_{ref} appears on this point. As the capacitor C_2 has a low impedance relative to the capacitors C_1 and C_3 , the resulting voltage division ensures that the voltage transient appearing on point B and hence on the inverting input 3 is reduced substantially. This results in a negative voltage transient on the output 4, which transient has a linear relationship with the voltage transient on the input 3, so that no distortion is introduced. The voltage transient on the output 4 gives rise to a current pulse, so that the capacitors C_1 and C_3 are charged and the

voltage on the inverting input 3, which is virtually earthed, is pulled back to zero volts. In the clock period t_1 - t_2 , in which the clock signal CK is low, the switches S_2 and S_4 are open and the switches S_1 and S_3 are closed. As a result of this, the capacitor C_3 is discharged completely, so that it can be recharged in the next clock period. In this way a positive current pulse is applied to the amplifier 1.

In the clock period 0 - t_1 , the switches S_6 and S_7 in the second switching network 20 are closed, so that the capacitor C_4 is discharged fully. In the clock period t_1 - t_2 the switches S_6 and S_7 are closed, so that the capacitor C_4 is charged to the reference voltage V_{ref} . In the interval t_2 - t_4 a logic 1 is again applied to the control means 40, so that again a positive current pulse is applied to the amplifier 1. As a result of this current pulse the output voltage V_4 decreases further by a same amount.

In the interval t_4 - t_6 the voltage of the input bit is comparatively low, which corresponds to a logic "0" in the present example. In this interval the switch S_4 is open, so that the first switching network is disconnected from the inverting input 3 of the amplifier 1. In the preceding clock period t_3 - t_4 the capacitor C_4 is charged to the reference voltage V_{ref} by means of the switches S_6 and S_7 . In the clock period t_4 - t_6 the switches S_5 and S_8 are closed. On point C this results in a negative voltage transient of a magnitude equal to the reference voltage. This gives rise to a negative voltage transient on point D and hence on the inverting input 3, but this transient is attenuated substantially as a result of the presence of the capacitor C_2 . Consequently, a positive voltage transient appears on the output 4, which transient exhibits a linear relationship with the voltage transient on the input 3, so that no distortion is introduced. The positive voltage transient on the output 4 produces a negative current pulse, so that the capacitors C_1 and C_4 are discharged and the voltage on the inverting input is restored to zero volts. In the period t_5 - t_6 the switches S_6 and S_7 are closed, so that the capacitor C_4 is again charged to the reference voltage V_{ref} .

In the clock period t_4 - t_5 the switches S_2 and S_3 in the switching network 10 are closed, so that the capacitor C_3 is charged to the reference voltage V_{ref} . In the next clock period t_5 - t_6 the switches S_1 and S_3 are closed, so that the capacitor C_3 is fully discharged.

In the interval t_6 - t_8 a logic 0 is again applied to the control means 40, so that again a negative current pulse is applied to the inverting input 3 of the amplifier. As a result of this, the output voltage V_4 increases to zero volts.

Thus, in the manner described above the consecutive input bits determine whether a current pulse is applied to or supplied by the capacitor C_1 and consequently whether the analog output voltage decreases or increases.

It is to be noted that in principle it is also possible to control the switches S_2 and S_6 by switching pulses derived from the digital input

signal and to control the switches S_4 and S_8 by the clock signal. However, this has the following drawback. The consecutive switching pulses by means of which the switch S_2 is then switched over contain low-frequency signal information, so that the voltage on point A will contain low-frequency components. These low-frequency signals may reach the inverting input 3 of the amplifier 1 via the stray capacitances of the switches and thus give rise to distortion of the output signal. If the switch S_4 is controlled by switching pulses derived from the digital input signal these low-frequency signals also appear on the inverting input 3 of the amplifier 1, but in this case the voltage level is very low because this input constitutes a virtual earth and stray capacitances have no effect at this point.

Fig. 3 shows a digital-to-analog converter in accordance with a second embodiment of the invention, identical parts bearing the same reference numerals in this Figure as in Fig. 1. The converter differs from that shown in Fig. 1 in that in the switching network 10 a switch S_9 is arranged in parallel with the switch S_3 and in the switching network 20 a switch S_{10} is arranged in parallel with the switch S_7 . The switches S_9 and S_{10} are controlled by switching pulses which are derived from the digital input signal I by the control means 40, in such a way that the switch S_9 is switched in the same way as the switch S_8 and the switch S_{10} is switched in the same way as the switch S_4 .

In the embodiment shown in Fig. 1 the switches S_3 and S_7 receive both clock pulses and switching pulses derived from the digital input signal. As a result of this, the switch S_7 remains closed in the case of consecutive bits of the value "1" and the switch S_3 remains closed in the case of consecutive bits of the value "0" (see Fig. 2). This may give rise to low-frequency signal on points B and D, caused by discharging of stray capacitances which signals give rise to distortion of the output signal. In the embodiment shown in Fig. 3 the switches S_3 and S_7 are switched by the clock pulses only, whilst the switching pulses derived from the digital input signal are applied to separate switches S_9 and S_{10} . As a result of this, at least one of the switches S_3 and S_9 in the switching network 10 and at least one of the switches S_7 and S_{10} in the switching network 20 is switched over after every clock period. This precludes the occurrence of low-frequency signals on points B and D, which may give rise to distortion of the output signal.

The scope of the invention is not limited to the embodiments shown. For example, as an alternative, the positive current pulses and the negative current pulses may, in principle, be generated by means of one switching network, in which case the steps which are performed simultaneously by the two switching networks should be performed after each other. In the present embodiment the non-inverting input 2 of the amplifier 1 and the switches connected thereto are connected to earth. However, instead they may be connected to

a point of non-zero potential. In the present embodiments the transistor switches are all of the same conductivity type. However, the switches to which the inverted clock signal is applied may be of the opposite conductivity type, which enables all the switches to be controlled by means of the same clock signal. In the present embodiments the charging and discharge times of the capacitors C_3 and C_4 are selected to be equal to each other. However, alternatively the discharge time may differ from the charging time.

Claims

1. A digital-to-analog converter for converting a one-bit coded signal into an analog signal, comprising an integrator for integrating current pulses of a first polarity when the coded signal has a first value and for integrating current pulses of a second polarity when the coded signal has a second value, which integrator comprises an operational amplifier having an inverting input, a non-inverting input which is coupled to a first terminal for a first reference voltage, and an output which is coupled to the inverting input at least by means of a first capacitor and a resistor, the converter further comprises at least a first switching network for generating the current pulses, which network is coupled to the inverting input of the amplifier and comprises a second capacitor, characterized in that a third capacitor is arranged between the inverting input of the amplifier and the first terminal, which third capacitor has a capacitance which is higher than that of the first capacitor and higher than that of the second capacitor.

2. A digital-to-analog converter as claimed in Claim 1, characterized in that the converter comprises a second switching network which is coupled to the inverting input of the amplifier and which comprises a fourth capacitor and the first switching network serves for generating current pulses of the first polarity and the second switching network serves for generating current pulses of the second polarity.

3. A digital-to-analog converter as claimed in Claim 2, characterized in that the first switching network comprises a first switch and a second switch, for connecting one pole of the second capacitor to the first terminal and to a second terminal for a second reference potential respectively, and a third switch and a fourth switch for connecting the other pole of the second capacitor to the first terminal and to the inverting input of the amplifier respectively, and the second switching network comprises a fifth switch and a sixth switch, for connecting one pole of the fourth capacitor to the first terminal and the second terminal respectively, and a seventh switch and an eighth switch, for connecting the other pole of the fourth capacitor to the first terminal and to the inverting input of the amplifier respectively.

4. A digital-to-analog converter as claimed in Claim 3, characterized in that the converter comprises clock means for closing the first switch, the

third switch, the sixth switch and the seventh switch during a first clock period and for closing the second and the fifth switch during a second clock period and the converter comprises control means controlled by the one-bit coded signal for closing the fourth switch during the second clock period when the coded signal has the first value and for closing the eighth switch during the second clock period when the coded signal has the second value.

5. A digital-to-analog converter as claimed in Claim 4, characterized in that the converter comprises a ninth switch, arranged in parallel with the third switch, and a tenth switch, arranged in parallel with the seventh switch, which ninth switch and tenth switch are controlled by the control means in the same way as the eighth switch and the fourth switch respectively.

Patentansprüche

1. Digital/Analog-Wandler zum Umsetzen eines codierten Einbitsignals in ein analoges Signal, mit einem Integrator zum Integrieren vom Stromimpulsen einer ersten Polarität, wenn das codierte Signal einen ersten Wert hat, und zum Integrieren von Stromimpulsen einer zweiten Polarität, wenn das codierte Signal einen zweiten Wert hat, wobei der Integrator einen Operationsverstärker mit einem Umkehreingang, einem Nichtumkehreingang, der an eine erste Klemme für eine erste Referenzspannung angeschlossen ist, und einem Ausgang enthält, der wenigstens über einen ersten Kondensator und einen Widerstand an den Umkehreingang angeschlossen ist, wobei der Wandler außerdem wenigstens ein erstes Schaltnetz zum Erzeugen der Stromimpulse enthält, und das Schaltnetz an den Umkehreingang des Verstärkers angeschlossen ist und einen zweiten Kondensator enthält, dadurch gekennzeichnet, daß zwischen dem Umkehreingang des Verstärkers und der ersten Klemme ein dritter Kondensator angeordnet ist, dessen Kapazität größer als die des ersten Kondensators und größer als die des zweiten Kondensators ist.

2. Digital/Analog-Wandler nach Anspruch 1, dadurch gekennzeichnet, daß der Wandler ein zweites Schaltnetz enthält, das an den Umkehreingang des Verstärkers angeschlossen ist und einen vierten Kondensator enthält, wobei das erste Schaltnetz zum Erzeugen von Stromimpulsen der ersten Polarität und das zweite Schaltnetz zum Erzeugen von Stromimpulsen der zweiten Polarität vorgesehen ist.

3. Digital/Analog-Wandler nach Anspruch 2, dadurch gekennzeichnet, daß das erste Schaltnetz einen ersten Schalter und einen zweiten Schalter zum Anschließen eines Pols des zweiten Kondensators an die erste Klemme bzw. an eine zweite Klemme für ein zweites Referenzpotential sowie einen dritten Schalter und einen vierten Schalter zum Anschließen des anderen Pols des zweiten Kondensators an die erste Klemme bzw. an den Umkehreingang des Verstärkers enthält, und das zweite Schaltnetz einen fünften Schalter und

a point of non-zero potential. In the present embodiments the transistor switches are all of the same conductivity type. However, the switches to which the inverted clock signal is applied may be of the opposite conductivity type, which enables all the switches to be controlled by means of the same clock signal. In the present embodiments the charging and discharge times of the capacitors C_3 and C_4 are selected to be equal to each other. However, alternatively the discharge time may differ from the charging time.

Claims

1. A digital-to-analog converter for converting a one-bit coded signal into an analog signal, comprising an integrator for integrating current pulses of a first polarity when the coded signal has a first value and for integrating current pulses of a second polarity when the coded signal has a second value, which integrator comprises an operational amplifier having an inverting input, a non-inverting input which is coupled to a first terminal for a first reference voltage, and an output which is coupled to the inverting input at least by means of a first capacitor and a resistor, the converter further comprises at least a first switching network for generating the current pulses, which network is coupled to the inverting input of the amplifier and comprises a second capacitor, characterized in that a third capacitor is arranged between the inverting input of the amplifier and the first terminal, which third capacitor has a capacitance which is higher than that of the first capacitor and higher than that of the second capacitor.

2. A digital-to-analog converter as claimed in Claim 1, characterized in that the converter comprises a second switching network which is coupled to the inverting input of the amplifier and which comprises a fourth capacitor and the first switching network serves for generating current pulses of the first polarity and the second switching network serves for generating current pulses of the second polarity.

3. A digital-to-analog converter as claimed in Claim 2, characterized in that the first switching network comprises a first switch and a second switch, for connecting one pole of the second capacitor to the first terminal and to a second terminal for a second reference potential respectively, and a third switch and a fourth switch for connecting the other pole of the second capacitor to the first terminal and to the inverting input of the amplifier respectively, and the second switching network comprises a fifth switch and a sixth switch, for connecting one pole of the fourth capacitor to the first terminal and the second terminal respectively, and a seventh switch and an eighth switch, for connecting the other pole of the fourth capacitor to the first terminal and to the inverting input of the amplifier respectively.

4. A digital-to-analog converter as claimed in Claim 3, characterized in that the converter comprises clock means for closing the first switch, the

third switch, the sixth switch and the seventh switch during a first clock period and for closing the second and the fifth switch during a second clock period and the converter comprises control means controlled by the one-bit coded signal for closing the fourth switch during the second clock period when the coded signal has the first value and for closing the eighth switch during the second clock period when the coded signal has the second value.

5. A digital-to-analog converter as claimed in Claim 4, characterized in that the converter comprises a ninth switch, arranged in parallel with the third switch, and a tenth switch, arranged in parallel with the seventh switch, which ninth switch and tenth switch are controlled by the control means in the same way as the eighth switch and the fourth switch respectively.

Patentansprüche

1. Digital/Analog-Wandler zum Umsetzen eines codierten Einbitsignals in ein analoges Signal, mit einem Integrator zum Integrieren von Stromimpulsen einer ersten Polarität, wenn das codierte Signal einen ersten Wert hat, und zum Integrieren von Stromimpulsen einer zweiten Polarität, wenn das codierte Signal einen zweiten Wert hat, wobei der Integrator einen Operationsverstärker mit einem Umkehreingang, einem Nichtumkehreingang, der an eine erste Klemme für eine erste Referenzspannung angeschlossen ist, und einem Ausgang enthält, der wenigstens über einen ersten Kondensator und einen Widerstand an den Umkehreingang angeschlossen ist, wobei der Wandler außerdem wenigstens ein erstes Schaltnetz zum Erzeugen der Stromimpulse enthält, und das Schaltnetz an den Umkehreingang des Verstärkers angeschlossen ist und einen zweiten Kondensator enthält, dadurch gekennzeichnet, daß zwischen dem Umkehreingang des Verstärkers und der ersten Klemme ein dritter Kondensator angeordnet ist, dessen Kapazität größer als die des ersten Kondensators und größer als die des zweiten Kondensators ist.

2. Digital/Analog-Wandler nach Anspruch 1, dadurch gekennzeichnet, daß der Wandler ein zweites Schaltnetz enthält, das an den Umkehreingang des Verstärkers angeschlossen ist und einen vierten Kondensator enthält, wobei das erste Schaltnetz zum Erzeugen von Stromimpulsen der ersten Polarität und das zweite Schaltnetz zum Erzeugen von Stromimpulsen der zweiten Polarität vorgesehen ist.

3. Digital/Analog-Wandler nach Anspruch 2, dadurch gekennzeichnet, daß das erste Schaltnetz einen ersten Schalter und einen zweiten Schalter zum Anschließen eines Pols des zweiten Kondensators an die erste Klemme bzw. an eine zweite Klemme für ein zweites Referenzpotential sowie einen dritten Schalter und einen vierten Schalter zum Anschließen des anderen Pols des zweiten Kondensators an die erste Klemme bzw. an den Umkehreingang des Verstärkers enthält, und das zweite Schaltnetz einen fünften Schalter und



einen sechsten Schalter zum Anschließen eines Pols des vierten Kondensators an die erste Klemme bzw. an die zweite Klemme sowie einen siebten Schalter und einen achten Schalter zum Anschließen des anderen Pols des vierten Kondensators an die erste Klemme bzw. an den Umkehreingang des Verstärkers enthält.

4. Digital/Analog-Wandler nach Anspruch 3, dadurch gekennzeichnet, daß der Wandler Taktgeber zum Schließen des ersten Schalters, des dritten Schalters, des sechsten Schalters und des siebten Schalters in einer ersten Taktzeit und zum Schließen des zweiten und des fünften Schalters in einer zweiten Taktzeit sowie außerdem Steuermittel, die durch das codierte Einbitsignal zum Schließen des vierten Schalters in der zweiten Taktzeit gesteuert werden, wenn das codierte Signal den ersten Wert hat, und zum Schließen des achten Schalters in der zweiten Taktzeit enthält, wenn das codierte Signal den zweiten Wert hat.

5. Digital/Analog-Wandler nach Anspruch 4, dadurch gekennzeichnet, daß der Wandler einen zum dritten Schalter parallel geschalteten neunten Schalter und einen zum siebten Schalter parallel geschalteten zehnten Schalter enthält, wobei die neunten und zehnten Schalter genau so wie der achte Schalter bzw. der vierte Schalter von den Steuermitteln gesteuert werden.

Revendications

1. Convertisseur numérique-analogique pour convertir un signal codé à 1 bit en un signal analogique, comportant un intégrateur pour l'intégration d'impulsions de courant d'une première polarité lorsque le signal codé présente une première valeur et pour l'intégration d'impulsions de courant d'une seconde polarité lorsque le signal codé présente une seconde valeur, lequel intégrateur comporte un amplificateur opérationnel présentant une entrée inverseuse, une entrée non inverseuse qui est couplée à une première borne pour une première tension de référence et une sortie qui est couplée à l'entrée inverseuse au moins à l'aide d'un premier condensateur et d'une résistance, le convertisseur comportant en outre au moins un premier réseau de commutation pour engendrer les impulsions de courant, lequel réseau est couplé à l'entrée inverseuse de l'amplificateur et comporte un deuxième condensateur, caractérisé en ce qu'un troisième condensateur est disposé entre l'entrée inverseuse de l'amplificateur et la première borne, lequel condensateur présente une capacité qui est supérieure à celle du premier condensateur et supérieure à celle du deuxième condensateur.

2. Convertisseur numérique-analogique selon

la revendication 1, caractérisé en ce que le convertisseur est muni d'un deuxième réseau de commutation qui est couplé à l'entrée inverseuse de l'amplificateur et qui est muni d'un quatrième condensateur et en ce que le premier réseau de commutation sert à engendrer les impulsions de courant de la première polarité, le deuxième réseau de commutation sert à engendrer des impulsions de courant de la deuxième polarité.

3. Convertisseur numérique-analogique selon la revendication 2, caractérisé en ce que le premier réseau de commutation est muni d'un premier commutateur et d'un deuxième commutateur pour respectivement la connexion d'un pôle du deuxième condensateur à la première borne et à une deuxième borne pour un deuxième potentiel de référence et d'un troisième commutateur et d'un quatrième commutateur pour la connexion de l'autre pôle du deuxième condensateur respectivement à la première borne et à l'entrée inverseuse de l'amplificateur, et en ce que le deuxième réseau de commutation est muni d'un cinquième commutateur et d'un sixième commutateur pour la connexion d'un pôle du quatrième condensateur respectivement à la première borne et d'un septième commutateur et d'un huitième commutateur pour la connexion de l'autre pôle du quatrième condensateur respectivement à la première borne et à l'entrée inverseuse de l'amplificateur.

4. Convertisseur numérique-analogique selon la revendication 3, caractérisé en ce que le convertisseur est muni de moyens d'horloge pour la fermeture du premier commutateur, du troisième commutateur, du sixième commutateur et du septième commutateur pendant une première période d'horloge et pour la fermeture du deuxième commutateur et du cinquième commutateur pendant une deuxième période d'horloge et en ce que le convertisseur est muni de moyens de commande commandés par un signal codé à 1 bit pour la fermeture du quatrième commutateur pendant la deuxième période d'horloge lorsque le signal codé présente la première valeur et pour la fermeture du huitième commutateur pendant la deuxième période d'horloge lorsque le signal codé présente la deuxième valeur.

5. Convertisseur numérique-analogique selon la revendication 4, caractérisé en ce que le convertisseur comporte un neuvième commutateur monté en parallèle avec le troisième commutateur et un dixième commutateur monté en parallèle avec le septième commutateur, lesquels neuvième commutateur et dixième commutateur sont commandés par des moyens de commande de la même façon que respectivement le huitième commutateur et le quatrième commutateur.

