

The invention relates to a method for managing an electronic memory, the content of which represents predetermined homogeneous units, and to a system for implementing this method.

There are known electronic systems that comprise a memory, the content of which represents predetermined homogeneous units and which implement particular methods for managing this memory. For example, electronic payment systems are known that use a memory-type card. In such systems, at least one zone of the memory of the card is intended for making an accounting entry for transactions, or storing them, with a view to their payment. Elementary cells in the zone then represent homogeneous payment units, and the card can be prepaid, that is, the credit allocated depends on an amount of money actually paid in advance, or else the consumption of units can be used for the preparation of a subsequent invoice. Of course, the example of payment systems is in no way limiting, and other applications have already been envisaged. For example, such a memory can be used to make an accounting entry for all sorts of transactions that do not necessarily require compensation in the form of payment.

In such systems, the zone of the memory used for accounting is generally an electrically programmable memory (EPROM-type memory), and each time there is an accounting operation, the management unit of the memory modifies the structure of the latter by "gridding" at least one cell of the unit.

In the earliest projects for payment systems using an electronic memory, the initial credit was represented by a number of non-gridded cells in the zone, and each transaction was accompanied by the gridding of a cell in the zone as follows: the reading of the elements available in the memory zone allocated to transactions was performed in one direction, and the writing (gridding) in another direction. On reading, the credit limit was found when the management system detected the first gridded cell that it encountered. Before a first transaction the convention was that a first gridded cell was considered to exist at the end of the zone. At the time of a transaction, the system was positioned just before the first gridded cell encountered in reading and it counted out the number of units corresponding to the transaction,

then gridded the last cell counted. Thus, in so far as the various transactions involved several units, there remained non-gridded cells between the first gridded cell encountered on reading and the end of the zone. These first systems had the major disadvantage not being rechargeable, that is, when the credit was exhausted, it was not possible to re-use the memory.

To remedy these disadvantages, methods have been envisaged for managing the memory that allow recharging, that is, the allocation of new units when the initial credit is exhausted, or is on the point of being so. Thus, in the case of payment systems with memory-type cards, the possibility of allocating further credit has been envisaged.

Recharging, or the allocation of further credit, consists of rendering capable of use at least some of the cells located beyond the first gridded cell encountered in read mode. For this, methods and systems have been devised that made it possible, on reading, to ignore the cells gridded during previous transactions. For this purpose, at the time of a transaction, action is generally taken on one cell that is gridded and, at the time of recharging, action is taken by gridding another cell paired with the first one which, according to its state, indicates whether the first one is the actual credit limit, or else must be ignored, recharging having taken place. Methods and systems based on the principle are known from European patent application no. 0 227 532 and French patent application 2 605 431.

In the European application, the memory intended for making accounting entries for units is separated into two zones of equal capacity, a first one known as the payment zone, and a second one known as the recharging zone. At the beginning, when the memory is blank, all the binary cells are in a given logic state, corresponding for example to logic "1". The allocation of an initial credit of N units, if N is less than the capacity of the memory, consists of gridding, in the recharging zone, the $N + 1$ st cell encountered in reading, starting from the beginning of this zone, such that a stop is constituted by a pair (A, B) of cells, of binary value (1, 0), A being the cell ranked $N + 1$ in the payment zone and B the cell ranked $N + 1$ in the recharging zone. At the time of a transaction requiring the debiting of units, starting

at the beginning of the zones, as many pairs are counted as there are units to debit, and the state of the last cell counted in the payment zone is modified, without affecting the state of the corresponding cell in the recharging zone.

At the time of another transaction, a search is made for where the last gridded cell is located in the payment zone, and a count is made beyond that cell, toward the stop, of as many pairs as there are units to debit. Of course, in all cases, if the transaction involves a number of units exceeding the number available, then the transaction is refused.

At the time of recharging, the management unit starts by making an accounting entry for the balance of the card at the time of the instruction to recharge, that is, the number of pairs in their original state located between the last modified pair and the stop initially placed, then, starting again from the beginning of the zones, it places a new stop after a number of intact pairs equal to the amount to be recharged, added to the balance, is counted. The stop is produced with the pair ranking immediately higher than the result of the addition. Following this creation of a new stop, the unmodified cell out of all the pairs that had a modified cell between the creation of the previous stop and the creation of the present stop, that is, the pairs corresponding to the old stop and to the prior transactions, is modified in turn, such that subsequent operations ignore these pairs.

This method has various disadvantages in its implementation.

On the one hand, the difference between the constitution of the pairs indicating the stop and that of the pairs indicating the various transactions that have taken place makes it essential to have a relatively complicated operating system, since each pair can take four possible configurations, namely the state 1,1 corresponding to an available unit, the state 0,1 corresponding to a transaction, the state 1,0 corresponding to a stop and, finally, the state 0,0 corresponding to a pair to be ignored; on the other hand, at the time of a transaction, it is necessary to read at least once the whole of the memory element by element, up to the stop, in order to identify the position of the pair written at the last transaction; finally, recharging is

relatively complicated since, after having positioned a new stop, the whole memory zone located between this new stop and the beginning of the zone has to be reread, in order to neutralise the previous stop on the one hand and, on the other hand, to neutralise the pairs modified at the time of the series of previous transactions.

The invention described in French patent application 2 605 431 makes it possible to remedy some of these disadvantages since there is no longer any difference between the stop and the recordings made at the time of the transactions. Before a transaction, the operating system searches for the stop previously placed and creates a new stop near the beginning of the zone.

The memory comprises a single zone constituted of elements each having an address and an even number of cells. When the memory is in its initial state, each element is said to be even; when it comprises an odd number of cells in their initial state, the element in question is said to be odd; when all the cells are modified, then the element is said to be neutral.

The positioning of a stop consists of making an element that was previously even into an odd one, by modifying the state of one of its cells, and the recharging consists of making odd elements available by making them even once more, while ignoring the elements that no longer have a modifiable cell.

Before each transaction, the balance is determined by the number of even, non-neutral elements encountered before the stop, which is therefore the first odd-numbered element encountered in reading.

This process has the major disadvantage that searching for the last stop, before any transaction, requires reading cell by cell from the beginning of the memory, in order to determine the parity of each element, since the stop is constituted by the first odd-numbered element encountered in reading.

Furthermore, any one element which, at the start, contains an even number of cells greater than two, for example, four, six or more, can be used for several

transactions after recharging, which considerably complicates management. Indeed, recharging consists of creating a new stop near the bottom of the memory, while making available, that is, even, the odd-numbered elements comprised between the last stop before recharging and the new one to be created, that is, all the elements that have been modified at the time of the last series of transactions before recharging, and moreover, the creation of the new stop must take account of the fact that some of said elements which had been made odd, including the last stop, are capable of becoming neutral while others will still be usable.

It is therefore necessary, on the one hand, to make an accurate accounting entry for the number of reusable elements and, on the other hand, to determine the parity of all the elements encountered since the beginning of the zone, reading it cell by cell, which considerably increases the processing time. Furthermore, as in the other method of the prior art, a large number of cells have to be modified on recharging, which presents significant risks of error, and of loss of money in the case of payment devices.

To remedy these disadvantages, the invention proposes a method in accordance with Claim 1 and a system in accordance with Claim 8.

The invention is particularly advantageous in that it allows a considerable saving of time in processing transactions while offering great security compared with the systems of the prior art. Indeed, at the time of a transaction, the search for the previous stop is no longer performed by reading the memory cell by cell but element by element, which makes possible the current systems which generally comprise processing units, and are capable of working more rapidly in a given, non unitary, format, than cell by cell. Reading cell by cell takes place only in a pair of elements in which the possible presence of the stop has been detected. Furthermore, at the time of recharging, it is no longer necessary to neutralise the stops created at the time of the various transactions that have taken place since the previous recharging, since the neutralisation of a stop takes place just after the creation of the following stop, which increases the security of the operations, since each operation is now accompanied only by the modification of two cells: one cell in a series of elements

to create the new stop, and one cell in the other series in order to neutralise the transaction unit constituting the previous stop. This helps to reduce the risks of error, and therefore of the loss of units.

The systems of the prior art made it necessary to neutralise one cell in each transaction unit that had been modified since the previous recharging, which increased the risks of error, especially where, for a technical reason, it was impossible to modify one of the cells. Furthermore, neutralisation required a perfect knowledge of the state of the memory (re-reading, for example), which made the operations complex.

Other characteristics and advantages of the invention will become apparent with the following description made with regard to the attached figures in which:

- Figures 1 and 2 illustrate two possible variants for organising the memory of a system for implementing the method of the invention;
- Figures 3 to 19 illustrate different configurations that can be taken by the memory zone reserved for making accounting entries for predetermined homogeneous units, during the various operating phases (transaction or recharging).

In the variant illustrated by Figure 1, the two series Z1, Z2 of elements comprise the same number n of elements each having a same non-unitary number k of cells (C1, C2, ... Ck).

The first series Z1 contains for example the elements E11, E12, ... E1n in which one cell is modified in order to create the new stop at the time of a transaction, and the second series Z2 then contains the elements E21, E22, ... E2n, which comprise the cells, of which one is modified after a transaction to neutralise the previous stop.

Each element can be identified in memory by its address, for example T1, T2, ... Tn for the elements in the first series and N1, N2, ... Nn for the elements in the second.

Furthermore, an element in the first series is paired with an element in the second; for example, in the example, the element E11, with the address T1, in the first series is paired with the element E21, with the address N1 in the second, etc., as far as the element E1n, with the address Tn in the first series, which is paired with the element E2n, with the address Nn in the second.

Furthermore, each cell of an element in the first series is paired with a given cell of the corresponding element in the second series. It is this pair of cells, constituted in this way, that forms a transaction unit. The management of the memory is performed by a processing unit structured around a microprocessor, and in order to facilitate the task of the latter, one cell of an element in one series is paired with the cell having the identical significance in the corresponding element of the other series.

What has been illustrated with regard to Figure 1 for the relative arrangement of the elements among themselves has no other object than to facilitate the understanding of the method of the invention. Clearly, a different organisation could be envisaged, the only prime aspect being that pairs of elements are constituted, and that it is known how to rapidly manage the system in order to reconstitute said pairs of elements, and that it is also known how to rapidly reconstitute each pair of cells constituting a transaction unit.

The memory could therefore be organised differently, for example as illustrated by Figure 2, in which the pairs of elements constituted follow each other in the memory, the first element E11 in the first series being at an address A1, its corresponding one E21 in the second series being at the address A2, the second element E12 in the first series being at the address A3, its corresponding one E22 in the second series being at the address A4, and so on, up to the last element E2n in the second series which is at an address Af.

All other intermediate configurations may be envisaged, as long as they do not significantly prejudice processing time.

As described above, all the elements contain the same non-unitary number of memory cells and the speed of processing times is obtained by reading the memory element by element. Each element comprises a number of cells corresponding to the processing format of the associated management unit. Indeed, to be usable, the memory must be associated with a processing or management unit which, as already indicated above, can be a microprocessor. This will be the case for example for memory-type cards having the function of an electronic wallet, that is, capable of use for making payments. In such a case, the processing format will, for example, be the 8-bit byte which corresponds to the usual working format of microprocessors incorporated into memory-type cards, and each element will then comprise eight cells.

It is the choice of such a structure that allows considerable time-saving in processing, in comparison with devices of the prior art which, by reason of their configuration, make cell-by-cell processing imperative. Known microprocessors work more easily on a number of cells corresponding to their working format than cell by cell. In the rest of the description, the examples will be illustrated with the assumption that the working format of the processing unit associated with the memory is the 8-bit byte, although this is by no means limiting, but since it corresponds to a format commonly used in the field of memory-type cards, which constitutes a particularly interesting implementation of the method of the invention, for an electronic payment application.

Figure 3 illustrates the original state, of a portion of the memory allocated to making accounting entries for transactions with the aid of predetermined homogeneous units. To determine easily the quantity of available transaction units, the elements are stored in a given order so that the management unit can read them or make recordings therein, taking account of said order in order to avoid accounting errors. Thus, for example, referring to Figures 1 and 3, it will be noted that the elements in the first series Z1 are stored in the ascending order of their addresses, from T1 to Tn, and similarly the elements in the second series Z2 are stored in the ascending order of their addresses from N1 to Nn. Furthermore, the most significant cell in

each element is considered to be the first cell in the element. In the example illustrated, the most significant value is "7", and the least significant, "0".

At the start, all the cells are for example in the logic state "0", and the writing or gridding of a cell causes it to change to the logic state "1". Of course, this is a matter of convention.

Also by convention, the first series Z1 will be called the transaction series, since it is in this series that the cell marking the new stop will be written at the time of a transaction, and the second series Z2 will be called the neutralisation series, since it is in this series that the neutralisation cell of the previous stop will be written.

Furthermore, on reading what has been written above, for the rest of the description, the start of the first series Z1 will be the most significant cell of the element with the address T1, the end of this series being constituted by the least significant cell of the element with the address Tn, and the start of the second series Z2 will be the most significant cell of the element with the address N1, its end being the least significant cell of the element with the address Nn.

Furthermore, by preference, it will be considered that a transaction unit is constituted of a pair formed by a cell of a given significance in an element of the transaction series, and by the cell of the same significance in the corresponding element of the neutralisation series. Such a unit is blank, that is, consumable, when both its cells are in their original state, in this case the state "0", and it constitutes a stop when its cell in the transaction zone is in the logic state "1", its other cell being in its original state, and it is neutralised, that is, considered to be logically non-existent, when both its cells are modified.

Prior to the start of a transaction in a system implementing the method of the invention, it is necessary on the one hand to reserve a certain amount of memory or elements for making accounting entries for transactions, that is, to reserve the two series Z1 and Z2, other zones being able to serve for other things (this reservation can, it will be remembered, involve the whole memory). On the other

hand, after the reservation has been made, a balance of transaction units has to be constituted since, at the start, the balance, that is, the transaction power expressed in units, is zero; on the other hand the system has an accreditive power, that is, a certain number of transaction units that can be used to constitute the balance. Furthermore, a transaction will be accompanied by a debiting of units within the limit of the balance, or a crediting of units within the limit of the accreditive power, depending on whether a consumption or recharging is involved.

Figures 3 and 5 to 19 cover the case where the zone allocated to making accounting entries for homogeneous units comprises 32 transaction units, that is, is constituted of four 8-bit bytes in the transaction series and four 8-bit bytes in the neutralisation series.

Figure 3 illustrates perfectly the correspondence between the cells of each element in the transaction series, and the cells of each element in the neutralisation series, forming the transaction units.

Initially, it is considered that the accreditive power is equal to the number of transaction units reserved in the memory, less one. In the example chosen, the accreditive power is therefore 31 transaction units. At the same time, the balance is zero. Any debiting is therefore impossible, until at least one credit operation has taken place.

The assumption that the accreditive power is initially equal to the number of reserved transaction units less one is particularly advantageous since this makes it possible to contribute to the time-saving during transactions. Indeed, it is noted that, until a credit operation has taken place, all the transaction units are in their original state and are available. Reading the two series at that time makes it possible to detect this state. If it were admitted that the accreditive power corresponded to the number of reserved transaction units, this would be equivalent to authorising an initial credit to be effected such that the balance before an initial transaction would correspond to the number of units actually reserved. Now, reading the transaction and neutralisation series would not allow the processing unit

to detect whether the memory is in a state corresponding to a maximum accreditive power, or to a maximum balance. In order for this detection to take place, it would then be necessary to reserve in memory another complementary zone of the two series Z1, Z2, in order to check that a credit operation has already taken place, which would oblige the processing unit to read this specially reserved memory zone, and would increase the processing time and complicate the implementation process. For this reason, in order to simplify the implementation of the method, it is preferred to consider that the accreditive power of the blank memory is equal to the number of reserved transaction units less one, such that at the time of the first credit operation, at least one actual stop can be created at the last pair of cells located in the last element of the reserved series, which is equivalent to saying in other words that the initial balance can be at most equal to the number of reserved transaction units less one.

As will be demonstrated below, the method of the invention is particularly advantageous, in that, whether at the time of a debit operation or a credit operation, it entails the implementation of identical functions, after having very quickly searched for the position of the stop. After its precise position has been detected, and depending on this position, it may be possible to carry out, either solely a debit operation or solely a credit operation, or else one or other of these operations. For example, following the reservation of zones for making accounting entries for transactions, that is, where no credit operation has yet taken place, any debit operation is impossible; only a credit operation can take place.

The case can occur where the balance is maximum, that is, when the stop is detected on the last available transaction unit; in this case only a debit can take place.

Finally, cases can occur where the stop is detected elsewhere in the zone, and in this case it may be possible to authorise either debit operations or credit operations. In such a case, the refusal of a debit operation or a credit operation may for example be caused by the fact that the operation concerns a transaction involving a number of transaction units greater than the authorised debit or credit.

Thus, a debit or a credit may be authorised only if the state of the memory is compatible with the amount of the transaction envisaged.

In accordance with the invention, in order to detect rapidly the position of the stop, the processing device associated with the memory is arranged so as to perform a logic operation between the content of each element in the transaction series, and its equivalent in the neutralisation series. The logic operation chosen gives a particular result where the stop is detected in a given pair of elements. When a result indicates that the stop is present in a pair of elements, then its precise position in said pair of elements is sought, for example by reading all the cells of the element of said pair, located in the transaction series, until a cell modified in comparison with its initial state is found in this element, then by checking whether or not said modified cell belongs to the stop. Indeed, it can happen that a modified cell in the first series belongs to the stop or to a neutralised unit.

The mere detection of a modified cell in an element of the first series is therefore not sufficient to confirm that that cell belongs to the stop. In the case of a stop, the corresponding cell in the element in the second series Z2 is not modified in comparison with its original state, while, in the case of a neutralised unit, said corresponding cell is modified. It is therefore necessary to determine whether or not the corresponding cell of the corresponding element in the second series is modified in order to know whether said cell belongs to a neutralised unit or to the stop.

In practice, searching for the pair of elements in which the transaction element corresponding to the stop is located takes place for example by comparing each element in the transaction series in succession, in the order of ascending addresses, with the corresponding element in the neutralisation series.

Indeed, it will be noted, by comparing the elements of each series making up any one pair that, where the stop exists, then the element in the first series is different from its corresponding one in the second series.

This is illustrated in Figure 4, with a configuration that at a given moment can be taken by the memory which, in order not to cause an overload, would be composed of four pairs of elements each constituted by a 4-bit byte of cells. The upper portion of the figure shows the content of the first series Z1 which can correspond to the transaction series, the intermediate portion represents the second series Z2 which can be the neutralisation series and the lower portion gives the results R1 to R4 of a comparison applied to each pair of elements and would give a positive result for elements containing the stop. The pair P1 of elements is constituted solely of cells in their original state. The pair P2 contains two available transaction units (state 0,0) and two neutralised transaction units (state 1,1). The pair P3 contains two available transaction units, one neutralised unit and the stop B. The pair P4 contains solely neutralised transaction units.

In a particularly advantageous embodiment, the comparison between an element in the first series Z1, and its corresponding one in the second one Z2, is carried out by applying the "EXCLUSIVE OR" function between said elements.

Indeed, where the two elements in question are different, that is, when they contain the stop, then the result of applying the "EXCLUSIVE OR" function between these two elements is different from what would appear when the elements contain only available and/or neutralised transaction units.

Furthermore, simple logic functions, such as "EXCLUSIVE OR", are generally available on current processing units such as microprocessors. As explained above, current processing units have a non-unitary working format, which corresponds for example to the 8-bit byte, that is, it is possible to apply functions such as "EXCLUSIVE OR" between binary words, each constituted by eight cells. Other formats can be used.

It can therefore be noted that by working element by element, there is considerable time-saving compared with the methods of the prior art, which would involve working cell by cell.

Finally, it will be noted that the "EXCLUSIVE OR" function is particularly advantageous to use since it applies equally well where the original state of the cells is the logic level "0" and where this original state is the logic level "1".

When a pair of elements containing the stop has been detected, on comparison between each element in the first series Z1 and the corresponding one in the second series Z2, then the precise position of the stop is sought in this pair of elements, as explained above, by reading all the cells of the element of said pair, located in the transaction series Z1, then as soon as a cell of said element is detected as being modified in comparison with its original state, by looking to see whether or not the corresponding cell in the element of said pair, located in the neutralisation series Z2, is modified, in order to determine whether the modified cell in the transaction series belongs to a neutralised transaction unit or to the stop.

In a variant, at said pair of elements that has been detected as containing the stop, instead of reading a cell from the neutralisation series only when the corresponding one in the transaction series has been detected as being modified in comparison with its original state, in order to determine whether or not that cell in the neutralisation series is also modified, each cell in the transaction series and its corresponding one in the neutralisation series is read systematically, in said pair of elements, until a pair of cells is detected in which the cell in the transaction series is modified while the cell in the neutralisation series is not.

This variant does not increase the security of the check, but may be simpler to implement with certain particular types of processing units.

Figure 5 illustrates what would result from a comparison between the corresponding elements of the memory in its original state, as shown in Figure 3. In this case, each pair of elements would entail the appearance of a logic result with the level "0". Reading these results, starting from the beginning of the zone and going as far as the end, would not make it possible to detect the presence of a stop such that the processing unit would consider that the memory is in its original state and that only a credit operation, in order to constitute a balance, is possible. In Figure 5, the

result R1 is that of the comparison between the element in the transaction series located at the address T1 and the corresponding element in the neutralisation series located at the address N1, and so on, as far as the result Rn of the comparison between the elements with the address Tn in the transaction series Z1, and those with the address Nn in the neutralisation series Z2.

In a practical embodiment, cell-by-cell or element-by-element comparison circuits can easily be produced with conventional logic circuits, or these functions can be performed with the aid of a microprocessor with a suitable operating mode. In the case of a memory-type card incorporating a memory for managing predetermined homogeneous units, for example with a view to payment, and a microprocessor for managing this memory, it will be possible to configure the microprocessor to perform one and/or the other of these functions, depending on the choice made to determine the position of the stop.

The following will illustrate the various cases that can occur during the life of a system implementing the method of the invention.

As stated previously, before a first credit operation, that is, when the memory zone allocated to accounting contains only cells in their original state, the search for the stop does not make it possible to detect its presence in any of the elements. The system implementing the method then considers that there is a fictitious stop previous the memory zone allocated to accounting. In this case, only crediting is possible, and a credit operation is performed by displacing the fictitious stop from the beginning of the memory zone to the end, within the limit of the accreditive power. In this particular case of an initial credit, there are as yet no transaction units that have been neutralised. However, in general, the system must check that there are no such neutralised units, and the positioning of the new stop consists of leaving available the appropriate number of transaction units between the old stop, in this case a fictitious one, and the new stop. Thus, in a credit operation involving k units, the management unit counts k available transaction units and positions the stop at the k + 1st available unit encountered. The stop is recorded by modifying the state of the transaction cell of the pair that has to constitute the stop. In this particular

case of an initial credit, there is no neutralisation of the previous stop since it was fictitious.

Figure 6 illustrates the state of a memory containing 32 transaction units divided into elements constituted by 8-bit bytes. The transaction series contains four 8-bit bytes, with the addresses T1, T2, T3, T4, and the neutralisation series also contains four 8-bit bytes, with the addresses N1, N2, N3, N4. The credit involved 30 units, and it will be noted that the stop B1 was positioned at the 31st transaction unit by modifying the corresponding transaction cell.

In this particular case, the memory is available for debit operations, its balance is 30 transaction units and its accreditive power is 0 since there remains only one transaction unit between the stop B1 created and the end of the zone. As explained before, in order to simplify the management operations for the wallet, this last transaction element can serve only for constituting a stop, for it is not possible to consider the existence of a fictitious stop beyond the end of the zone since it would be necessary to reserve another zone in the memory to indicate to the system that such a fictitious stop existed. This would complicate management operations, since it would be necessary for the management unit systematically to read the state of this zone indicating whether or not a fictitious stop exists.

In general, the accreditive power is constituted by the number of available transaction units less one located between the last stop positioned and the end of the zone.

A debit operation consists of displacing the stop towards the beginning of the memory zone allocated to the accounting of transactions. The first operation performed is the search for the stop as described above, by comparing the elements pair by pair, then a precise search for the position in the pair of elements in which the stop has been detected.

After this detection of the stop, the debit operation consists of creating a new stop between the previous one and the start of the zone. This has to take place within

the limit of the balance while taking account of any units neutralised in previous operations. As explained before, the fact that an element is neutralised results in the presence of a cell modified in comparison with its original state in the series of neutralisation elements. Thus, to displace the stop, the management unit associated with the memory counts the number of cells in the series of neutralisation elements which have not been modified, skipping over any which have been modified, and when a number of cells corresponding to the number of units to be debited for the transaction has been counted, the management unit modifies the state of the transaction cell paired with the last cell in the neutralisation series that has been counted.

Figure 7 illustrates this counting in the series of neutralisation elements: the management unit counts a number of unmodified cells, starting from the neutralisation cell of the last stop, and aims at the last cell counted out. In the case illustrated by Figure 7, the counting involves four units. Following the creation of a new stop, the management unit modifies the state of the cell located in the neutralisation series Z2 of the previous stop, such that, after the debit and neutralisation operation, the memory takes a configuration as illustrated by Figure 8. The 31st transaction unit which corresponded to the previous stop B1 is neutralised, and the 27th transaction unit constitutes the new stop B2 after a debit of four units. The balance is then 26 units and the accreditive power 3 units.

Preferably, the system is arranged so that credit and debit operations cannot be repeated when the number of neutralised units is too great, limiting the accreditive power and making the system difficult to exploit. In this case, either a new memory zone is allocated in another device, or else, if there is still a memory zone available in the system used, then another zone is reserved to allow the accounting of homogeneous units.

Figure 9 illustrates the state of the memory after a further debit of seven units. A search is made for the position of the new stop B3 by counting the number of unmodified cells in the neutralisation series since the previous stop B2. In this particular case, since the system is still in a phase where there has been no

recharging, all the cells in the neutralisation series which have been encountered in reading since the last stop were in their initial state and it has not therefore been necessary to make a shift taking account of the transaction units that would have been cancelled previously. It will also be noted in this figure that the previous stop B2 was cancelled after the positioning of the new stop (state of its cells 1,1).

Figure 10 illustrates the state of the memory after a further debit, this time involving ten units. Once again, the search for the position of the new stop B4, after detecting the old one B3, by counting the number of unmodified cells in the neutralisation series located in front of the position of the previous stop B3, has not made it possible to detect any cells previously modified, which results in the debit being accompanied by the positioning of the new stop B4 at the tenth transaction unit encountered starting from the last stop, in the balance zone.

After this operation, the balance is nine units and the accreditive power 18 units.

Figure 11 illustrates the state of the memory following the previous debit operations and a credit of 17 units.

A first phase consists of searching for the position of the stop B4. This search has made it possible to determine the address of the element in the neutralisation series and the significance of the cell in this series corresponding to the stop B4, so as to perform the credit operation starting from said stop. As for a debit, the credit consists of making accounting entries for the cells in the neutralisation series, located between the detected stop B4 and the end of that series, which were not modified in previous operations. Indeed, each cell in the neutralisation series detected as having been modified in comparison with its original state signifies the presence of a transaction element which is neutralised and thus incapable of use. Crediting consists of leaving free between the previous stop B4 and the new stop B5 as many transaction units as there are units involved in the credit.

In the example illustrated, the counting of 17 unmodified cells in the neutralisation zone led to the encountering of two cells modified at the last two debit operations,

respectively the fourth cell of the neutralisation element with the address N3 which had been recorded when the stop B3 was neutralised, and the third cell of the neutralisation element with the address N4 which had been neutralised at the time of the last but one debit operation (stop B2). The new stop B5 is then constituted on the sixth cells of the transaction element with the address T4 and the neutralisation element with the address N4.

A credit operation involving 18 units instead of the 17 illustrated by Figure 11 would have led to the stop being positioned at the last cells of the elements with the addresses T4 and N4, and a credit greater than 18 units would have been impossible in the case illustrated.

After the positioning of the new stop B5, the transaction unit corresponding to the previous stop B4 is cancelled by modifying the state of the neutralisation cell of that unit.

Figure 12 illustrates the state of the memory after a further debit of five units following the credit of seventeen illustrated by Figure 11. The search for the stop leads to the detection of the last stop B5 positioned after the credit, and the counting of the unmodified neutralisation cells between the stop and the beginning of the series, in order to detect the position of the new stop to be positioned, leads to the detection of a modified neutralisation cell, corresponding to the stop B2, such that the positioning of the new stop B6 has taken account of this modified cell encountered during the counting.

From reading the above, it will be noted that the method according to the invention allows great transparency of the operations, since the positioning of a new stop is systematically accompanied by the neutralisation of the transaction unit constituting the previous stop such that, especially at the time of recharging, there is no longer any need, as in the methods disclosed by the prior art, to reread the whole memory in order to neutralise the elements used, or else to make them available once more as is the case in the aforementioned French patent application. Taking account of the content of the neutralisation series, errors are avoided when counting units to

position the new stop, and the systematic neutralisation following the creation of a new stop makes it possible to obtain recharging times, that is, the times necessary for a credit operation, much faster than in the implementation of the methods of the prior art. Debiting or crediting entails systematically the implementation of the same operations, the only difference arising from the fact that the stop in the memory is not displaced in the same direction.

However, while the fact that the transaction units that constituted a stop are neutralised when the next stop is created makes it possible to obtain great security at the time of a credit operation, without having to use complicated management processes, it can happen that a system for implementing the method of the invention does not operate correctly and that, in particular, it is impossible to modify the state of a transaction cell when a new stop is created or else the state of a neutralisation cell when an attempt is made to neutralise the previous stop, following the creation of a new stop.

Malfunctions of such types have to be taken into account to guarantee that there is no loss of units at the time of transactions, which can be particularly damaging when such a memory is used in an electronic wallet. Indeed, malfunctioning of the memory entails losses of money.

A first type of dysfunction that can arise is the impossibility of modifying the state of the neutralisation cell of the previous stop, after the creation of a new stop.

This can occur after a debit operation. In this case, the old stop is located between the new one and the bottom of the zone allocated to transactions. This is illustrated by Figure 13 which reproduces the previous state of the memory illustrated in Figure 12, from which it was wished to make a debit of fifteen units. The new stop B7 is therefore located at the seventh-rank cells of the elements with the addresses T1 and N1, while the previous one B6 is located at the eighth cells of the elements with the addresses T3 and N3. It is this last stop B6 which cannot be neutralised, since its neutralisation cell cannot be modified. In this case, it is considered that the new stop B7 placed in the address elements T1 and N1, following the debit, indicates the

current limit of the balance, while the old stop which cannot be neutralised will be considered subsequently as the limit of the accreditive power of the memory. In this case, the new balance is equal to six units and the accreditive power is reduced to thirteen units while, if the stop for the previous transaction B could have been cancelled, it would have been seventeen units.

Thus, in such a case, the impossibility of neutralising the stop corresponding to a previous transaction results in a reduction in the accreditive power of the memory. Indeed, it is considered that the old stop constitutes the new bottom of the memory.

Figure 14 illustrates the case where it is impossible to neutralise the previous stop after a credit attempt.

The example illustrated comes from Figure 13 in which the previous stop B7 was positioned at the seventh-rank cells of the elements with the addresses T1 and N1. The credit attempt involves, for example, five units, such that the new stop B8, by taking account of the neutralised units encountered, is located at the sixth cells of the elements with the addresses T2 and N2. However, should it prove impossible to modify the state of the neutralisation cell of the previous stop and a new credit attempt is made, the system rejects the attempt and it is then considered that the old stop constitutes the limit of the memory zone allocated to the transactions, and therefore to the accreditive power. In other words, as in the previous case, the old stop which cannot be crossed becomes the new limit of the reserved zone.

Another type of dysfunction can consist in the impossibility of modifying the state of a transaction cell. In this case, the transaction should not be refused at any price, since the balance authorises such an operation, this being simply for the reason that the system for storing in memory is not functioning correctly. To remedy such a disadvantage during the use of a system implementing the method of the invention, a back-up method has been provided, the principle of which is the same whether the impossibility of gridding a transaction cell is the result of a debit operation or a credit operation.

The principle of this method is to create the stop at the available transaction unit of immediately higher rank, in the direction of the bottom of the memory, than that at which the stop should have been created. In the case of a debit, in no case may a stop shifted beyond the old stop, towards the bottom of the memory, be constituted. In the case of a credit, the possible limit of shifting will be the bottom of the memory. However, this shifting of the stop, if not followed by any other operation, has the effect of increasing the balance by one unit. In order to preserve the correct value of the balance, after the creation of the stop with a shifted rank, one transaction unit available in the balance zone, that is, in the portion of the memory allocated to transactions located between the beginning of the memory zone, as defined, and the new stop, is neutralised.

After the creation of the shifted stop and the neutralisation of that unit, the previous stop is neutralised.

Should it prove impossible to neutralise the previous stop, that is, to modify its neutralisation cell, then one comes back to the problem detailed above, that is, a reduction in the accreditive power, limited by the previous stop, is considered.

More specifically, the operation of creating a shifted stop, after it has proved impossible to create a stop at the pair of cells at which it should have been created, can be broken down into several phases:

- a first phase therefore consists of determining which transaction unit ranking immediately higher than that at which the stop should have been created, is available;
- the second phase consists of gridding the transaction cell of the transaction unit selected to constitute the shifted stop;
- a third phase consists of gridding the neutralisation cell of an available unit located in the zone representing the balance, that is, in the portion of the memory located between its beginning and the new stop created. This makes

it possible to compensate for the shifting of the stop and to maintain a balance equivalent to what it should have been;

- a fourth phase consists of gridding the transaction cell corresponding to the neutralisation cell gridded in the third phase, so that the transaction unit which was previously available in the balance zone is totally neutralised, in order to simplify subsequent transactions;
- the fifth phase consists of neutralising the previous stop, by modifying the state of its neutralisation element.

It can happen that in implementing this method the transaction cell corresponding to the neutralisation cell modified to compensate for the shifting of the new stop cannot be modified in turn. It follows that, where for example the initial state of the cells is the logic state "0", the transaction unit available in the balance zone, the neutralisation cell of which has been modified, then has the following configuration: transaction cell in the logic state "0" and neutralisation cell in the logic state "1".

Now, the operation of the "EXCLUSIVE OR" allowing the stop to be detected (which, it will be recalled, has the following configuration: transaction cell in the logic state "1" and neutralisation cell in the logic state "0") as stated above, would lead the memory management device to consider that there is a difference between the transaction element and the corresponding neutralisation element, such that it could consider that this difference comes from the presence of a stop. However, in the precise search for the rank of the stop among these elements, the system would detect that the result of the comparison between the two elements is due to the fact that this configuration "0, 1" exists, which must be considered different from the configuration "1, 0" that actually indicates the presence of a stop.

Therefore, to summarise, when the comparison between an element in the transaction series and its corresponding one in the neutralisation series makes it possible to detect a difference, this may be due to the fact that the stop is present in these elements, or else that there is a transaction unit, the neutralisation cell of

which has been modified to compensate for the creation of a shifted stop, and where it has been impossible to modify the state of the corresponding transaction cell. At the time of the search for the pair of cells that led to such a result in the comparison, it should be found out whether it is the transaction cell that has been modified, considering, in this case, that a stop is involved or whether it is merely the neutralisation cell that has been modified, and a search should therefore be made elsewhere to find the stop.

Figures 15 to 19 illustrate the method described, applied to the impossibility of creating a new stop in the desired location at the time of a debit operation.

Figure 15 illustrates the state of the memory before this operation. The previous stop B6 is constituted, in the example, by the transaction unit located in the eighth rank of the elements with the addresses T3 and N3. This relates to the stop positioned in the illustration in Figure 12. Furthermore, the fourth cells of these elements with the addresses T3 and N3 are modified in comparison with their original state, constituting a neutralised transaction unit (stop B3). The desired debit operation involves seven units, such that the new stop BN should be created on the eighth transaction unit, constituted by the eighth-ranking cells of the elements with the addresses T2 and N2. After the management system associated with the memory has detected the impossibility of gridding the transaction cell which should have been gridded, it searches for the immediately available transaction unit located between the unit at which the new stop should have been created and the old stop in the specific case of a debit. In this particular case, this available unit is constituted by the first-rank cells of the elements with the addresses T3 and N3. The management system therefore modifies the state of the first-rank cell of the transaction element with the address T3, so as to constitute the new stop BR, as illustrated by Figure 16.

Next, the management system searches for an available unit UD located in the balance zone, that is, in the example illustrated, the zone constituted by the elements with the addresses T1, N1, T2, N2, then modifies the state of the neutralisation cell of one of these available elements. In order to simplify

processing, at the time of a debit operation, the system is preferably arranged so as to modify the state of the first available unit UD encountered when reading from the beginning of the zone. In this particular case, the first available unit from the beginning of the zone is constituted by the first-rank cells of the elements with the addresses T1 and N1, such that, in the figure illustrated, it is the first neutralisation cell of the memory zone allocated to the transactions that is modified.

Figure 18 illustrates the next modification, which involves the transaction cell corresponding to the neutralisation cell modified in the previous phase, that is, in the case illustrated, the first transaction cell encountered in reading from the series of transaction elements.

Finally, after this operation, the management system associated with the memory neutralises the previous stop B6, by modifying the state of its neutralisation cell. This is illustrated by Figure 19.

From consulting these different figures, it will be noted that the balance remaining after these various operations is identical to what it should have been if the transaction had been successful from the start, that is, if it had been possible to constitute the stop at the desired location. On the other hand, the artifice chosen to compensate for this impossibility of creating the stop at the desired location simply leads to a diminution in the accreditive power, which has absolutely no importance in making accounting entries for transactions.

To generalise, it will be seen that the impossibility of producing the stop corresponding to a debit of d units leads to the production of a consumption of $d - 1$ units then to the neutralisation of a cell in the balance zone.

In parallel, the impossibility of placing a new stop, in a credit operation of c units, will lead to the constitution of the new stop at a position corresponding to a credit of $c + 1$ units, then the neutralisation of a transaction unit left in the balance zone, in order to produce the compensation, then the neutralisation of the previous stop.

In this particular case of credit, the unit neutralised for compensation is chosen from among the available transaction units between the previous stop and the new stop. The previous stop is indeed located between the start of the zone and the new stop, so that the same is true for the unit selected in order to carry out the compensation.

This artifice has the aim of preventing a loss from the balance in the event that it should prove impossible to neutralise the previous stop, which would lead to the credit operation being refused, as explained above.

Now, after the refusal of a credit operation, the balance has to be the same as before the attempt.

If a transaction unit were neutralised, for compensation, between the start of the zone and the old stop then, in such a case where it is impossible to neutralise the previous stop, followed by the refusal of the transaction, a reduction in the balance would appear, owing to the neutralisation of the compensation unit, which reduction would be prejudicial to the user of the device.

As a variant in the particular case of credit attempts, it is provided that the neutralisation of a transaction unit, corresponding to a shift owing to the impossibility of positioning the new stop at the desired location, is carried out after there has been a successful attempt to neutralise the previous stop. If it is impossible to neutralise the previous stop, then the credit operation is refused. On the other hand, if it is possible to neutralise the previous stop, then it is possible to choose any available transaction unit, located between the beginning of the zone and the new stop, in order to neutralise it to carry out the compensation owing to the shifting of the new stop.

This variant has the advantage that, on the one hand, no useless operation is performed, since the neutralisation of available units to carry out compensation is performed only if it has been possible to neutralise the previous stop, after the creation of the new stop and, on the other hand, this significantly simplifies the production of a device for implementing the method of the invention, since it is not

necessary to take account of the location of the old stop in order to choose an available transaction unit so as to neutralise it for compensation.

Of course, it is also possible to choose this variant in the case of a dysfunction when an attempt is made to record a new stop at the time of a debit, i.e. the attempt to neutralise the previous stop is made before the neutralisation of a transaction unit available in the balance zone, in order to carry out compensation.

Preferably, when this second variant is used to remedy the dysfunction at the time of credit attempts, then it is also chosen to remedy the dysfunction during debit attempts, in order to simplify the implementation processes in the various cases in point.

Naturally, the sign of the operations depends on the convention that has been chosen at the start, which consists of referring constantly to the start of the zone, and of considering that the ascending order of cells starts from the first cells of the elements with the addresses T1 and A1, ending at the last cells of the elements with the addresses T4 and N4 in the example illustrated. The positive direction is therefore the direction in which the zone is read, starting from its beginning. Clearly, this could be modified without any effect on the results of the transactions.

Cases can also occur, at the time of a credit or debit, where it would be impossible to create the shifted stop in the selected location either because, where it proves impossible to create a stop following a credit operation, the shifted position would exceed the limits of the zone: in this case the credit operation will be refused; or else because after an order to shift when it has proved impossible to modify the state of a transaction cell, it additionally becomes impossible also to modify the state of the transaction cell corresponding to the transaction unit chosen to constitute the shifted stop, for a reason inherent to the memory.

In this case, a further shift order can be given until an available transaction unit is found, having a transaction cell that can be modified. However, in such a case, account should be taken of the different shift orders given successively and, to

compensate for them, it will be necessary to neutralise in the balance zone as many transaction units as there have been shifts relative to the position that should actually have been occupied by the new stop, by implementing one or other of the two variants presented above.

Also, as an addition, it may be considered that after a given number of successive shift orders, the credit or debit operation is refused since there is too great a number of unmodifiable cells in the memory.

In one embodiment, it may for example be considered that three successive unfruitful shifts lead to the refusal of the desired debit or credit operation.

Moreover, if there are not sufficient available cells to produce the shifted stop and/or the compensations, then the transaction is refused.

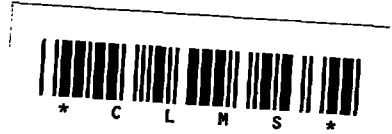
In conclusion, the invention is particularly advantageous since it uses the same functions whether for a transaction involving a debit, or a transaction involving a credit. The systematic neutralisation of the transaction units that have served to constitute the previous stop, when a new stop is created following a transaction, allows considerable time-saving on processing, particularly for credit operations, since this avoids having to reread the whole memory in order to neutralise the transaction units that have been used since the last credit operation.

Furthermore, in addition to the remarkable performance of a device implementing the method of the invention, another advantage of the invention lies in the fact that the user, or the processing system, no longer needs to know the internal configuration of the memory reserved for the transactions, as was the case with the systems and methods of the prior art which required perfect knowledge of the content of the memory, particularly at the time of neutralisation operations. Here, all the operations are totally transparent and the risks of dysfunction or error are fully taken into account.

The search for the element containing the old stop, in order to determine the starting point for counting the units corresponding to the transaction to be performed, allows considerable time-saving since the memory is not read cell by cell, given that cell-by-cell reading is carried out only in the pair of elements in which the stop is detected.

Finally, any dysfunctions that may arise when the method is implemented are taken into account, while the prior art provides nothing in this respect, such that a system implementing the method of the invention is particularly safe and reliable which, especially in the case of use in an electronic wallet, avoids the loss of money for the holder of a memory-type card which would be used in this way, or for the money provider.

A system implementing the method of the invention could be built around a microprocessor with the usual processing format, for example eight bits, and the memory used for managing the homogeneous units could be an EPROM-type memory, that is, one where the content of one or other of the cells can be modified once only by application of an electrical signal.



CLAIMS

1. A method for managing an electronic memory representing predetermined homogeneous units, consisting of writing into memory a stop indicating the balance at the end of a transaction bearing on said units, and of dividing the memory into two series (Z1, Z2) of cells, such that each cell of the first series is paired with a given cell of the second series, each pair of cells thus constituted forming one transaction unit, in which method a transaction is taken into account by creating a new stop, the location of which is defined from the position of the previous stop by modifying the state of one cell in one of the series, characterised in that it additionally consists of:
 - dividing each series of cells into elements (E11, E12, ... E1n) of the same format, containing a non-unitary number (k) of cells (C1, C2, ... Ck), each element in the first series being paired with an element of the second such that each cell of an element in the first series is paired with a cell of the corresponding element in the first series;
 - using said stop to make accounting entries for a debit and a credit at the same time, this stop dividing said series of cells (Z1, Z2) into two zones, namely one zone representing a balance containing the available transaction units and one zone representing an accreditive power containing the transaction units that it is possible to use to increase the balance, an accounting entry being made for a debit of (d) units by writing the new stop at the (d)th available transaction unit counted from the previous stop in the balance zone, whereas an accounting entry is made for a credit of (c) units by writing the new stop at the (c)th available transaction unit counted from the previous stop in the accreditive power zone;
 - neutralising the previous stop at the time of each transaction by modifying the state of the cell unmodified at the time of its creation; and



- identifying the position of the previous stop, starting from which that of the new stop is calculated, by first seeking the pair of elements in which this previous stop is located by using a logic operation, applied to different pairs of elements in the first and second series, and suitable for producing a particular result in the case of said sought pair of elements, then by comparing successively, in this pair of elements, the two cells of each transaction unit until said previous stop is detected.
2. A method according to Claim 1, characterised in that the balance of units is constituted by the number of available transaction units, that is, the pairs of cells of which the two cells are in their original state, and which are located between a first end of the zone allocated to the transactions and the stop, and in that the accreditive power, that is, the number of transaction units that it is possible to use to increase the balance, is constituted by the number of available transaction units minus one located between the stop and the second end of the zone.
 3. A method according to Claim 1 or Claim 2, characterised in that, to determine the position of the new stop and to create the latter at the time of the transaction, an accounting entry is made for a number of unmodified cells in the second series (Z2), that is, cells corresponding to the available units, from the position of the previous stop, in the zone representing the balance in the case of a debit operation, or in the zone representing the accreditive power in the case of a credit operation, and the modified cells of the second series, that is, those corresponding to cancelled transaction units, are ignored, and the state of the cell in the first series paired with the last cell counted in the second series is modified in order to create the new stop.
 4. A method according to Claim 3, characterised in that, after the creation of a new stop at the time of an attempt at a debit or credit operation, whenever it is impossible for some reason internal to the memory to modify the state of the cell of the previous stop located in the second series in order to cancel it, which would lead to having two transaction units with the configuration of a stop in



the memory, then it is assumed that among these two elements, the previous stop constitutes a new limit to the accreditive power.

5. A method according to Claim 4, characterised in that whenever it is impossible, for reasons internal to the memory, to modify the state of the cell of the first series corresponding to the new stop to be created, a search is made, between the position that this new stop should have occupied and the limit of the accreditive power, in the case of a credit, or between the position that the new stop should have occupied and the previous stop, in the case of a debit, for the first available transaction unit of which it is possible to modify the state of the cell that it includes in the first series (Z1), and the state of said cell located in the first series is modified in such a manner as to constitute the new stop, and in order to compensate for the shifting occasioned by this dysfunction, intervention is made upon a number of available transaction units in the portion of the memory representing the balance, said number corresponding to the number of units by which the new stop has been shifted in comparison with the position that it should have occupied, on the one hand by modifying the state of the cells located in the second series of said available transaction units, and on the other hand by attempting, as soon as possible after having modified the state of a cell located in the second series of each of these available transaction units, to modify the state of the corresponding cell located in the first series, in such a manner as to attempt to neutralise each of said transaction units, and in that, after having performed this compensation, an attempt is made to neutralise the previous stop by modifying the state of this cell located in the second series.
6. A method according to Claim 5, characterised in that in order to compensate for the shifting caused by the creation of a new stop at the time of an attempt at credit, an intervention is made upon a number of transaction units available in the portion of the memory representing the balance, included between the previous stop and the new stop.



7. A method according to Claim 4, characterised in that whenever it is impossible, for reasons internal to the memory, to modify the state of the cell in the first series corresponding to the new stop to be created, a search is made, between the position that this new stop should have occupied and the limit of the accreditive power in the case of a credit, or between the position that the new stop should have occupied and the previous stop in the case of a debit, for the first available transaction unit of which it is possible to modify the state of the cell that it includes in the first series (Z1), and the state of said cell located in the first series is modified in such a manner as to constitute the new stop, an attempt is made to neutralise the previous stop by modifying the state of its cell located in the second series, and in order to compensate for the shifting occasioned by this dysfunction, an intervention is made upon a number of available transaction units in the portion of memory representing the balance, said number corresponding to the number of units by which the new stop has been shifted in comparison with the position that it should have occupied, on the one hand by modifying the state of the cells located in the second series of said available transaction units, and on the other hand by attempting as soon as possible after having modified the state of a cell located in the second series of each of these available transaction units, to modify the state of the corresponding cell located in the first series, in such a manner as to neutralise each of said transaction units.
8. A system for management of an electronic memory representing predetermined homogeneous units, including a microprocessor and an electrically programmable electronic memory, associated with this microprocessor, the system including means for writing into memory a stop indicating the balance at the end of a transaction involving said units and dividing the memory into two series (Z1, Z2) of cells, such that each cell in the first series is paired with a given cell in the second series, each pair of cells thus constituted forming one transaction unit, in which system a transaction is taken into account by creating a new stop, the location of which is defined starting from the position of the previous stop, by modifying the state of one cell in one of the series, and by leaving the corresponding cell in the other



series in its initial state, characterised in that said memory is arranged such that each series of cells is divided into elements (E11, E12, ..., E1n) of the same format, corresponding to the processing format of the microprocessor, containing a non-unitary number (k) of cells (C1, C2, ... Ck), each element of the first series being paired with an element of the second such that each cell of an element in the first series is paired with a cell of the corresponding element in the second series, and in that the management system further comprises:

- means for using said stop to make accounting entries for a debit and a credit at the same time, this stop dividing said series of cells (Z1, Z2) into two zones, namely one zone representing a balance containing the available transaction units and one zone representing an accreditive power containing the transaction units that it is possible to use to increase the balance, an accounting entry being made for a debit of (d) units by writing the new stop on the (d)th available transaction unit counted from the previous stop in the balance zone, whereas an accounting entry is made for a credit of (c) units by writing the new stop on the (c)th available transaction unit counted from the previous stop in the accreditive power zone;
- means for neutralising the previous stop at the time of each transaction by modifying the state of the cell unmodified at the time of its creation;
- means for identifying the position of the previous stop, starting from which that of the new stop is calculated, by first seeking the pair of elements in which this previous stop is located by using a logic operation applied to different pairs of elements in the first and second series and suitable for producing a particular result in the case of said sought pair of elements, then by comprising successively, in this pair of elements, the two cells of each transaction unit until said previous stop is detected.



9. A system according to Claim 8, characterised in that the microprocessor and the memory are incorporated in a portable object.