WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first transistor on a substrate; and

a second transistor on the substrate,

wherein each of the first and second transistors includes,

a plurality of semiconductor patterns vertically stacked on the substrate and vertically spaced apart from each other, and

a gate dielectric pattern and a work function pattern filling a space between the semiconductor patterns, wherein

the work function pattern of the first transistor includes a first work function metal layer,

the work function pattern of the second transistor includes the first work function metal layer and a second work function metal layer,

the first work function metal layer of each of the first and second transistors has a work function greater than that of the second work function metal layer, and

the first transistor has a threshold voltage less than that of the second transistor.

2. The device of claim 1, wherein the work function pattern of each of the first and second transistors completely fills the space between the semiconductor patterns.

3. The device of claim 1, wherein

each of the first and second transistors further comprises an electrode pattern on the work function pattern, and

the electrode pattern has resistance less than that of the work function pattern and does not fill the space.

4. The device of claim 1, wherein

the first work function metal layer of each of the first and second transistors comprises a metal nitride layer, and

the second work function metal layer comprises a metal nitride layer doped with an element from the group including silicon and aluminum.

5. The device of claim 4, wherein a silicon or aluminum doping concentration of the second work function metal layer is in a range from about 10 at% to about 30 at%.

6. The device of claim 1, wherein

the first transistor further includes a work function control liner between the work function pattern and the semiconductor patterns, and

the work function control liner is configured to generate a dipole that changes a threshold voltage of the first transistor.

7. The device of claim 1, further comprising:

a third transistor on the substrate; and

a fourth transistor on the substrate,

wherein each of the third and fourth transistors includes

a plurality of semiconductor patterns vertically stacked on the substrate and vertically spaced apart from each other, and

a gate dielectric pattern and a work function pattern that fill a space between the semiconductor patterns,

wherein the work function pattern of the third transistor includes the first work function metal layer and a third work function metal layer,

the work function pattern of the fourth transistor includes the first work function metal layer, the second work function metal layer, and the third work function metal layer,

the third work function metal layer of each of the third and fourth transistors has a work function less than that of the second work function metal layer of the fourth transistor,

the first and second transistors are PMOSFETs, and

the third and fourth transistors are NMOSFETs.

8. The device of claim 7, wherein the second work function metal layer of the second transistor has a thickness greater than that of the second work function metal layer of the fourth transistor.

9. The device of claim 1, wherein the work function pattern of each of the first and second transistors surrounds a top surface, a bottom surface, and sidewalls of the semiconductor patterns.

10. The device of claim 1, wherein

each of the first and second transistors further includes a pair of source/drain patterns, and

the plurality of semiconductor patterns vertically stacked are between the pair of source/drain patterns.

11. A semiconductor device, comprising:

a first transistor on a substrate; and

a second transistor on the substrate,

wherein each of the first and second transistors includes,

a plurality of semiconductor patterns vertically stacked on the substrate and vertically spaced apart from each other, and

a gate dielectric pattern and a work function pattern that fill a space between the semiconductor patterns,

wherein the space of the first transistor has the same size as that of the space of the second transistor,

the work function pattern of the first transistor comprises a first work function metal layer,

the work function pattern of the second transistor comprises the first work function metal layer and a second work function metal layer, and

the first transistor has a threshold voltage different from that of the second transistor.

12. The device of claim 11, wherein the work function pattern in the space of the first transistor has a thickness the same as that of the work function pattern in the space of the second transistor.

13. The device of claim 11, wherein

the first work function metal layer of each of the first and second transistors comprises a metal nitride layer, and

the second work function metal layer comprises a metal nitride layer doped with an element from the group including silicon and aluminum.

14. The device of claim 11, wherein

the first and second transistors are PMOSFETs,

the first work function metal layer of each of the first and second transistors has a work function greater than that of the second work function metal layer, and

the second work function metal layer of the second transistor has a thickness greater than that of the first work function metal layer of the second transistor.

15. The device of claim 11, wherein

the first and second transistors are PMOSFETs,

the first work function metal layer of each of the first and second transistors has a work function greater than that of the second work function metal layer, and

the second work function metal layer of the second transistor has a thickness less than that of the first work function metal layer of the second transistor.

16. A method of manufacturing a semiconductor device, the method comprising:

forming sacrificial layers and semiconductor layers alternately and repeatedly stacked on a substrate;

forming sacrificial gate patterns crossing over the sacrificial layers and the semiconductor layers and extending in one direction;

removing the sacrificial gate patterns to form a first trench and a second trench that expose the semiconductor layers and the sacrificial layers;

selectively removing the sacrificial layers exposed to the first and second trenches;

forming a first work function pattern that fills a first space between the semiconductor layers in the first trench; and

forming a second work function pattern that fills a second space between the semiconductor layers in the second trench,

wherein

the first work function pattern comprises a first work function metal layer,

the second work function pattern comprises the first work function metal layer and a second work function metal layer,

the first space and the second space have the same size as each other, and

the first work function pattern and the second work function pattern have different work functions from each other.

17. The method of claim 16, before forming the first work function pattern,

further comprising forming a work function control liner that partially fills the first space,

wherein the work function control liner is configured to generate a dipole that changes the work function of the first work function pattern.

18. The method of claim 16, before forming the first and second work function patterns, further comprising forming a gate dielectric layer that partially fills the first and second spaces.

19. The method of claim 16, wherein

the first space includes a region where the sacrificial layer exposed to the first trench is removed, and

the second space includes a region where the sacrificial layer exposed to the second trench is removed.

20. The method of claim 16, further comprising:

forming a first mask pattern that covers the second trench and exposes the first trench; and

forming a second mask pattern that covers the first trench and exposes the second trench,

wherein the first and second work function patterns are formed using the first and second mask patterns, respectively.