CLAIMS

1. A semiconductor structure, comprising:

a first active area;

a first gate located on the first active area, the first active area and the first gate being configured to form a first transistor;

a second active area, the second active area and the first active area being arranged along a first direction, the second active area and the first active area being independent from each other; and

a second gate located on the second active area, the second active area and the second gate being configured to form a second transistor,

wherein the first gate and the second gate are both L-shaped and non-axisymmetric; the shape of the overlapping region between the first active area and the first gate is same to that of the overlapping region between the second active area and the second gate, and the shape of the overlapping region is approximately L-shaped, sizes of the first transistor and the second transistor are same, and a deviation between an electrical parameter of the first transistor and an electrical parameter of the second transistor is below a preset threshold, and the first transistor and the second transistor belong to a cross coupling amplifying unit.

2. The semiconductor structure according to claim 1, wherein shapes of the first gate and the second gate are same;

in the first direction, an upper edge of the first gate is higher than an upper edge of the first active area, and a lower edge of the first gate is lower than a lower edge of the first active area; an upper edge of the second gate is higher than an upper edge of the second active area, and a lower edge of the second gate is lower than a lower edge

of the second active area.

3. The semiconductor structure according to claim 2, wherein,

in the first direction, a distance between the upper edge of the first active area and the upper edge of the first gate is a first value; and a distance between the upper edge of the second active area and the upper edge of the second gate is a second value, wherein the first value and the second value are same; and

a distance between the lower edge of the first active area and the lower edge of the first gate is a third value, and a distance between the lower edge of the second active area and the lower edge of the second gate is a fourth value, wherein the third value and the fourth value are same.

4. The semiconductor structure according to claim 1, further comprising:

a first contact region located in the first active area;

a second contact region located in the first active area, the first contact region, the first gate and the second contact region being arranged along a second direction in sequence;

a third contact region located in the second active area; and

a fourth contact region located in the second active area, the third contact region, the second gate and the fourth contact region being arranged along the second direction in sequence.

5. The semiconductor structure according to claim 4, wherein,

in the second direction, a distance between the first contact region and the first

gate is a fifth value, and a distance between the third contact region and the second gate is a sixth value, and the fifth value and the sixth value are same; a distance between the second contact region and the first gate is a seventh value, and a distance between the fourth contact region and the second gate is an eighth value, and the seventh value and the eighth value are same.

6. The semiconductor structure according to claim 4, wherein,

in the first direction, an upper edge of the second contact region is flush with an upper edge of the first contact region, and a lower edge the second contact region is lower than a lower edge of the first contact region; a lower edge of the fourth contact region is flush with a lower edge of the third contact region, and an upper edge of the fourth contact region is higher than an upper edge of the third contact region.

7. The semiconductor structure according to claim 4, wherein,

in the first direction, an upper edge of the second contact region is higher than an upper edge of the first contact region, and a lower edge of the second contact region is lower than a lower edge of the first contact region; an upper edge of the fourth contact region is higher than an upper edge of the third contact region, and a lower edge of the fourth contact region is lower than a lower edge of the third contact region.

8. The semiconductor structure according to claim 7, wherein,

in the first direction, a distance between the upper edge of the first contact region and the upper edge of the second contact region is a ninth value, and a distance between the upper edge of the third contact region and the upper edge of the fourth contact region is a tenth value, wherein the ninth value and the tenth value are same; and

a distance between the lower edge of the first contact region and the lower edge of the second contact region is an eleventh value, and a distance between the lower edge of the third contact region and the lower edge of the fourth contact region is a twelfth value, wherein the eleventh value and the twelfth value are same.

9. The semiconductor structure according to claim 8, wherein,

the ninth value, the tenth value, the eleventh value and the twelfth value are same.

10. The semiconductor structure according to claim 4, further comprising:

a third gate located on the first active area and disposed at a side of the second contact region away from the first gate, the first active area and the third gate being configured to form a third transistor; and

a fourth gate located on the second active area and disposed at a side of the fourth contact region away from the second gate, the second active area and the fourth gate being configured to form a fourth transistor,

wherein the third transistor and the fourth transistor belong to another cross coupling amplifying unit.

11. The semiconductor structure according to claim 10, further comprising:

a five contact region located in the first active area and disposed at a side of the third gate away from the second contact region; and

a sixth contact region located in the second active area and disposed at a side of

the fourth gate away from the fourth contact region.

12. The semiconductor structure according to claim 11, wherein,

shapes of the first contact region and the fifth contact region are same, and shapes of the third contact region and the sixth contact region are same;

in the first direction, central points of the first contact region and the fifth contact region are located at a same position, and central points of the third contact region and the sixth contact region are located at a same position; and

the first gate and the third gate are centrosymmetric with respect to the second contact region; and the second gate and the fourth gate are centrosymmetric with respect to the fourth contact region.

13. The semiconductor structure according to claim 12, wherein the first active area, the second active area, the first gate to the fourth gate, the first contact region to the sixth contact region together constitute a repeat unit, and a plurality of the repeat units are arranged along the second direction;

a distance between the first gate and the third gate in a same repeat unit is a thirteenth value, and a distance between the first gate in a repeat unit and the third gate in an adjacent repeat unit is a fourteenth value; and

a distance between the second gate and the fourth gate in a same repeat unit is a fifteenth value, and a distance between the second gate in a repeat unit and the fourth gate in an adjacent repeat unit is a sixteenth value,

wherein the thirteenth value, the fourteenth value, the fifteenth value and the sixteenth value are same.

14. The semiconductor structure according to claim 12, wherein the first gate is provided with a seventh contact region, the second gate is provided with an eighth contact region, the third gate is provided with a ninth contact region, and the fourth gate is provided with a tenth contact region, wherein

the seventh contact region and the tenth contact region are centrosymmetric, and the eighth contact region and the ninth contact region are centrosymmetric.

15. A memory, comprising the semiconductor structure according to any one of claims 1 to 14.