A (110) oriented silicon substrate and a bonded pair of substrates comprising said (110) oriented silicon substrate

The present invention relates to method of fabricating a (110) oriented silicon substrate and to a method of fabricating a bonded pair of substrates comprising such a (110) oriented silicon substrate. The invention further relates to a silicon substrate with (110) orientation and to a bonded pair of silicon substrates comprising a first silicon substrate with (100) orientation and a second silicon substrate with (110) orientation.

Since it is known that hole mobility is more than doubled on (110) silicon substrates compared with conventional (100) substrates, there is an increasing interest in manufacturing of high quality silicon substrates with (110) orientation. However, electron mobility is the highest on (100) substrates. Based on this knowledge, a new technology to fabricate high performance CMOS devices has been developed using hybrid silicon substrates with different crystal orientations, wherein pFETs are formed on a (110) oriented surface and nFETs are formed on a (100) surface and the different substrates are bonded.

For the manufacturing of such hybrid substrates with high quality, in particular the surface quality of the bonded substrates plays an important role. It is known from SOI substrates that the surface quality of the thin silicon layer on top of SOI substrates can suffer from some defects like HF-defects due to the presence of crystal defects being already present in the original CZ silicon material such as Crystal Oriented Pits (COP) and oxygen precipitations.

Therefore, some wafer manufacturers developed special processes to fabricate (100) oriented silicon substrates with very low densities of COPs resulting in the effect that almost no defects such HF-defects on final hybrid substrates were observed. It was further tried to form similarly bulk (110) silicon substrates without such defects, but these technologies are very expensive and show a very low yield due to low crystal growth. Beyond it, (110) oriented silicon is known to become easily rough and having problems in surface reconstruction because heat treatment of (110) substrates reveals low energy planes.

It is therefore the object of the present invention to provide an (110) oriented silicon substrate as well as a method of fabricating such a (110) oriented silicon substrate and

to provide a bonded pair of substrates comprising a (110) oriented silicon substrate as well as a method of fabricating such a bonded pair of substrates with a high efficiency wherein the formed (110) substrate has at least near and at its surface virtually no defects.

The object is solved by a method of fabricating a silicon substrate with (110) orientation, comprising the steps of providing a basic silicon substrate with (110) orientation, said basic silicon substrate having a roughness being equal or less than 0.15 nm RMS in a 2x2 μm^2 or a 10x10 μm^2 scan, and depositing epitaxially a silicon layer with (110) orientation on the basic silicon substrate at a pressure between about 40 Torr and about 120 Torr, preferably 80 Torr, and at a temperature between about 1000°C and about 1200°C and using trichlorosilane or dichlorosilane as silicon precursor gas.

Surprisingly, the low pressure during the deposition of the epitaxial silicon layer leads in comparison to normally applied processes under atmospheric pressure to a decrease of the number of surface defects. Thus, the inventive method can be applied on bulk (110) basic silicon wafers having initially an increased number of surface defects, wherein after the formation of the (110) silicon layer on top of said substrate the surface quality is much better than before. In doing so, the surface quality of the substrate can be enhanced without the necessity to provide initially (110) substrate with a high crystal quality with time and cost intensive crystal growth processes.

To the contrary, the inventive method leads in a relatively fast and low cost way to the effect that the produced (110) substrates have at least at and near the surface virtually no defects. The epitaxial (110) silicon layer covers effectively all defects, in particular the COPs, of the underlying (110) basic silicon substrate without degrading the surface roughness of the resulting (110) silicon substrate.

Although it is known from the prior art, that the formation of epitaxial (110) silicon layers at temperatures between 1000°C and 1200°C leads to substrates with high haze, it is possible with the present invention by means of the application of the low pressure to result in substrates with a very low haze.

According to a favorable embodiment of the present invention, a heat treatment at a temperature between about 1000°C and about 1200°C is applied in a H_2 containing environment on the basic silicon substrate before depositing the silicon layer. This bake

treatment before the deposition of the epitaxial (110) silicon layer helps to form good conditions for silicon deposition on the surface of the basic silicon substrate. In other variants of the present invention, the temperature can be modified before the epitaxial growth.

In a particularly suitable example of the invention is the pressure during the deposition of the silicon layer (2) from about 40 Torr to about 120 Torr, preferably 80 Torr. Processes performed at this pressure showed especially well surface characteristics of the produced substrates. For instance, it could be shown that the number of defects on an initial basic (110) silicon wafer of more than 1000 COPs on the surface could be decreased to a number of less than 10 defects with a size of equal or more than 0.13 µm.

It is furthermore advantageous if the silicon layer is deposited up to a thickness of at least 1 µm. This thickness is especially effective if all defects with a size of more than 0.13 µm on the surface of the produced (110) substrate shall be removed.

In a beneficial embodiment of the invention, the silicon layer is deposited with a growth rate of about 0.25 µm/min to about 1.0 µm/min at a temperature up to 1100°C with dichlorosilane (DCS) as precursor or with a growth rate of about 3.0 µm/min using trichlorosilane (TCS) as precursor at a temperature up to 1200°C . Astonishingly, despite of the relatively high growth rate which normally leads to higher roughness due to the phenomenon of step bunching, the formed (110) silicon substrate has a very low surface roughness which is comparable with the original roughness of the basic (110) silicon substrate before layer deposition and can be, for instance, about 0.1 nm RMS in a 2x2 μm^2 as well as in a 10x10 μm^2 scan.

In an appropriate example of the invention, the silicon layer is deposited in such a way that it contains no defects with a size of more than 0.13 µm, measured by light scattering tools.

The object is moreover solved by a method of fabricating a bonded pair of silicon substrates comprising a first silicon substrate with (100) orientation and a second silicon substrate with (110) orientation, the method comprising the steps of providing the first silicon substrate, providing a basic silicon substrate with (110) orientation, said basic silicon substrate having a roughness being equal or less than 0.15 nm RMS in a 2x2 μm^2

or a 10x10 μm^2 scan, depositing epitaxially a silicon layer with (110) orientation on the basic silicon substrate at a pressure between about 40 Torr and about 120 Torr, preferably 80 Torr, and at a temperature between about 1000°C and about 1200°C and using trichlorosilane or dichlorosilane as silicon precursor gas to form the second silicon substrate, and bonding the first silicon substrate with the second silicon substrate.

With this inventive method, a bonded pair of silicon substrates with different orientations can be provided wherein in particular the (110) silicon substrate has very good surface characteristics which are especially suited to form at this surface microelectronic devices with high performance.

The above mentioned method of fabricating the bonded pair of substrates can be modified in accordance with the particular embodiments of the present invention for fabricating the (110) silicon substrate as explained above.

Moreover, the object of the invention is solved by a silicon substrate with (110) orientation, comprising a basic silicon substrate with (110) orientation, said basic silicon substrate having a roughness being equal or less than 0.15 nm RMS in a 2x2 μm^2 or a 10x10 μm^2 scan, and an epitaxial silicon layer with (110) orientation grown on the basic silicon substrate.

It is especially advantageous if said epitaxial silicon layer contains no defects with a size of more than 0.13 µm measured by light scattering tools.

Furthermore, the object of the invention is solved by a bonded pair of silicon substrates comprising a first silicon substrate with (100) orientation and a second silicon substrate with (110) orientation, wherein the second silicon substrate comprises a basic silicon substrate with (110) orientation, said basic silicon substrate having a roughness being equal or less than 0.15 nm RMS in a 2x2 μm^2 or a 10x10 μm^2 scan, and an epitaxial silicon layer with (110) orientation grown on the basic silicon substrate.

In a beneficial variant of the invention, said epitaxial silicon layer contains no defects with a size of more than 0.13 µm, as measured light scattering tools.

In the following, favorable embodiments of the invention and their advantages are exemplified by means of the figures wherein

Figure 1 schematically shows a basic (110) silicon substrate,

Figure 2 schematically shows the substrate of Figure 1 after the deposition of an epitaxial (110) silicon layer,

Figure 3 shows an example of a possible sequence of steps for fabricating a (110) silicon substrate as shown in Figure 2 according to the method of the present invention,

Figure 4 schematically shows a bonded pair of substrates comprising a (110) oriented silicon substrate and a (100) oriented silicon substrate, produced by a method according to the present invention, and

Figure 5 shows an example of a possible sequence of steps for fabricating a bonded pair of substrates comprising a (100) substrate and a (110) substrate, as shown in Figure 4, in accordance with the present invention.

Figure 1 schematically shows a basic silicon CZ bulk substrate 1 with a (110) crystal orientation. The silicon substrate 1 has on its surface 4 a roughness which is equal or less than 0.15 nm RMS in a 2x2 μm^2 or a 10x10 μm^2 scan and has a defect number of more than 1000 COPs at its surface 4, as measured by light scattering tools like for example SP1 tool developed by KLA Tencor.

Figure 2 schematically shows a (110) silicon substrate 12 consisting of the basic silicon substrate 1 of Figure 1 and an epitaxial (110) silicon layer 2 formed on the surface 4 of the basic (110) silicon substrate 1.

Figure 3 shows an example of a possible sequence of steps for fabricating the (110) silicon substrate 12 of Figure 2 according to the method of the present invention.

With reference to step 101, (110) oriented silicon wafers such as the substrate 1 of Figure 1are loaded in a process chamber.

Then, in the process chamber a pressure p of about 20 to about 200 Torr, preferably of about 100 Torr, is set in step 102.

According to step 103, an appropriate temperature T of about 1000°C to about 1200°C is adjusted in the process chamber.

Thereafter, in step 104, a bake treatment is applied on the wafers at a temperature T of about 1000°C to about 1200°C in an H_2 containing environment. The pressure p as well as the temperature T may be modified during the bake treatment.

In the next step 105, the epitaxial (110) silicon layer 2 is formed on the substrate 1 using trichlorosilane (TCS) or dichlorosilane (DCS) as silicon precursor gas at a pressure p between about 20 Torr and about 200 Torr, preferably about 100 Torr and at a temperature T between about 1000°C and about 1200°C. The process time of the epitaxial deposition is adapted to the flow of the precursor gas in dependence on the desired thickness of the epitaxial layer 2. Preferably, the (110) silicon layer 2 is deposited with a thickness t of at least 1 µm.

The epitaxial layer 2 is preferably grown with a growth rate between 0.25 µm/min and 1.0 µm/min using DCS precursor or even more around 3 µm/min using TCS precursor, wherein the more rapid the growth rate is the more step bunching effects occur leading to a higher roughness.

In the particular example shown, the epitaxial layer 2 is deposited at a pressure p of 80 Torr, at a temperature T of 1080°C, with a growth rate of 1.0 µm/min, a H_2 flow of 40 slm and a DCS flow of 400 sccm.

Referring to step 106, the pressure of the process chamber as well as the temperature are adjusted to unload the wafers.

The (110) silicon layer 2 shows virtually no defects with a size of more than 0.13 µm. Moreover, the roughness at the surface of the resulting (110) silicon substrate is very low.

Figure 4 schematically shows a bonded pair of substrates 10 comprising a first (100) oriented silicon substrate 11 and a second (110) oriented silicon substrate 12, produced by a method according to the present invention. The second (100) oriented silicon

substrate 11 corresponds to the substrate 11 of Figure 2 produced by a method as described with reference to Figure 3.

Figure 5 shows an example of a possible sequence of steps for fabricating the bonded pair of substrates 12 of Figure 4 comprising the first (100) oriented silicon substrate 11 and the second (110) oriented silicon substrate 12, as shown in Figure 4, in accordance with the present invention. The steps for producing the (110) silicon substrate correspond, in general, to steps of Figure 3..

As shown in step 107, the (100) oriented silicon substrate 11 and the (110) oriented silicon substrate 12 are provided.

According to step 108, the (100) oriented silicon substrate 11 and the (110) oriented silicon substrate 12 are bonded together to form the bonded wafer pair 10. One of the substrate could be thinned down, by grinding & etching techniques or implantation and splitting, in order to provide a final layer of one of the material on top of the other substrate.

The bonded wafer pair 10 is a hybrid substrate which can be used to integrate therein complementary metal oxide semiconductor (CMOS) devices. In the (100) oriented silicon substrate 11 n-channel metal oxide semiconductor field effect transistors (nFETs) can be formed because of the high electron mobility of the (100) oriented silicon substrate 11. In particular in the (110) oriented silicon layer 2 of the (110) oriented silicon substrate 12 p-channel MOSFETs can be formed because of the high hole mobility and the nearly defect free crystallinity of said layer 2.

Claims

1. Method of fabricating a silicon substrate (12) with (110) orientation, comprising the steps of
providing a basic silicon substrate (1) with (110) orientation, said basic silicon substrate (1) having a roughness being equal or less than 0.15 nm RMS in a 2x2 μm^2 or a 10x10 μm^2 scan, and
depositing epitaxially a silicon layer (2) with (110) orientation on the basic silicon substrate (1) and at a temperature (T) between 1000°C and 1200°C and using trichlorosilane or dichlorosilane as silicon precursor gas,
characterized in that
the pressure (p) during the deposition of the silicon layer (2) is from 40 Torr to 120 Torr, preferably 80 Torr.

2. Method of claim 1, **characterized in that** a heat treatment at a temperature (T) between about 1000°C and about 1200°C is applied in a H_2 containing environment on the basic silicon substrate (1) before depositing the silicon layer (2).

3. Method of one of the preceding claims, **characterized in that** the silicon layer (2) is deposited up to a thickness (t) of at least 1 µm.

4. Method of one of the preceding claims, **characterized in that** the silicon layer (2) is deposited with a growth rate of 0.25 µm/min to 1.0 µm/min using dichlorosilane as precursor.

5. Method of one of the preceding claims, **characterized in that** the silicon layer (2) is deposited with a growth rate of 3 µm/min using trichlorosilane as precursor.

6. Method of one of the preceding claims, **characterized in that** the silicon layer (2) is deposited in such a way that it contains no defects with a size of more than 0.13 µm, measured by light scattering tools.

7. Method according to one of claim 1 to 6, further comprising the steps of
providing a first silicon substrate (11) with 100 orientation, and

bonding the first silicon substrate (11) with the basic silicon substrate comprising the silicon layer (2) forming a second silicon substrate (12) to fabricate a bonded pair (10) of silicon substrates comprising the fist substrate (11) with (100) orientation and the second silicon substrate (12) with (110) orientation.

8. Silicon substrate (12) with (110) orientation, comprising a basic silicon substrate (1) with (110) orientation, said basic silicon substrate (1) having a roughness being equal or less than 0.15 nm RMS in a 2x2 μm^2 or a 10x10 μm^2 scan, and an epitaxial silicon layer (2) with (110) orientation grown on the basic silicon substrate (1) according to the method to one of claim 1 to 6.

9. Silicon substrates according to claim 8, further comprising a first silicon substrate (11) with (100) orientation and a second silicon substrate (12) with (110) orientation, wherein the second silicon substrate (12) comprises the basic silicon substrate (1) with (110) orientation, and the epitaxial silicon layer (2) with (110) orientation.

10. Silicon substrates of claim 8 or 9 **characterized in that** the epitaxial silicon layer (2) contains no defects with a size of more than 0.13 µm, as measured light scattering tools.