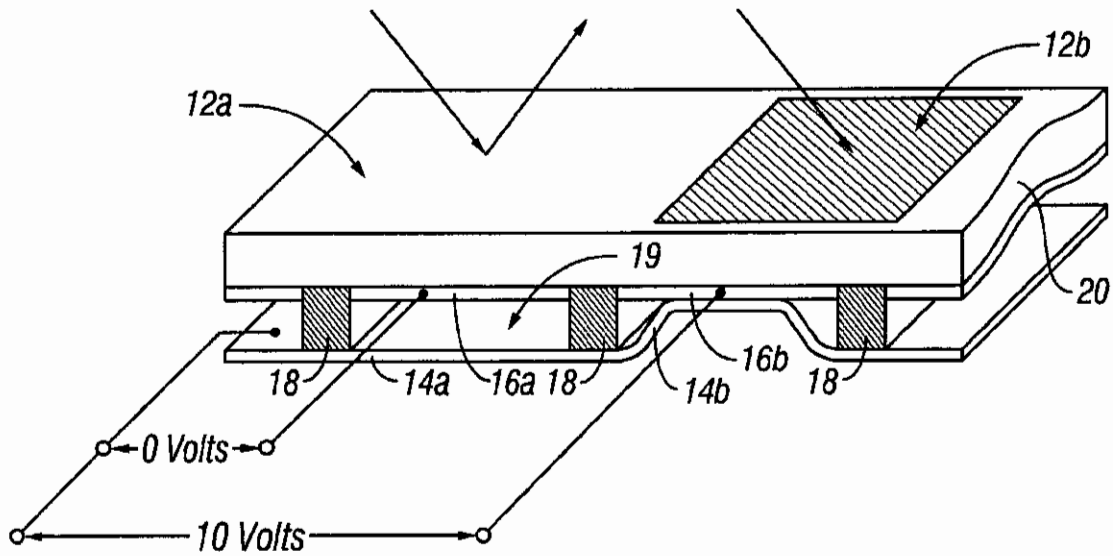

FIG. 1

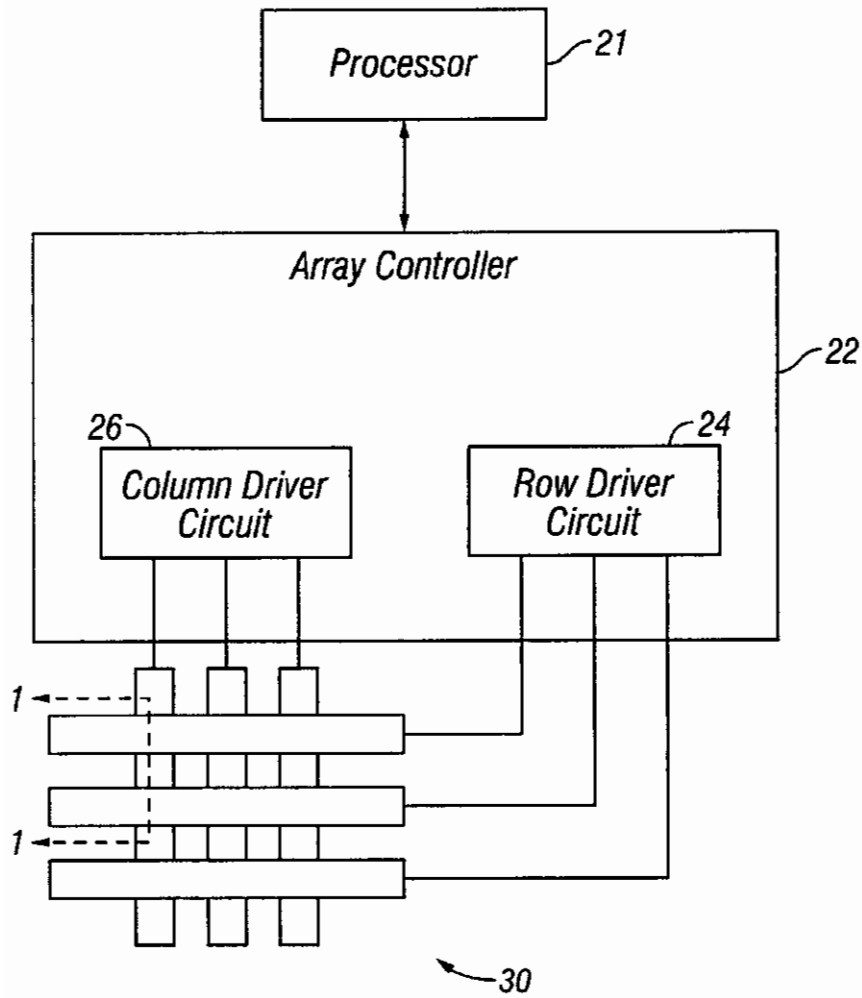
Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

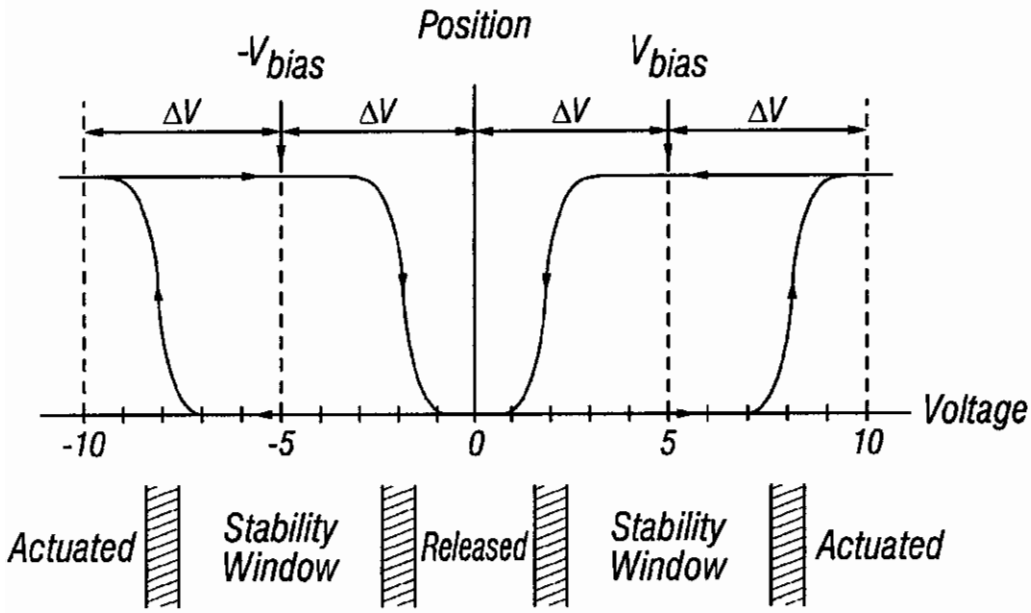

FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Release	Actuate

FIG. 4

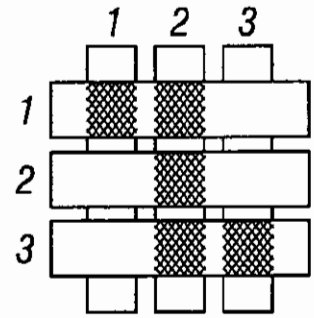
1
2
3
1
2
3

FIG. 5A

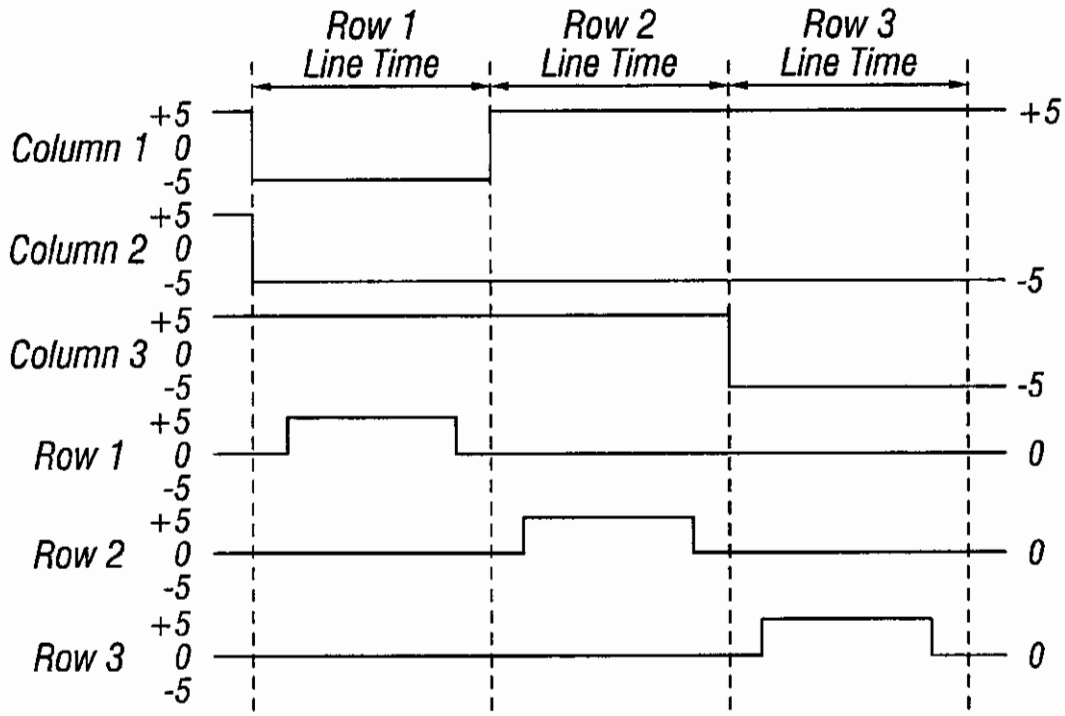
Row 1 Line Time
Row 2 Line Time
Row 3 Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

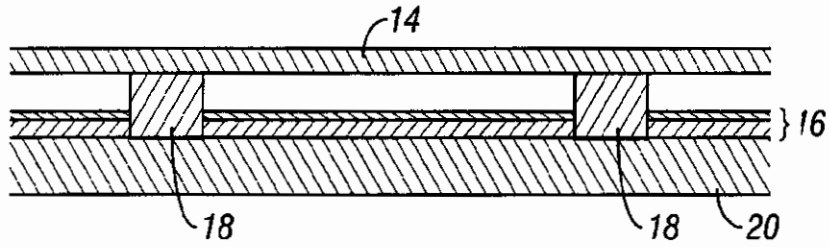

FIG. 6A

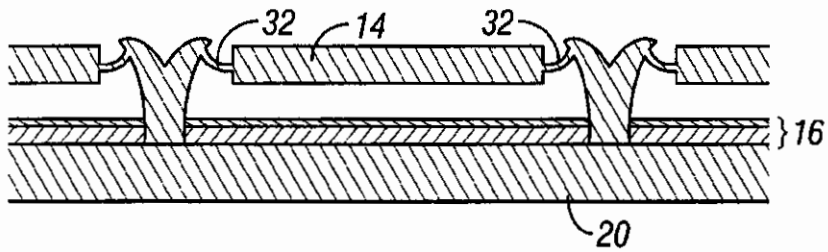

FIG. 6B

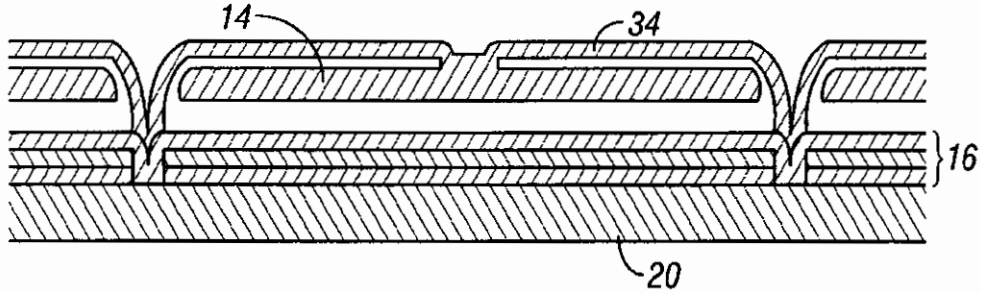

FIG. 6C

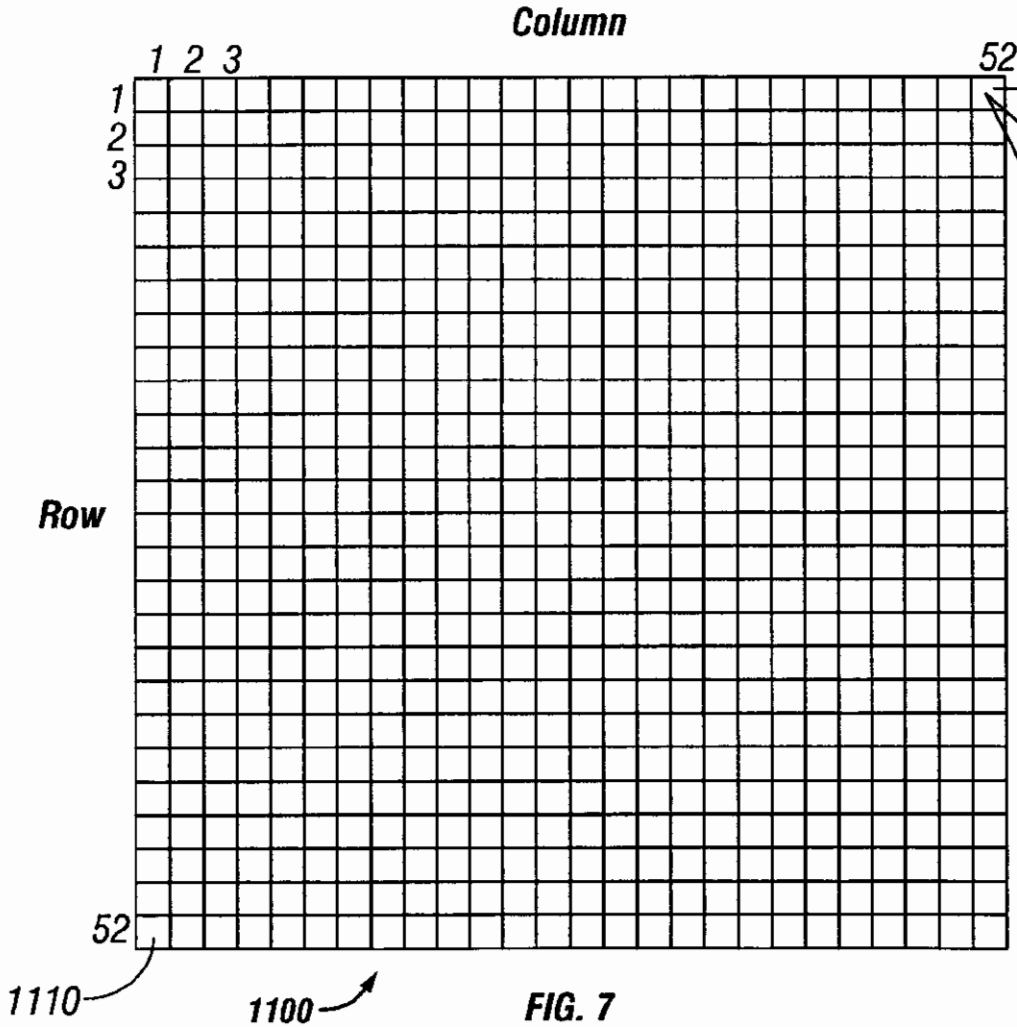

FIG. 7

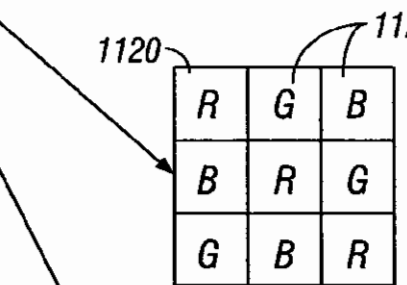

FIG. 8

Staggered RGB Sub-Pixel Structure

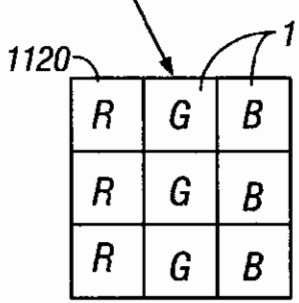

FIG. 9

Striped RGB Sub Pixel Structure

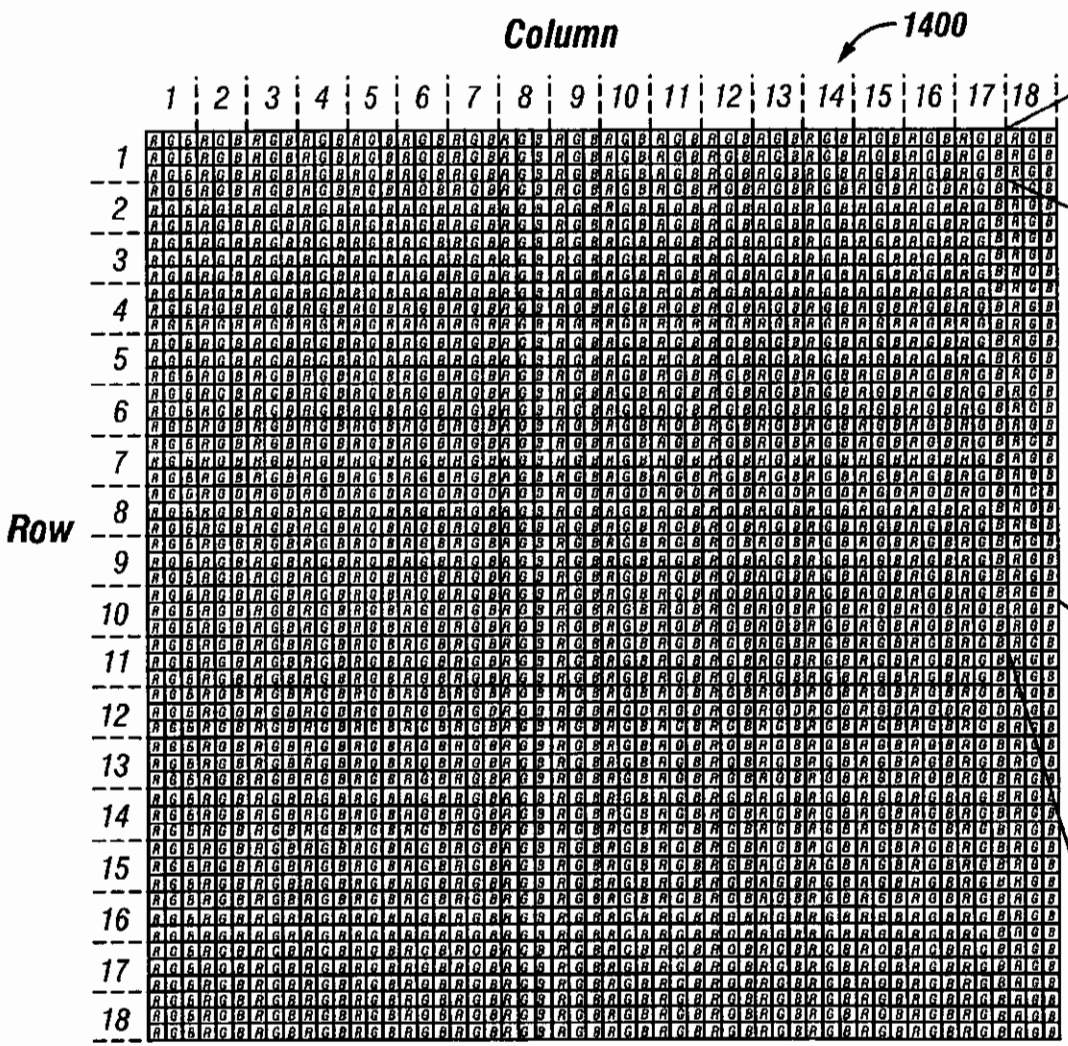

FIG. 10

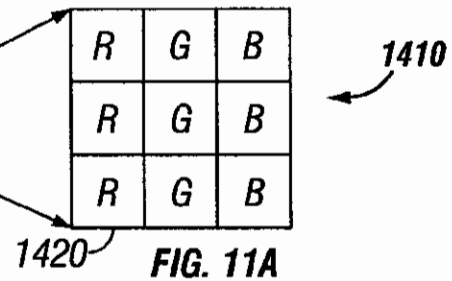

FIG. 11A

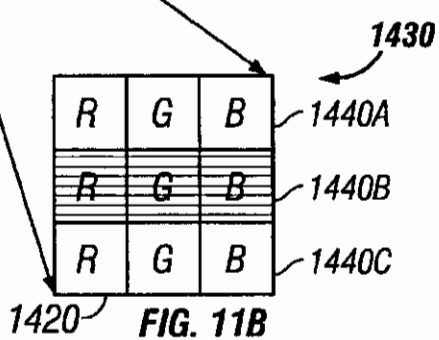

FIG. 11B

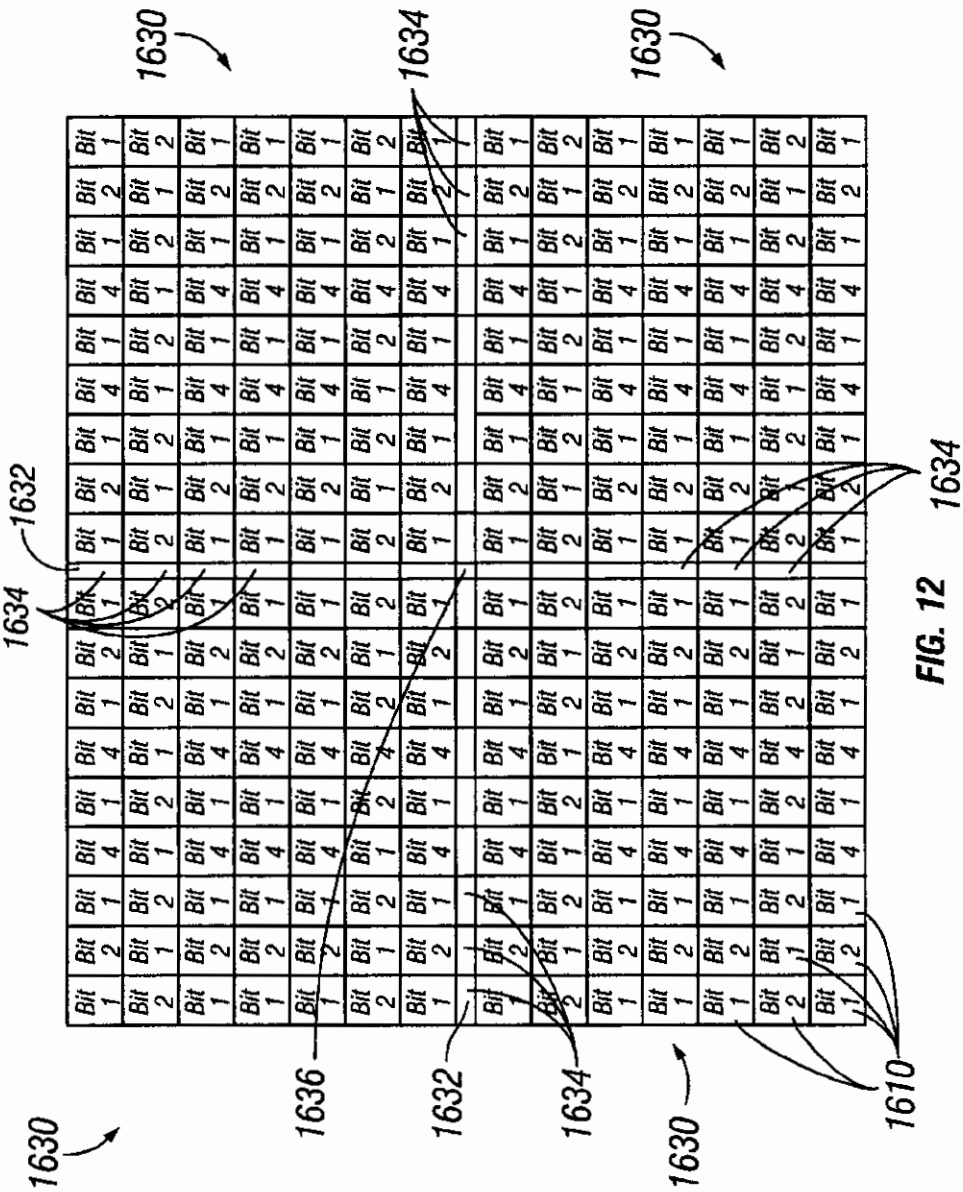

FIG. 12

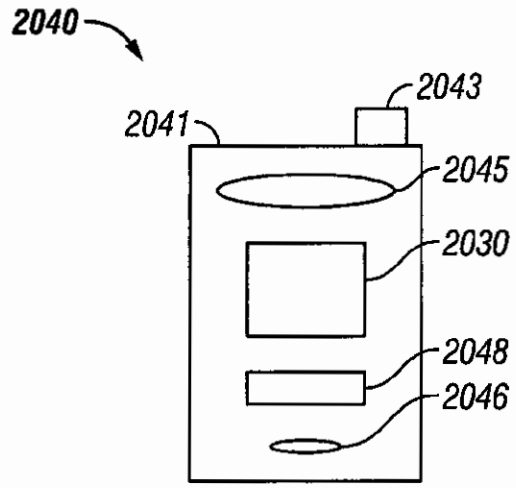

FIG. 13A

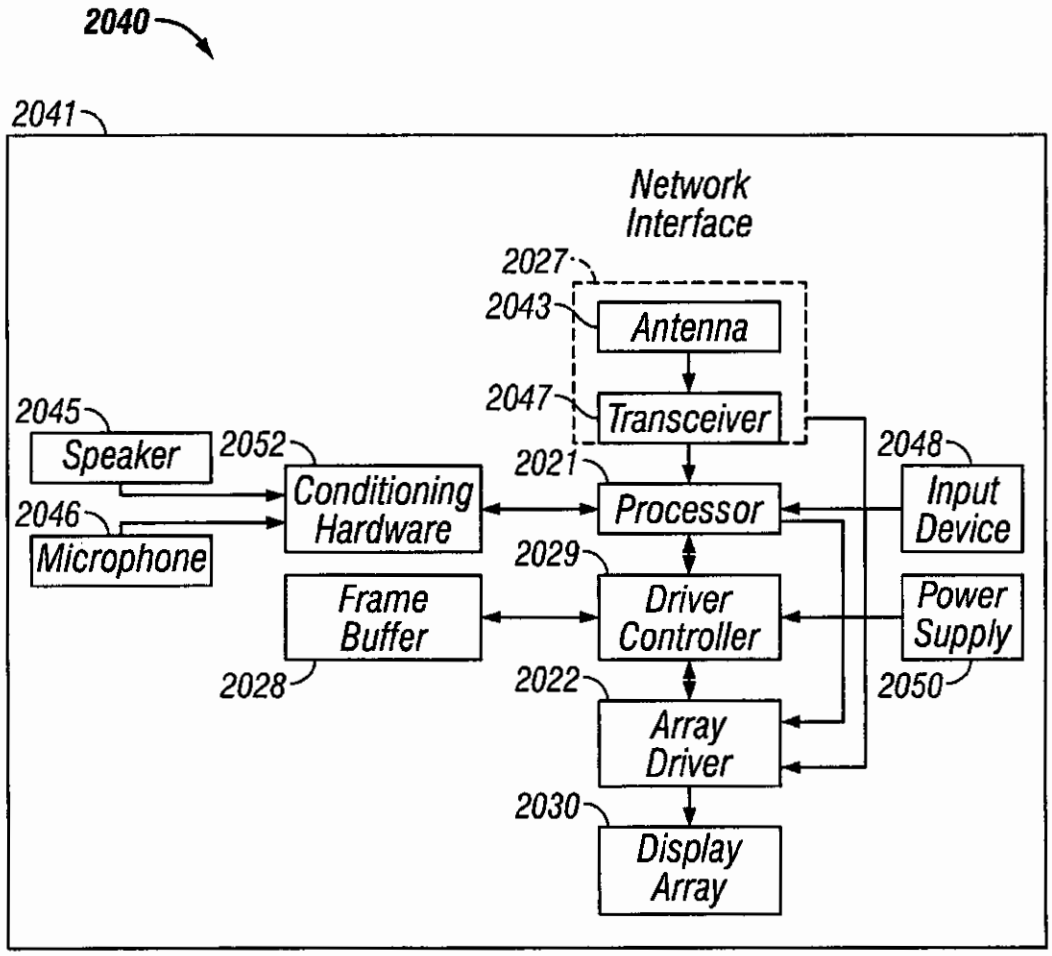

FIG. 13B