ABSTRACT

ACTIVATING SOURCE AND DRAIN JUNCTIONS AND EXTENSIONS USING A SINGLE LASER ANNEAL

A new method of forming MOS transistors with shallow source and drain extensions and deep source and drain junctions in the manufacture of an integrated circuit device has been achieved. Gates are provided overlying a semiconductor substrate. Temporary sidewall spacers are formed on the gates. Ions are implanted into the exposed semiconductor substrate to form a deep amorphous layer. Ions are implanted into the deep amorphous layer to form pre-annealed source and drain junctions. The temporary sidewall spacers are removed. Ions are implanted into the exposed semiconductor substrate to form a shallow amorphous layer. Ions are implanted into the shallow amorphous layer to form pre-annealed source and drain extensions. A capping layer may be deposited overlying the semiconductor substrate and the gates to protect the semiconductor substrate during irradiation. The semiconductor substrate is irradiated with laser light to melt the amorphous layer while the crystalline regions of the semiconductor substrate remain in solid state. Ions in the pre-annealed source and drain junctions diffuse in the deep amorphous layer while ions in the pre-annealed source and drain extensions diffuse into the shallower amorphous layer. The source and drain junctions and the source and drain extensions for the transistors are thereby simultaneously formed.

Fig. 9