APPARATUS AND METHODS FOR BIASING OF POWER AMPLIFIERS

BACKGROUND

Field

[0001] Embodiments of the invention relate to electronic systems, and in particular, to power amplifiers for radio frequency (RF) electronics.

Description of the Related Technology

[0002] Power amplifiers are used in radio frequency (RF) communication systems to amplify RF signals for transmission via antennas. It can be important to manage the power of RF signal transmissions to prolong battery life and/or provide a suitable transmit power level.

[0003] Examples of RF communication systems with one or more power amplifiers include, but are not limited to mobile phones, tablets, base stations, network access points, laptops, and wearable electronics. Power amplifiers provide amplification to RF signals, which can have a frequency in the range from about 30 kHz to 300 GHz, for instance, in a range from about 450 MHz to about 90 GHz for certain communication standards.

SUMMARY

[0004] In an aspect, the present disclosure relates to a mobile device. The mobile device includes a transceiver configured to generate a radio frequency input signal, a front end system including a power amplifier configured to receive the radio frequency input signal and to output a radio frequency output signal, and an antenna configured to wirelessly transmit the radio frequency output signal. The power amplifier includes a power amplifier transistor configured to amplify the radio frequency input signal, and a bias network configured to bias an input of the power amplifier transistor with a DC bias voltage. The bias network has a reactance operable to flatten a phase response of the power amplifier. The bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.

[0005] In some examples, the reactance is operable to track an intrinsic input capacitance of the power amplifier transistor.

[0006] In various examples, the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage. According to several examples, the bias impedance includes a first resistor, and the shunt impedance includes a second resistor and a capacitor in series. In accordance with a number of examples, the shunt impedance further includes an inductor in series with the second resistor and the capacitor. According to some examples, the reference voltage is ground.

[0007] In a number of examples, the power amplifier transistor is a bipolar transistor having a base corresponding to the input.

[0008] In various examples, the power amplifier transistor is a field effect transistor having a gate corresponding to the input.

[0009] In some examples, the bias network includes a resistor and a capacitor electrically connected in parallel between the input of the power amplifier transistor and the DC bias voltage.

[0010] In several examples, the power amplifier transistor is implemented as a plurality of transistor elements operating in parallel with one another. According to a number of examples, the bias network includes a plurality of resistors and a plurality of capacitors, each of the plurality of resistors connected in parallel with a corresponding one of the plurality of capacitors between the DC bias voltage and an input to a corresponding one of the plurality of transistor elements.

[0011] In various examples, the bias network includes a series combination of a capacitor and an inductor electrically connected between the DC bias voltage and the input to the power amplifier transistor, and a resistor in parallel with the series combination of the capacitor and the inductor.

[0012] In a number of examples, the power amplifier includes an input stage and an output stage, the power amplifier transistor incorporated in the output stage of the power amplifier.

[0013] In another aspect, the present disclosure relates to a power amplifier system. The power amplifier system includes a bias control circuit configured to generate a DC bias voltage, and a power amplifier configured to receive a radio frequency input signal and to output a radio frequency output signal. The power amplifier including a power amplifier transistor configured to amplify the radio frequency input signal, and a bias network configured to bias an input of the power amplifier transistor with the DC bias voltage. The bias network has a reactance operable to flatten a phase response of the power amplifier. The bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.

amplifying the radio frequency input signal using a power amplifier transistor of the power amplifier, and biasing an input of the power amplifier transistor with the DC bias voltage using a bias network of the power amplifier, including flattening a phase response of the power amplifier with a reactance of the bias network. The bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.

[0023] In some examples, the method further includes tracking an intrinsic input capacitance of the power amplifier transistor with the reactance of the bias network.

[0024] In several examples, the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage. According to a number of examples, the bias impedance includes a first resistor, and the shunt impedance includes a second resistor and a capacitor in series. In accordance with various examples, the shunt impedance further includes an inductor in series with the second resistor and the capacitor. According to several examples, the reference voltage is ground.

[0025] In various examples, the power amplifier transistor is a bipolar transistor having a base corresponding to the input.

[0026] In a number of examples, the power amplifier transistor is a field effect transistor having a gate corresponding to the input.

[0027] In several examples, the bias network includes a resistor and a capacitor electrically connected in parallel between the input of the power amplifier transistor and the DC bias voltage.

[0028] In some examples, the power amplifier transistor is implemented as a plurality of transistor elements operating in parallel with one another. According to several examples, the bias network includes a plurality of resistors and a plurality of capacitors, each of the plurality of resistors connected in parallel with a corresponding one of the plurality of capacitors between the DC bias voltage and an input to a corresponding one of the plurality of transistor elements. In accordance with various examples, the bias network includes a series combination of a capacitor and an inductor electrically connected between the DC bias voltage and the input to the power amplifier transistor, and a resistor in parallel with the series combination of the capacitor and the inductor. According to several examples, the power amplifier includes an input stage and an output stage, and the power amplifier transistor incorporated in the output stage of the power amplifier.

WHAT IS CLAIMED IS:

1. A mobile device comprising:

a transceiver configured to generate a radio frequency input signal;

a front end system including a power amplifier configured to receive the radio frequency input signal and to output a radio frequency output signal, the power amplifier including a power amplifier transistor configured to amplify the radio frequency input signal and a bias network configured to bias an input of the power amplifier transistor with a DC bias voltage, the bias network having a reactance operable to flatten a phase response of the power amplifier; and

an antenna configured to wirelessly transmit the radio frequency output signal; wherein the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.

2. The mobile device of claim 1 wherein the reactance is operable to track an intrinsic input capacitance of the power amplifier transistor.

~~3. The mobile device of claim 1 wherein the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.~~

~~4.~~3. The mobile device of claim ~~3~~ 1 wherein the bias impedance includes a first resistor, and the shunt impedance includes a second resistor and a capacitor in series.

~~5.~~4. The mobile device of claim ~~4~~ 3 wherein the shunt impedance further includes an inductor in series with the second resistor and the capacitor.

~~6.~~5. The mobile device of claim 1 wherein the bias network includes a resistor and a capacitor electrically connected in parallel between the input of the power amplifier transistor and the DC bias voltage.

~~7.~~6. The mobile device of claim 1 wherein the power amplifier transistor is implemented as a plurality of transistor elements operating in parallel with one another, and the bias network includes a plurality of resistors and a plurality of capacitors, each of the plurality of resistors connected in parallel with a corresponding one of the plurality of capacitors between the DC bias voltage and an input to a corresponding one of the plurality of transistor elements.

~~8.~~7. The mobile device of claim 1 wherein the bias network includes a series combination of a capacitor and an inductor electrically connected between the DC bias voltage and the input to the power amplifier transistor, and a resistor in parallel with the series combination of the capacitor and the inductor.

~~9.~~8. The mobile device of claim 1 wherein the power amplifier includes an input stage and an output stage, the power amplifier transistor incorporated in the output stage of the power amplifier.

~~10.~~9. A power amplifier system comprising:

a bias control circuit configured to generate a DC bias voltage; and

a power amplifier configured to receive a radio frequency input signal and to output a radio frequency output signal, the power amplifier including a power amplifier transistor configured to amplify the radio frequency input signal, and a bias network configured to bias an input of the power amplifier transistor with the DC bias voltage, the bias network having a reactance operable to flatten a phase response of the power amplifier;

wherein the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.

~~11.~~10. The power amplifier system of claim ~~10~~ 9 wherein the reactance is operable to track an intrinsic input capacitance of the power amplifier transistor.

~~12. The power amplifier system of claim 10 wherein the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.~~

~~13.~~11. The power amplifier system of claim ~~12~~ 9 wherein the bias impedance includes a first resistor, and the shunt impedance includes a second resistor and a capacitor in series.

~~14.~~12. The power amplifier system of claim ~~13~~ 11 wherein the shunt impedance further includes an inductor in series with the second resistor and the capacitor.

~~15.~~13. The power amplifier system of claim ~~10~~ 9 wherein the power amplifier transistor is a bipolar transistor having a base corresponding to the input.

~~16.~~14. The power amplifier system of claim ~~10~~ 9 wherein the bias network includes a resistor and a capacitor electrically connected in parallel between the input of the power amplifier transistor and the DC bias voltage.

~~17.~~15. The power amplifier system of claim ~~10~~ 9 wherein the power amplifier transistor is implemented as a plurality of transistor elements operating in parallel with one another, and the bias network includes a plurality of resistors and a plurality of capacitors, each of the plurality of resistors connected in parallel with a corresponding one of the plurality of capacitors between the DC bias voltage and an input to a corresponding one of the plurality of transistor elements.

~~18.~~16. The power amplifier system of claim ~~10~~ 9 wherein the bias network includes a series combination of a capacitor and an inductor electrically connected between the DC bias voltage and the input to the power amplifier transistor, and a resistor in parallel with the series combination of the capacitor and the inductor.

~~19.~~17. A method of biasing a power amplifier, the method comprising:

generating a DC bias voltage using a bias control circuit;

receiving a radio frequency input signal as an input to a power amplifier;

amplifying the radio frequency input signal using a power amplifier transistor of the power amplifier; and

biasing an input of the power amplifier transistor with the DC bias voltage using a bias network of the power amplifier, including flattening a phase response of the power amplifier with a reactance of the bias network; wherein the bias network includes a bias impedance electrically connected between the DC bias voltage and the input of the power amplifier transistor, and a shunt impedance electrically connected between the input of the power amplifier transistor and a reference voltage.

~~20.~~18. The method of claim 19 further comprising tracking an intrinsic input capacitance of the power amplifier transistor with the reactance of the bias network.