

METHOD OF FORMING SILICON CARBIDE EPITAXIAL WAFER AND SILICON CARBIDE SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of Singapore application No. 10202113497Q filed December 3, 2021, the contents of it being hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] Various embodiments of this disclosure may relate to a method of forming a silicon carbide epitaxial wafer, and a silicon carbide epitaxial wafer formed thereof. Various embodiments may further relate to a method of forming a silicon carbide substrate.

BACKGROUND

[0003] Silicon carbide (SiC) power electronic devices like metal-oxide-semiconductor field-effect transistor (MOSFETs) and Schottky Barrier Diodes (SBDs) have seen rising demand due to increased adoption in applications like electric vehicles. However, SiC power electronic devices remain more expensive than conventional silicon-based power electronic devices due to the high costs of SiC substrates and high SiC epilayer defect densities resulting in low chip yields. Yield-killer defects include surface morphological defects (carrots, triangles, downfalls) and bulk defects (in-grown stacking faults, basal plane dislocations). It is known that SiC epilayer defect density may be affected by factors such as substrate defect density and epitaxy growth conditions.

[0004] High densities of crystal defects in SiC epiwafers remain challenges for their applications in SiC power electronic devices.

SUMMARY

[0005] Various embodiments may relate to a method of forming a silicon carbide epitaxial wafer. The method may include providing a silicon carbide substrate with a predetermined negative substrate bow; and forming a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate.

[0006] Various embodiments may relate to a method of preparing a substrate. The method may include forming a protective layer on a front surface of a silicon carbide substrate; conducting an ion implantation of predetermined dopants on a back surface of the silicon carbide substrate, thereby forming the silicon carbide substrate with a predetermined negative substrate bow; and removing the protective layer from the front surface of the silicon carbide substrate.

[0007] Various embodiments may relate to a silicon carbide epitaxial wafer. The silicon carbide epitaxial wafer may include a silicon carbide substrate; and a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate, wherein the silicon carbide epitaxial layer may be formed on the silicon carbide substrate having a predetermined negative substrate bow.

[0008] Various embodiments may relate to a silicon carbide epitaxial wafer. The silicon carbide epitaxial wafer may include a silicon carbide substrate; and a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate. A stacking fault density in the silicon carbide epitaxial layer may be less than 1.0 per cm^2 , and a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide epitaxial layer may be lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate.

[0009] Various embodiments may relate to a silicon carbide epitaxial wafer. The silicon carbide epitaxial wafer may include a silicon carbide substrate; and a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate. The silicon carbide substrate may include a layer of predetermined dopants at a back surface of the silicon carbide substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily drawn to scale, emphasis instead generally being placed upon illustrating the principles of various embodiments. In the following description, various embodiments of the invention are described with reference to the following drawings.

FIG. 1 is a general illustration of a method of forming a silicon carbide epitaxial wafer according to various embodiments.

FIG. 2 shows a schematic of a silicon carbide substrate according to various embodiments.

FIG. 3 is a general illustration of a method of preparing a substrate according to various embodiments.

FIG. 4 shows a schematic of a silicon carbide epitaxial wafer according to various embodiments.

FIG. 5 shows a schematic illustrating basal plane dislocations in a silicon carbide epitaxial wafer according to various embodiments.

FIG. 6 shows a) a plot of BPD density (in cm^{-2}) as a function of a SiC substrate bow (in micrometers or μm) illustrating the experiment results of the present disclosure; b) a plot of SF density (in cm^{-2}) as a function of a SiC substrate bow (in micrometers or μm); c) a plot of BPD density (in cm^{-2}) as a function of a SiC epitaxial wafer bow (in micrometers or μm) after epitaxy; d) a plot of SF density (in cm^{-2}) as a function of a SiC epitaxial wafer bow (in

micrometers or μm) after epitaxy; e) a plot of BPD density (in cm^{-2}) as a function of a bow change from epitaxy (in micrometers or μm) ; and f) a plot of SF density (in cm^{-2}) as a function of a bow change from epitaxy (in micrometers or μm); illustrating the experiment results of the present disclosure.

DESCRIPTION

[0011] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0012] Embodiments described in the context of one of the methods or structures are analogously valid for the other methods or structures. Similarly, embodiments described in the context of a method are analogously valid for a wafer structure and a substrate structure, and vice versa.

[0013] Features that are described in the context of an embodiment may correspondingly be applicable to the same or similar features in the other embodiments. Features that are described in the context of an embodiment may correspondingly be applicable to the other embodiments, even if not explicitly described in these other embodiments. Furthermore, additions and/or combinations and/or alternatives as described for a feature in the context of an embodiment may correspondingly be applicable to the same or similar feature in the other embodiments.

[0014] The wafer and the substrate as described herein may be operable in various orientations, and thus it should be understood that the terms “top”, “bottom”, etc., when used in the following description are used for convenience and to aid understanding of relative positions or directions, and not intended to limit the orientation of the wafer/substrate structure.

[0015] In the context of various embodiments, the articles “a”, “an” and “the” as used with regard to a feature or element include a reference to one or more of the features or elements.

[0016] In the context of various embodiments, the term “about” or “approximately” as applied to a numeric value encompasses the exact value and a reasonable variance.

[0017] As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[0018] Various embodiments may provide a method of reducing silicon carbide (SiC) epilayer yield-killer defects, e.g., bulk defects like in-grown stacking faults (SF) and basal plane dislocations (BPD) in SiC epilayers. Various embodiments may provide a silicon carbide epitaxial wafer wherein stacking faults and basal plane dislocations may be reduced. Based on the findings of the present disclosure, various embodiments may provide unexpected improvements in the reduction of stacking faults and basal plane dislocations.

[0019] FIG. 1 is a general illustration of a method of forming a silicon carbide (SiC) epitaxial wafer according to various embodiments.

[0020] At 102, a silicon carbide substrate with a predetermined negative substrate bow may be provided. At 104, a silicon carbide epitaxial layer may be formed on a front surface of the silicon carbide substrate, thereby forming the silicon carbide epitaxial wafer.

[0021] In other words, SiC epitaxy may be conducted on the SiC substrate having a negative bow, based on the finding of the present disclosure that negative SiC substrate bow may result in lower densities of SiC epilayer defect. Accordingly, the method according to

various embodiments may use the SiC substrate with a negative substrate bow prior to SiC epitaxy to achieve lower densities of yield-killer crystal defects in the SiC epitaxial layers.

[0022] In this context, the SiC substrate with the predetermined negative substrate bow may refer to a concave type SiC substrate, e.g., as shown in FIG. 2 below wherein the the SiC substrate is in a concave shape when the front surface of the silicon carbide substrate is facing up and a back surface of the silicon carbide substrate is facing down. The front surface of the SiC substrate may refer to a Si-face of the SiC substrate which may be an epi-ready surface on which SiC epitaxy may be conducted, and the back surface may refer to a C-face of the SiC substrate which is terminated by carbon atoms. Bow represents the deviation of a center point of the median surface of a free, un-clamped wafer/substrate from a reference plane, where the reference plane is defined by three corners of an equilateral triangle. A concave SiC substrate may have a negative substrate bow, and a convex SiC substrate may have a positive substrate bow. A flat SiC substrate may have a zero substrate bow.

[0023] In various embodiments, the predetermined negative substrate bow may be in a range between about $-15\mu\text{m}$ and $0\mu\text{m}$. In an example, the predetermined negative substrate bow may be in a range between about $-10\mu\text{m}$ and about $-5\mu\text{m}$. In another example, the predetermined negative substrate bow may be about $-3\mu\text{m}$.

[0024] In various embodiments, the SiC substrate may be a 4H-SiC substrate. In other embodiments, the SiC substrate having other polytypes may be provided, such as a 3C-SiC or 6H-SiC substrate.

[0025] SiC substrates used in power electronics applications may be heavily doped with nitrogen (e.g., about 10^{19} cm^{-3}), and SiC epitaxial layers may be lightly doped with nitrogen (e.g., about 10^{16} cm^{-3}). Since heavy nitrogen doping may result in contraction of the SiC crystal lattice, the SiC epitaxial layer may have a larger lattice constant than the SiC substrate. As a result and as an example, a SiC substrate starting with a zero (flat) bow may take on a positive

(convex) wafer bow after SiC epitaxy, due to the epitaxy misfit stress between the SiC epitaxial layer and the SiC substrate.

[0026] A total wafer stress may be given by an algebraic sum of a pre-existing SiC substrate stress, epitaxy misfit stress between the SiC epitaxial layer and the SiC substrate, and thermal stress due to temperature non-uniformities during epitaxy. As described above, the epitaxy misfit stress may be due to lower nitrogen doping density (e.g., about $1 \times 10^{16} \text{ cm}^{-3}$) in the SiC epitaxial layer compared to that in the SiC substrate (e.g., about $8 \times 10^{18} \text{ cm}^{-3}$). Nitrogen dopants may contract the SiC crystal lattice, e.g., the 4H-SiC crystal lattice, placing the SiC epitaxial layer under compressive stress. According to various embodiments of the present disclosure wherein the SiC substrate may be provided or engineered with negative (concave) bow prior to SiC epitaxy, the pre-existing SiC substrate stress thereof may counteract the epitaxy misfit stress, in contrast to a SiC substrate with positive (convex) bow wherein the pre-existing SiC substrate stress may act in the same direction as the epitaxy misfit stress. When the total wafer stress exceeds a critical resolved shear stress (CRSS), e.g., approximately +1MPa in 4H-SiC, basal planes may slip and misfit dislocations may form, resulting in the formation of stacking faults (SF) and basal plane dislocations (BPD). The method of various embodiments is based on the finding of the present disclosure that the total wafer stress may be more likely to stay within the CRSS limit when the SiC epitaxial layer is grown on the SiC substrate with a negative (concave) substrate bow, in contrast to a SiC epitaxial layer grown on a SiC substrate with positive (convex) substrate bow which is more likely for the CRSS to be exceeded. Accordingly, formation of yield-killer SiC crystal defects, such as stacking faults (SF) and basal plane dislocations (BPD), may be suppressed by the method of FIG. 1 which provides negative (concave) SiC substrate bow prior to epitaxy to form the SiC epitaxial wafer.

[0027] Further, the majority of in-grown SF defects formed during SiC epitaxy may be Shockley-type SF defects with (44), (53) and (62) stacking sequences in Zhdanov's notation.

Shockley-type SF defects may be formed due to basal plane slips when lateral shear stresses exceed the CRSS. Based on the finding of the present disclosure, SiC epitaxy on substrates with positive (convex) bow may enhance the formation of in-grown SF defects, while SiC epitaxy on substrates with negative (concave) bow according to various embodiments of the present disclosure may suppress the formation of in-grown SF defects. In addition, BPD defects may be highly correlated with in-grown SF defects since BPD defects may be found around the periphery of in-grown SF defects. Accordingly, the method according to various embodiments above may suppress the formation of SF and BPD defects.

[0028] According to various embodiments, a stacking fault density in the silicon carbide epitaxial layer formed according to the embodiments of FIG. 1 may be less than 1.0 per cm^2 . In addition, a density of basal plane dislocation with an extra half-plane (EHP) pointing towards the silicon carbide epitaxial layer (BPD+) is lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate (BPD-), as illustrated in FIG. 5 below.

[0029] According to various embodiments, the method of FIG. 1 may further include forming the silicon carbide substrate with the predetermined negative substrate bow by ion implantation. In other words, a silicon carbide substrate with any pre-existing bow values (e.g., positive, negative, or zero) may be provided, and may be engineered or prepared by the method of the present disclosure to form the predetermined negative substrate bow.

[0030] The silicon carbide substrate provided or formed according to the method of various embodiments may be a 4H-SiC substrate. In other embodiments, the SiC substrate having other polytypes may be provided or formed, such as a 3C-SiC or 6H-SiC substrate.

[0031] In an embodiment, at least one of a dose, an energy or a type of dopants for the ion implantation may be determined based on the predetermined negative substrate bow. In other words, the dose, energy and/or the type of dopants for the ion implantation may be selected

based on a target negative bow value. Accordingly, at least one of the type of dopants, dose, or energy for the ion implantation at the C-face of the SiC substrate may be controlled or adjusted to produce SiC substrates with different target bow values for different SiC epitaxial designs and SiC device applications. In various embodiments, the energy for the ion implantation may be selected in a range of about 200keV-600keV, and the dose may be selected in a range of about $1 \times 10^{13} \text{cm}^{-2}$ – $1 \times 10^{15} \text{cm}^{-2}$ for Phosphorus (P) or Aluminum (Al) dopants. The energy used for ion implantation may dictate the depth of the implanted species (e.g., on the order of micrometers). Al and P may have similar doping profile in the SiC substrate. In an example, Al implant with a dose of $1 \times 10^{13} \text{cm}^{-2}$ at 200keV may have a depth of $0.6 \mu\text{m}$ with a corresponding dopant concentration of about $1.7 \times 10^{17} \text{cm}^{-3}$, achieving a target negative bow around $-10 \mu\text{m}$. In another example, Al implant with a dose of $1 \times 10^{13} \text{cm}^{-2}$ at 600keV may have a depth of $1 \mu\text{m}$ with a corresponding dopant concentration of about $1 \times 10^{17} \text{cm}^{-3}$, achieving a target negative bow around $-10 \mu\text{m}$.

[0032] In various embodiments, the method of forming the SiC substrate in FIG. 1 may include conducting the ion implantation of predetermined dopants on a back surface of the silicon carbide substrate to form a layer of the predetermined dopants at the back surface of the silicon carbide substrate, thereby forming the silicon carbide substrate with the predetermined negative substrate bow.

[0033] In further embodiments, the method of forming the SiC substrate in FIG. 1 may include forming a protective layer or capping layer on a front surface of the silicon carbide substrate before conducting the ion implantation, and removing the protective layer or capping layer from the front surface of the silicon carbide substrate after conducting the ion implantation. In an example, the protective layer or capping layer may include silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). The protective layer or capping layer may be provided to

prevent contamination of the SiC substrate front surface while conducting ion implantation on the SiC substrate back surface.

[0034] In various embodiments, the ion implantation, e.g., on the 4H-SiC substrate, may be conducted at temperatures between room temperature (RT) and 650°C. In further embodiments, the ion implantation may be conducted at temperatures, e.g., between 100°C and 650°C, e.g., between 300°C and 650°C, e.g., between 500°C and 650°C.

[0035] In various embodiments, the predetermined dopants may include at least one of Phosphorus (P), Aluminum (Al), Titanium (Ti), Chromium (Cr), Iron (Fe), Vanadium (V), or Germanium (Ge). In various embodiments, the predetermined dopants may include any other types of dopants which may expand the SiC crystal lattice, e.g., the 4H-SiC crystal lattice. In various embodiments, a doping concentration of the predetermined dopants may be in a range between $1 \times 10^{16} \text{cm}^{-3}$ and $1 \times 10^{20} \text{cm}^{-3}$. In various embodiments, a depth of the layer of the predetermined dopants may be in a range between 0.1 μm and 2.0 μm , e.g., between 0.1 μm and 1.0 μm .

[0036] In various embodiments based on the findings of the present disclosure, when performing ion implantation on the back surface of the SiC substrate using dopants like phosphorus or aluminum, the SiC substrate will take on a negative (concave) bow due to the implantation damage and the additional atoms introduced by the ion implantation. Accordingly, ion implantation, e.g., high-dose ion implantation, may form the predetermined negative substrate bow in the silicon carbide substrate due to the introduction of additional atoms expanding the crystal lattice and crystal amorphization. In an exemplary embodiment, a phosphorus doping concentration of about $1 \times 10^{20} \text{cm}^{-3}$, an implantation depth on the order of hundreds of nanometers to one micrometer may be used to generate a negative (concave) substrate bow of about -5 μm to -10 μm . This negative (concave) substrate bow will suppress the formation of in-grown SF and BPD defects during SiC epitaxy.

[0037] During the subsequent SiC epitaxy process (e.g., at about 1600°C), the negative (concave) wafer bow may be reduced as the implantation damage is repaired, leaving a residual negative (concave) wafer bow (e.g., as shown in FIG. 6 below) that may be attributed to phosphorus or aluminum dopants expanding the SiC crystal lattice on the wafer backside.

[0038] According to the method of various embodiments above, lower densities of SF and BPD defects in SiC epitaxial layers may be achieved, which may improve SiC MOSFET chip yield. For a 10 mm² chip area, reduction of SF and BPD defect density from 5 cm⁻² to 1 cm⁻² may increase the chip yield from 60% to 90%. Higher chip yields result in lower cost of manufacturing per chip. Hence, the method of various embodiments above is effective in enabling significantly higher SiC power device chip yield. In addition, the method of various embodiments above is highly amenable for mass manufacturing.

[0039] The silicon carbide epitaxial wafer formed according to the method of various embodiments above may be applied in power electronic devices, such as metal-oxide-semiconductor field-effect transistor (MOSFET) and Schottky-barrier diode (SBD).

[0040] FIG. 2 shows a schematic of a silicon carbide substrate 210 according to various embodiments. Many of the aspects of the silicon carbide substrate 210 are the same or similar to those described with reference to the method of FIG. 1. For the sake of brevity, duplicate descriptions of features and properties are omitted. It will be understood that the descriptions of any feature and/or property relating to FIG. 2 that are the same or similar to a feature and/or property in FIG. 1 will have those descriptions be applicable hereinbelow as well.

[0041] As shown in FIG. 2, the silicon carbide substrate 210 may have a negative substrate bow, which may be in a concave shape when a front surface 212 of the silicon carbide substrate 210 is facing up and a back surface 214 of the silicon carbide substrate 210 is facing down.

[0042] In various embodiments, the predetermined negative substrate bow may be in a range between about -15μm and 0μm. In various embodiments, the predetermined negative

substrate bow may be in a range between about -10 μm and about -5 μm . In an example, the predetermined negative substrate bow may be about -3 μm .

[0043] The front surface 212 of the SiC substrate 210 may refer to a Si-face of the SiC substrate 210, which may be an epi-ready surface on which SiC epitaxy may be conducted. The back surface 214 may refer to a C-face of the SiC substrate 210, which is terminated by carbon atoms.

[0044] According to various embodiments, the silicon carbide substrate 210 may include a layer or region 216 of predetermined dopants at the back surface 214 of the silicon carbide substrate 210. The layer 216 with implanted dopants may expand crystal lattice on the backside of the silicon carbide substrate 210, giving rise to the negative (concave) bow of the silicon carbide substrate 210.

[0045] In various embodiments, the predetermined dopants may include at least one of Phosphorus (P), Aluminum (Al), Titanium (Ti), Chromium (Cr), Iron (Fe), Vanadium (V), or Germanium (Ge). In various embodiments, the predetermined dopants may include any other types of dopants which may expand the SiC crystal lattice, e.g., the 4H-SiC crystal lattice.

[0046] In various embodiments, a doping concentration of the predetermined dopants may be in a range between $1 \times 10^{16} \text{cm}^{-3}$ and $1 \times 10^{20} \text{cm}^{-3}$.

[0047] In various embodiments, a depth of the layer of the predetermined dopants may be in a range between 0.1 μm and 2.0 μm , e.g., between 0.1 μm and 1.0 μm .

[0048] In an embodiment, the silicon carbide substrate 210 may be a 4H-SiC substrate. In other embodiments, the silicon carbide substrate 210 may have other polytypes, and may be a 3C-SiC or 6H-SiC substrate, for example.

[0049] By providing or preparing the silicon carbide substrate 210 with the predetermined negative substrate bow, formation of SF and BPD may be suppressed when the epilayer is grown on the front surface 212 of the silicon carbide substrate 210.

[0050] FIG. 3 is a general illustration of a method of preparing a substrate, e.g., the silicon carbide substrate of FIG. 2, according to various embodiments. Many of the aspects of the method of FIG. 3 are the same or similar to those described with reference to the method of FIG. 1 and the silicon carbide substrate of FIG. 2. It will be understood that the descriptions of any feature and/or property relating to FIG. 3 that are the same or similar to a feature and/or property in FIG. 1 and FIG. 2 will have those descriptions be applicable hereinbelow as well.

[0051] At 302, a protective layer or capping layer may be formed on a front surface of a silicon carbide substrate.

[0052] At 304, an ion implantation of predetermined dopants may be conducted on a back surface of the silicon carbide substrate, thereby forming the silicon carbide substrate with a predetermined negative substrate bow.

[0053] At 306, the protective layer or capping layer may be removed from the front surface of the silicon carbide substrate.

[0054] According to various embodiments, the silicon carbide substrate with any pre-existing bow values (e.g., positive, negative, or zero) may be provided, and may be engineered or prepared according to the method of FIG. 3 to achieve the predetermined negative substrate bow.

[0055] The silicon carbide substrate prepared according to various embodiments of FIG. 3 may be a 4H-SiC substrate. In other embodiments, the SiC substrate prepared according to various embodiments of FIG. 3 may have other polytypes, and may be a 3C-SiC or 6H-SiC substrate, for example.

[0056] In various embodiments, the ion implantation may be performed uniformly across the backside of the silicon carbide substrate, using dopants, such as phosphorus, that expand the SiC crystal lattice (e.g., the 4H-SiC crystal lattice). The expansion of 4H-SiC crystal lattice

on the wafer backside may place the implanted region under compressive stress, producing the negative (concave) substrate bow in the silicon carbide substrate.

[0057] In an embodiment, at least one of a dose, an energy or a type of dopants for the ion implantation in 304 may be determined based on the predetermined negative substrate bow. In other words, the dose, energy and/or the type of dopants for the ion implantation may be selected based on a target negative bow value. Accordingly, at least one of the type of dopants, dose, and energy for the ion implantation on the back surface (e.g., the C-face) of the SiC substrate in 304 may be controlled or adjusted to produce SiC substrates with different target bow values for different SiC epitaxial designs and SiC device applications. In various embodiments, the energy for the ion implantation may be in a range of about 200keV-600keV, and the dose may be in a range of about $1 \times 10^{13} \text{cm}^{-2}$ – $1 \times 10^{15} \text{cm}^{-2}$ for Al or P dopants. The energy used for ion implantation may dictate the depth of the implanted species (e.g., on the order of micrometers). Al and P may have similar doping profile in the SiC substrate. In an example, Al implant with a dose of $1 \times 10^{13} \text{cm}^{-2}$ at 200keV may have a depth of $0.6 \mu\text{m}$ with a corresponding dopant concentration of about $1.7 \times 10^{17} \text{cm}^{-3}$, achieving a target negative bow around $-10 \mu\text{m}$. In another example, Al implant with a dose of $1 \times 10^{13} \text{cm}^{-2}$ at 600keV may have a depth of $1 \mu\text{m}$ with a corresponding dopant concentration of about $1 \times 10^{17} \text{cm}^{-3}$, achieving a target negative bow around $-10 \mu\text{m}$.

[0058] In various embodiments, the ion implantation of predetermined dopants on the back surface of the silicon carbide substrate may form a layer of the predetermined dopants at the back surface of the silicon carbide substrate, thereby forming the silicon carbide substrate with the predetermined negative substrate bow.

[0059] In various embodiments, the protective layer or capping layer may include silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). The protective layer or capping layer may be provided

to prevent contamination of the SiC substrate front surface while conducting ion implantation on the SiC substrate back surface.

[0060] In various embodiments, the ion implantation may be conducted on the silicon carbide substrate, e.g., a 4H-SiC substrate, at temperatures between room temperature (RT) and 650°C. In further embodiments, the ion implantation may be conducted at temperatures, e.g., between 100°C and 650°C, e.g., between 300°C and 650°C, e.g., between 500°C and 650°C.

[0061] In various embodiments, the predetermined dopants may include at least one of Phosphorus (P), Aluminum (Al), Titanium (Ti), Chromium (Cr), Iron (Fe), Vanadium (V), or Germanium (Ge). In various embodiments, the predetermined dopants may include any other types of dopants which may expand the SiC crystal lattice, e.g., the 4H-SiC crystal lattice.

[0062] In various embodiments, a doping concentration of the predetermined dopants may be in a range between $1 \times 10^{16} \text{ cm}^{-3}$ and $1 \times 10^{20} \text{ cm}^{-3}$.

[0063] In various embodiments, a depth of the layer of the predetermined dopants may be in a range between 0.1 μm and 2.0 μm , e.g., between 0.1 μm and 1.0 μm .

[0064] In various embodiments, when performing ion implantation on the back surface of the SiC substrate using dopants like phosphorus or aluminum, the SiC substrate will take on a negative (concave) bow due to the implantation damage and the additional atoms introduced by the ion implantation. Accordingly, ion implantation may form the predetermined negative substrate bow in the silicon carbide substrate due to the introduction of additional atoms expanding the 4H-SiC crystal lattice and crystal amorphization. In an exemplary embodiment, a phosphorus doping concentration of about $1 \times 10^{20} \text{ cm}^{-3}$, and an implantation depth on the order of hundreds of nanometers to one micrometer may be used to generate a negative (concave) substrate bow of about -5 μm to -10 μm . This negative (concave) substrate bow will suppress the formation of in-grown SF and BPD defects during SiC epitaxy.

[0065] Since ion implantation is commonly used in the SiC industry for manufacturing of SiC MOSFETs (e.g., for doping of source and p-well regions) and is highly economical, the method of FIG. 3 is thus highly amenable in the SiC industry for stress engineering of SiC substrates in a high-throughput fashion. Further, ion-implanted dopants at the back surface of the SiC substrate are stable and do not diffuse into the SiC substrate at the high temperatures (e.g., 1600°C) used during epitaxy, and thus the effectiveness of ion implantation in engineering substrate bow will be maintained.

[0066] After the silicon carbide substrate with the predetermined negative substrate bow is prepared according to the method of FIG. 3, a silicon carbide epitaxial layer may be formed on the front surface of the silicon carbide substrate according to 104 of the method in FIG. 1 to form a silicon carbide epitaxial wafer according to various embodiments of the present disclosure. The engineering or preparing of negative (concave) substrate bow according to various embodiments of FIG. 3 is highly effective in suppressing the formation of in-grown SF and BPD defects in the silicon carbide epitaxial layer, enabling significantly higher SiC power device chip yield.

[0067] FIG. 4 shows a schematic of a silicon carbide epitaxial wafer 400 according to various embodiments, e.g., formed according to the method of FIG. 1. Many of the aspects of FIG. 4 are the same or similar to those described with reference to the method of FIG. 1, FIG. 3, and the silicon carbide substrate of FIG. 2. It will be understood that the descriptions of any feature and/or property relating to FIG. 4 that are the same or similar to a feature and/or property in FIG. 1 - FIG. 3 will have those descriptions be applicable hereinbelow as well.

[0068] As shown in FIG. 4, the silicon carbide epitaxial wafer 400 may include a silicon carbide substrate 410, and a silicon carbide epitaxial layer 420 on a front surface 412 of the silicon carbide substrate 410. The silicon carbide epitaxial layer 420 may be formed on the

silicon carbide substrate 410 having a predetermined negative substrate bow, as described in various embodiments above.

[0069] Similar to the silicon carbide substrate 210 of FIG. 2, the silicon carbide substrate 410 may have a negative substrate bow. Accordingly, the silicon carbide substrate 410 may be in a concave shape when the front surface 412 of the silicon carbide substrate 410 is facing up and a back surface 414 of the silicon carbide substrate 410 is facing down. The front surface 412 of the SiC substrate 410 may refer to a Si-face of the SiC substrate 410, which may be an epi-ready surface on which SiC epitaxy may be conducted. The back surface 414 may refer to a C-face of the SiC substrate 410, which is terminated by carbon atoms.

[0070] In various embodiments, the predetermined negative substrate bow of the silicon carbide substrate 410 may be in a range between about $-15\mu\text{m}$ and $0\mu\text{m}$. In various embodiments, the predetermined negative substrate bow may be in a range between about $-10\mu\text{m}$ and about $-5\mu\text{m}$. In an example, the predetermined negative substrate bow may be about $-3\mu\text{m}$.

[0071] When the silicon carbide epitaxial layer 420 is formed on the silicon carbide substrate 410 through a SiC epitaxy process (e.g., according to the method of FIG. 1 above), the predetermined negative (concave) substrate bow of the initial silicon carbide substrate 410 may be reduced (e.g., by about $5\mu\text{m}$ to $10\mu\text{m}$), leaving a residual wafer bow (e.g., negative, positive, or zero) that may be attributed to phosphorus or aluminum dopants expanding the SiC crystal lattice on the wafer backside. By way of example, the initial silicon carbide substrate 410 may have a predetermined negative (concave) substrate bow of about $-15\mu\text{m}$, and the silicon carbide epitaxial wafer 400 with its silicon carbide epitaxial layer 420 formed on such an initial silicon carbide substrate 410 may have a negative (concave) wafer bow of about $-5\mu\text{m}$, since SiC epitaxy may induce a positive bow and thus the negative bow of the initial silicon carbide substrate 410 may be reduced after the SiC epitaxy. In another example, the

initial silicon carbide substrate 410 may have a predetermined negative (concave) substrate bow of about $-7\mu\text{m}$, and the silicon carbide epitaxial wafer 400 with its silicon carbide epitaxial layer 420 formed on such an initial silicon carbide substrate 410 may have a positive (convex) wafer bow of about $+3\mu\text{m}$. In a further example, the initial silicon carbide substrate 410 may have a predetermined negative (concave) substrate bow of about $-5\mu\text{m}$, and the silicon carbide epitaxial wafer 400 with its silicon carbide epitaxial layer 420 formed on such an initial silicon carbide substrate 410 may have a zero wafer bow of $0\mu\text{m}$.

[0072] According to various embodiments, the silicon carbide substrate 410 may include a layer or a region 416 of predetermined dopants at the back surface 414 of the silicon carbide substrate 410. The layer 416 with implanted dopants may expand crystal lattice on the backside of the silicon carbide substrate 410, giving rise to the negative (concave) bow of the silicon carbide substrate 410. As described in various embodiments above, ion implantation may be used to form the predetermined negative substrate bow in the silicon carbide substrate 410 due to the introduction of additional atoms expanding the SiC crystal lattice and crystal amorphization.

[0073] In various embodiments, the predetermined dopants may include at least one of Phosphorus (P), Aluminum (Al), Titanium (Ti), Chromium (Cr), Iron (Fe), Vanadium (V), or Germanium (Ge). In various embodiments, the predetermined dopants may include any other types of dopants which may expand the SiC crystal lattice, e.g., the 4H-SiC crystal lattice.

[0074] In various embodiments, a doping concentration of the predetermined dopants may be in a range between $1 \times 10^{16} \text{cm}^{-3}$ and $1 \times 10^{20} \text{cm}^{-3}$.

[0075] In various embodiments, a depth of the layer of the predetermined dopants may be in a range between $0.1\mu\text{m}$ and $2.0\mu\text{m}$, e.g., between $0.1\mu\text{m}$ and $1.0\mu\text{m}$. In other words, the predetermined dopants may be detected within a depth of about $2.0\mu\text{m}$ from the back surface 414 of the silicon carbide substrate 410, if SiC wafer back thinning is not carried out.

[0076] In an embodiment, the silicon carbide substrate 410 may be a 4H-SiC substrate. In other embodiments, the silicon carbide substrate 410 may have other polytypes, and may be a 3C-SiC or 6H-SiC substrate, for example.

[0077] Since the silicon carbide epitaxial layer 420 is formed on the front surface 412 of the silicon carbide substrate 410 with the predetermined negative substrate bow, formation of SF and BPD may be suppressed in the silicon carbide epitaxial layer 420. Hence, lower densities of SF and BPD defects in the silicon carbide epitaxial layer 420 may be achieved.

[0078] According to various embodiments, a stacking fault (SF) density in the silicon carbide epitaxial layer 420 of the silicon carbide epitaxial wafer 400 may be less than 1.0 per cm^2 . In addition, a density of basal plane dislocation with an extra half-plane (EHP) pointing towards the silicon carbide epitaxial layer (BPD+) may be lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate (BPD-), as illustrated in FIG. 5 below.

[0079] Lower densities of SF and BPD defects in SiC epitaxial layers improve SiC MOSFET chip yield. For a 10 mm^2 chip area, reduction of SF and BPD defect density from 5 cm^{-2} to 1 cm^{-2} may increase the chip yield from 60% to 90%. Higher chip yields result in lower cost of manufacturing per chip. Hence, the silicon carbide epitaxial wafer 400 of various embodiments may be attractive in enabling significantly higher SiC power device chip yield.

[0080] The silicon carbide epitaxial wafer 400 of FIG. 4 may be formed or manufactured using the method of FIG. 1 described in various embodiments above. In further embodiments, the silicon carbide substrate 410 may be formed or prepared using the method of FIG. 3 described in various embodiments above.

[0081] FIG. 5 shows a schematic illustrating basal plane dislocations in a silicon carbide epitaxial wafer 500 according to various embodiments. Many of the aspects of FIG. 5 are the same or similar to those described with reference to the silicon carbide epitaxial wafer of

FIG. 4. It will be understood that the descriptions of any feature and/or property relating to FIG. 5 that are the same or similar to a feature and/or property in FIG. 4 will have those descriptions be applicable hereinbelow as well.

[0082] As illustrated in FIG. 5, a silicon carbide epitaxial wafer 500 includes a silicon carbide substrate 510 and a silicon carbide epitaxial layer 520 on a front surface of the silicon carbide substrate. In the silicon carbide epitaxial wafer 500, a density of basal plane dislocation with an extra half-plane (EHP) pointing towards the silicon carbide epitaxial layer (BPD+) 522 may be lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate (BPD-) 524. A stacking fault density in the silicon carbide epitaxial layer 520 may be less than 1.0 per cm^2 .

[0083] The stress state in the silicon carbide epitaxial layer may be defined as the difference in density of BPD, including partial dislocations, having an extra half-plane (EHP) pointing towards the epilayer surface (BPD+) and those with an EHP pointing towards the substrate (BPD-). If the SiC epilayer is under the tensile stress state condition, the density of BPD- may be always larger than that of BPD+. Tensile film stress in the silicon carbide epitaxial layer may indicate that negative (concave) substrate bow was applied prior to epitaxy.

[0084] When the silicon carbide epitaxial wafer 500 is formed according to the method of FIG. 1 above which may be subsequently fabricated into silicon carbide MOSFET chips, the silicon carbide epitaxial layer 520 in the silicon carbide epitaxial wafer 500 and the silicon carbide MOSFET chip may satisfy both conditions: 1) stacking fault density < 1.0 per cm^2 and 2) density of BPD+ $<$ density of BPD-. The densities of BPD+ and BPD- in the silicon carbide epitaxial layer may be measured using synchrotron X-ray topography.

[0085] FIG. 6 shows a) a plot of BPD density (in cm^{-2}) as a function of a SiC substrate bow (in micrometers or μm) illustrating the experiment results of the present disclosure; b) a plot of SF density (in cm^{-2}) as a function of a SiC substrate bow (in micrometers or μm); c) a

plot of BPD density (in cm^{-2}) as a function of a SiC epitaxial wafer bow (in micrometers or μm) after epitaxy; d) a plot of SF density (in cm^{-2}) as a function of a SiC epitaxial wafer bow (in micrometers or μm) after epitaxy; e) a plot of BPD density (in cm^{-2}) as a function of a bow change from epitaxy (in micrometers or μm) ; and f) a plot of SF density (in cm^{-2}) as a function of a bow change from epitaxy (in micrometers or μm); illustrating the experiment results of the present disclosure.

[0086] In the experiment of the present disclosure, 32 SiC substrates with both negative substrate bow and positive bow are provided. The negative substrate bow values of the SiC substrates may be in a range from $-15\mu\text{m}$ to 0 (flat substrate), and may be mainly localized around $-3\mu\text{m}$, as shown in FIG. 6 a) and FIG. 6 b). The positive substrate bow values of the SiC substrates may be localized around $+3\mu\text{m}$, and may have a maximum bow value of $+7\mu\text{m}$ in this batch of SiC substrates. The SiC substrates may be provided with pre-existing substrate bows. The SiC substrates with negative substrate bow may be prepared according to the method of FIG. 3 in various embodiments above.

[0087] Positive correlations between the bow values and the BPD/SF densities were observed in all cases. As illustrated in FIG. 6 a) and FIG. 6 b), SiC substrates with positive (convex) wafer bow give higher BPD and SF densities. Further, SiC epitaxial wafers with positive (convex) wafer bow give higher BPD and SF densities as illustrated in FIG. 6 c) and FIG. 6 d). A higher bow change Δbow from epitaxy also give higher BPD and SF densities as illustrated in FIG. 6 e) and FIG. 6 f). These observations are in agreement with the finding of the present disclosure that SiC epitaxy on substrates with positive bow enhances the formation of SF and BPD defects (with pre-existing substrate stress acting in the same direction as epitaxy misfit stress), and that SiC epitaxy on substrates with negative bow as provided in various embodiments of the present disclosure suppresses the formation of SF and BPD defects (with pre-existing substrate stress counteracting epitaxy misfit stress).

[0088] In a further aspect as shown in FIG. 6 c) and FIG. 6 d), the negative bow in the SiC epiwafers after epitaxy may be decreased by about 5 μ m to 10 μ m. Some of the SiC epiwafers may have positive bow after epitaxy on the SiC substrates with negative bow. The bow change in the SiC epiwafers may show that epitaxial growth may induce positive bow. It is also observed that SiC substrates with **high positive (convex) bow values also result in high Δ bow** and epiwafer bow values. In other words, it may be more likely for SiC substrates with high positive (convex) bow values to take on even higher bow values after epitaxy.

[0089] The experiment results show that SiC epitaxy on substrates with negative bow as provided in various embodiments of the present disclosure may provide a silicon carbide epitaxial wafer with lower densities of SF and BPD defects.

[0090] According to various embodiments, a silicon carbide epitaxial wafer may be provided. The silicon carbide epitaxial wafer may include a silicon carbide substrate; and a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate, wherein the silicon carbide epitaxial layer is formed on the silicon carbide substrate having a predetermined negative substrate bow.

[0091] According to various embodiments, a silicon carbide epitaxial wafer may be provided. The silicon carbide epitaxial wafer may include a silicon carbide substrate; and a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate. The silicon carbide substrate may include a layer of predetermined dopants at a back surface of the silicon carbide substrate.

[0092] According to various embodiments, a silicon carbide epitaxial wafer may be provided. The silicon carbide epitaxial wafer may include a silicon carbide substrate; and a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate. A stacking fault density in the silicon carbide epitaxial layer of the silicon carbide epitaxial wafer may be less than 1.0 per cm². A density of basal plane dislocation with an extra half-plane (EHP)

pointing towards the silicon carbide epitaxial layer (BPD+) may be lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate (BPD-).

[0093] By “comprising” it is meant including, but not limited to, whatever follows the word “comprising”. Thus, use of the term “comprising” indicates that the listed elements are required or mandatory, but that other elements are optional and may or may not be present.

[0094] By “consisting of” is meant including, and limited to, whatever follows the phrase “consisting of”. Thus, the phrase “consisting of” indicates that the listed elements are required or mandatory, and that no other elements may be present.

[0095] The inventions illustratively described herein may suitably be practiced in the absence of any element or elements, limitation or limitations, not specifically disclosed herein. Thus, for example, the terms “comprising”, “including”, “containing”, etc. shall be read expansively and without limitation. Additionally, the terms and expressions employed herein have been used as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding any equivalents of the features shown and described or portions thereof, but it is recognized that various modifications are possible within the scope of the invention claimed. Thus, it should be understood that although the present invention has been specifically disclosed by preferred embodiments and optional features, modification and variation of the inventions embodied therein herein disclosed may be resorted to by those skilled in the art, and that such modifications and variations are considered to be within the scope of this invention.

[0096] By “about” in relation to a given numerical value, such as for temperature and period of time, it is meant to include numerical values within 10% of the specified value.

[0097] The invention has been described broadly and generically herein. Each of the narrower species and sub-generic groupings falling within the generic disclosure also form part

of the invention. This includes the generic description of the invention with a proviso or negative limitation removing any subject matter from the genus, regardless of whether or not the excised material is specifically recited herein.

[0098] Other embodiments are within the following claims and non-limiting examples. In addition, where features or aspects of the invention are described in terms of Markush groups, those skilled in the art will recognize that the invention is also thereby described in terms of any individual member or subgroup of members of the Markush group.

[0099] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

What is claimed is:

1. A method of forming a silicon carbide epitaxial wafer, the method comprising:
providing a silicon carbide substrate with a predetermined negative substrate bow; and
forming a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate.
2. The method according to claim 1, wherein the predetermined negative substrate bow is in a range between $-15\mu\text{m}$ and $0\mu\text{m}$.
3. The method according to claim 1, further comprising:
forming the silicon carbide substrate with the predetermined negative substrate bow by ion implantation.
4. The method according to claim 3, wherein at least one of a dose, an energy or a type of dopants for the ion implantation is determined based on the predetermined negative substrate bow.
5. The method according to claim 3, further comprising:
conducting the ion implantation of predetermined dopants on a back surface of the silicon carbide substrate to form a layer of the predetermined dopants at the back surface of the silicon carbide substrate, thereby forming the silicon carbide substrate with the predetermined negative substrate bow.

6. The method according to claim 5, further comprising:
forming a protective layer on the front surface of the silicon carbide substrate before conducting the ion implantation; and
removing the protective layer from the front surface of the silicon carbide substrate after conducting the ion implantation.
7. The method according to claim 5, wherein the ion implantation is conducted at temperatures between room temperature and 650°C.
8. The method according to claim 5, wherein the predetermined dopants comprise at least one of Phosphorus, Aluminum, Titanium, Chromium, Iron, Vanadium, or Germanium.
9. The method according to claim 5, wherein a doping concentration of the predetermined dopants is in a range between $1 \times 10^{16} \text{cm}^{-3}$ and $1 \times 10^{20} \text{cm}^{-3}$.
10. The method according to claim 5, wherein a depth of the layer of the predetermined dopants is in a range between 0.1 μm and 2.0 μm .
11. The method according to claim 1, wherein a stacking fault density in the silicon carbide epitaxial layer is less than 1.0 per cm^2 , and wherein a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide epitaxial layer is lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate.

12. A method of preparing a substrate, the method comprising:
 - forming a protective layer on a front surface of a silicon carbide substrate;
 - conducting an ion implantation of predetermined dopants on a back surface of the silicon carbide substrate, thereby forming the silicon carbide substrate with a predetermined negative substrate bow; and
 - removing the protective layer from the front surface of the silicon carbide substrate.
13. The method according to claim 12, wherein the protective layer comprises silicon dioxide or silicon nitride.
14. The method according to claim 12, wherein at least one of a dose, an energy or a type of dopants for the ion implantation is determined based on the predetermined negative substrate bow.
15. A silicon carbide epitaxial wafer, comprising:
 - a silicon carbide substrate; and
 - a silicon carbide epitaxial layer on a front surface of the silicon carbide substrate, wherein the silicon carbide epitaxial layer is formed on the silicon carbide substrate having a predetermined negative substrate bow.
16. The silicon carbide epitaxial wafer according to claim 15, wherein the predetermined negative substrate bow is in a range between $-15\mu\text{m}$ and $0\mu\text{m}$.

17. The silicon carbide epitaxial wafer according to claim 15, wherein the silicon carbide substrate comprises a layer of predetermined dopants at a back surface of the silicon carbide substrate.
18. The silicon carbide epitaxial wafer according to claim 17, wherein the predetermined dopants comprise at least one of Phosphorus, Aluminum, Titanium, Chromium, Iron, Vanadium, or Germanium.
19. The silicon carbide epitaxial wafer according to claim 17, wherein a depth of the layer of predetermined dopants is in a range between 0.1 μm and 2.0 μm .
20. The silicon carbide epitaxial wafer according to claim 15, wherein a stacking fault density in the silicon carbide epitaxial layer is less than 1.0 per cm^2 , and
wherein a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide epitaxial layer is lower than a density of basal plane dislocation with an extra half-plane pointing towards the silicon carbide substrate.