

FIG. 1A
Prior Art

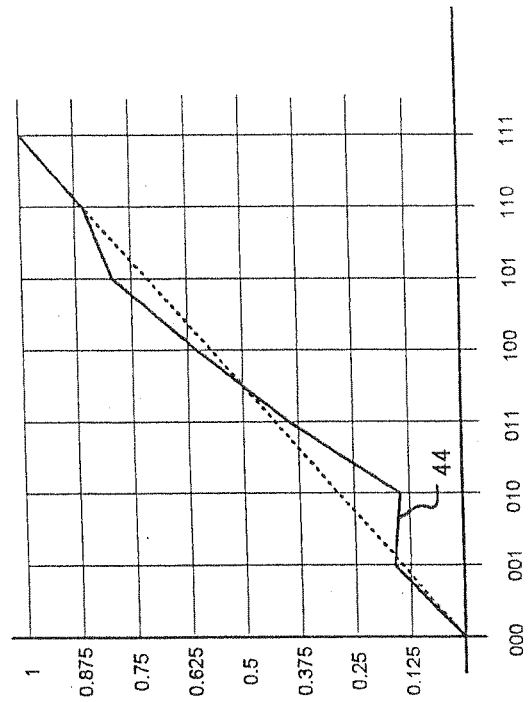
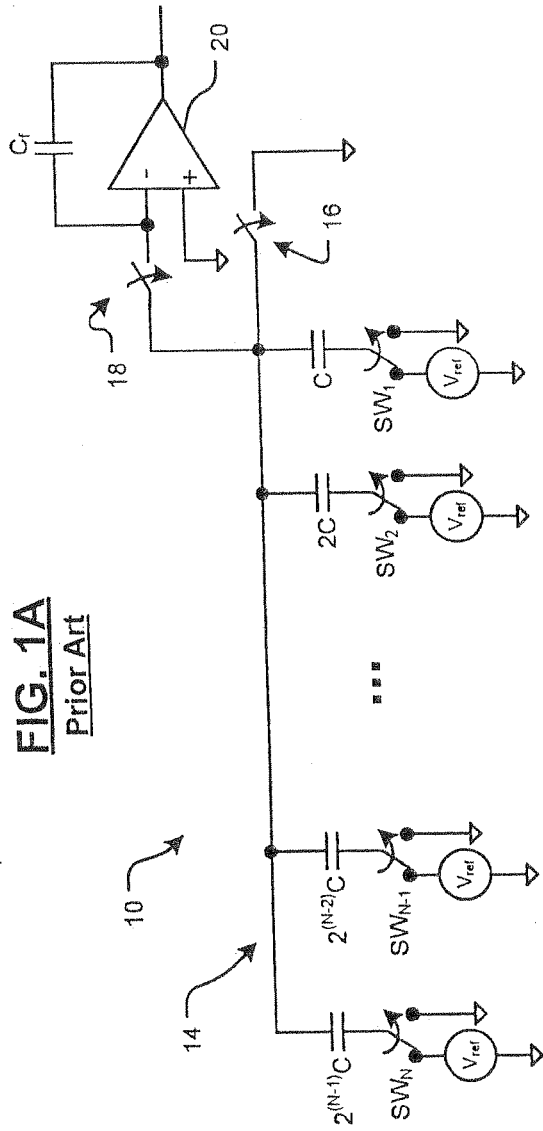


FIG. 1B
Prior Art

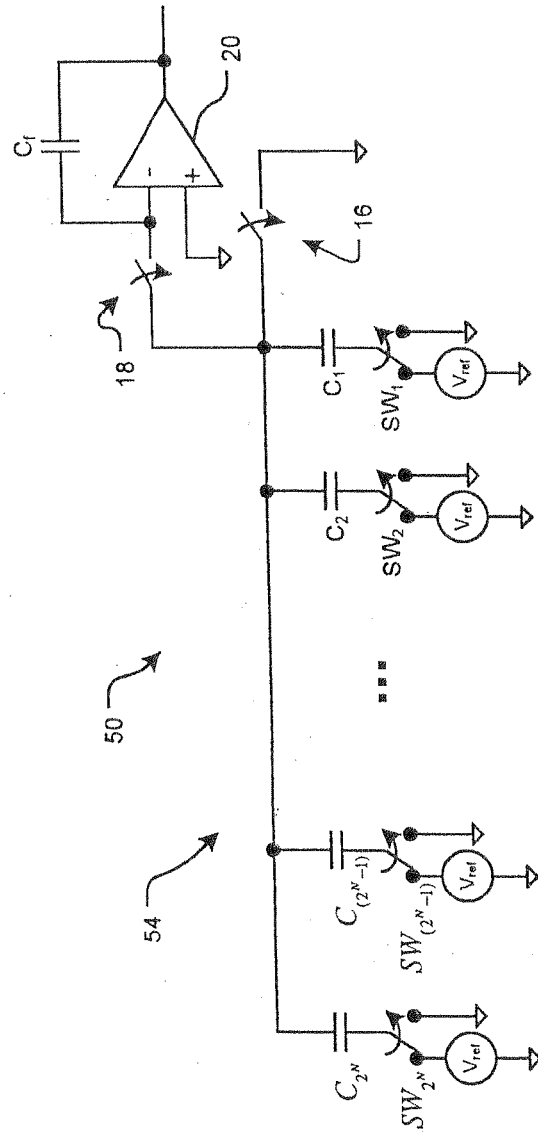
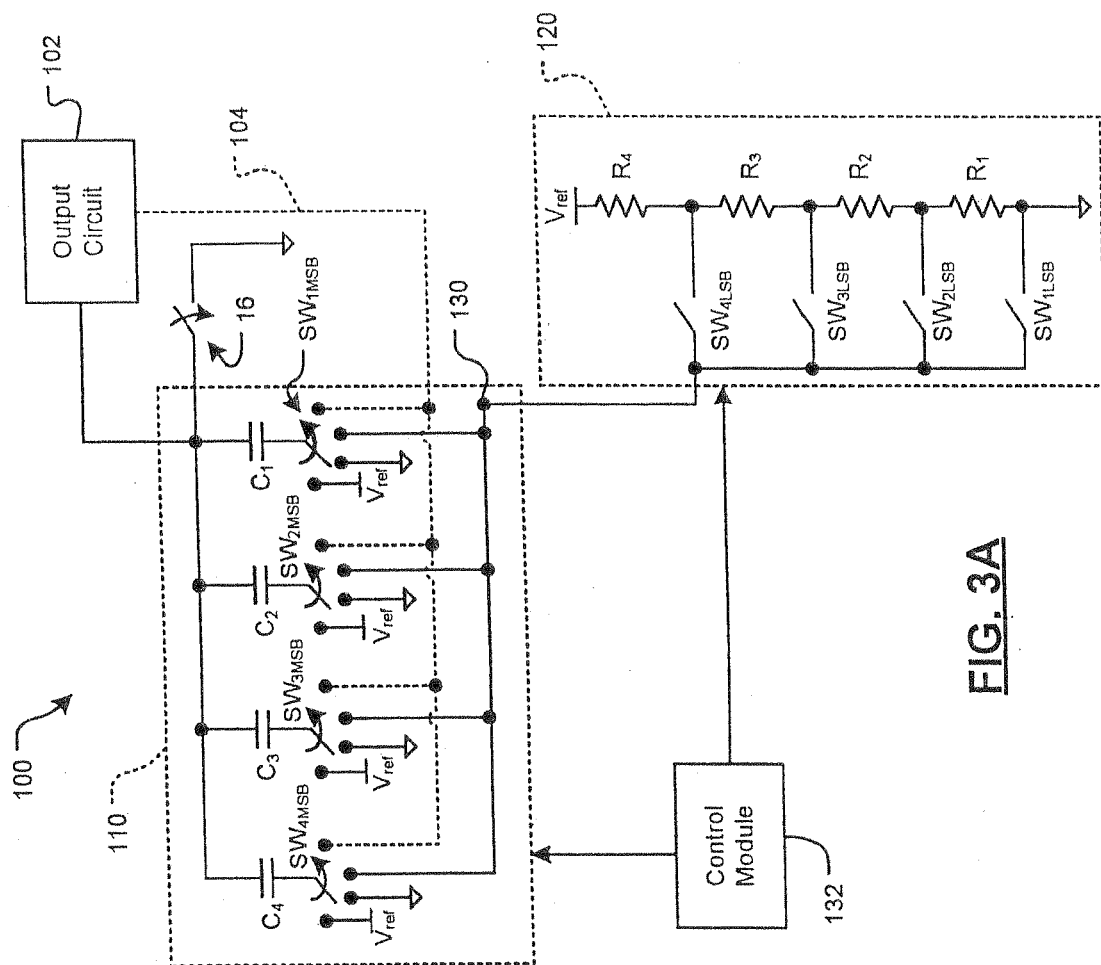
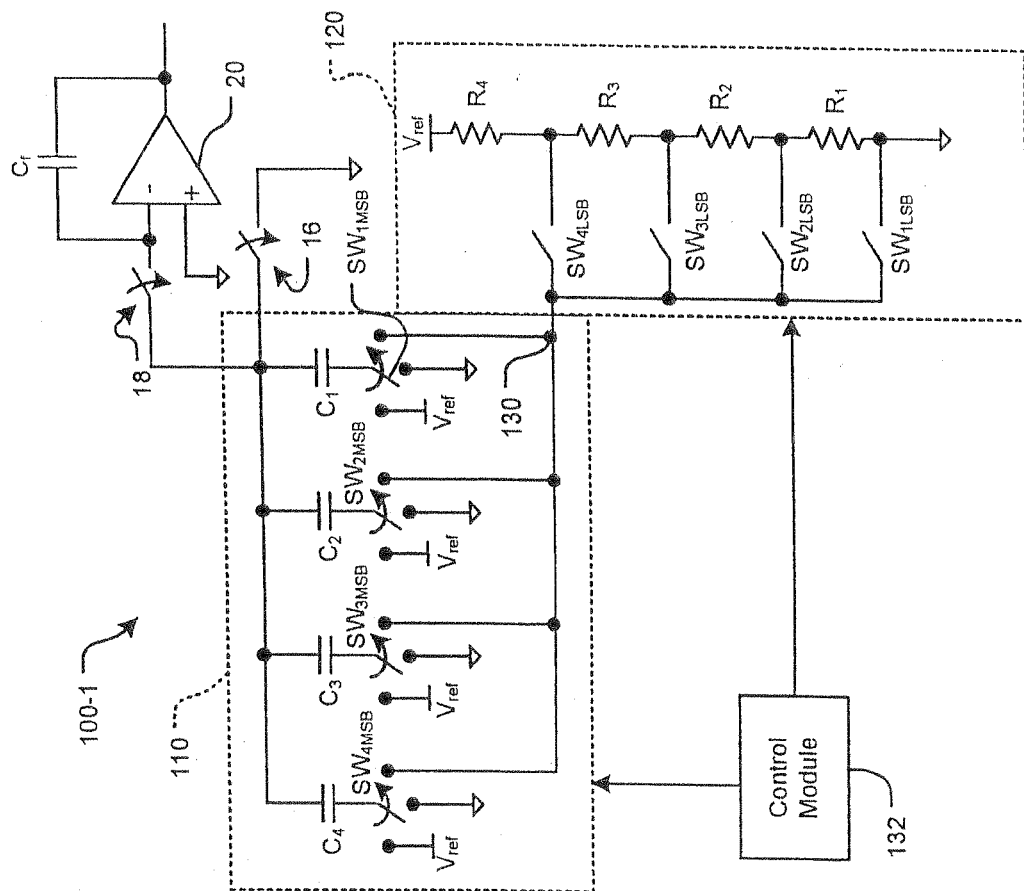


FIG. 2
Prior Art

**FIG. 3A**

**FIG. 3B**

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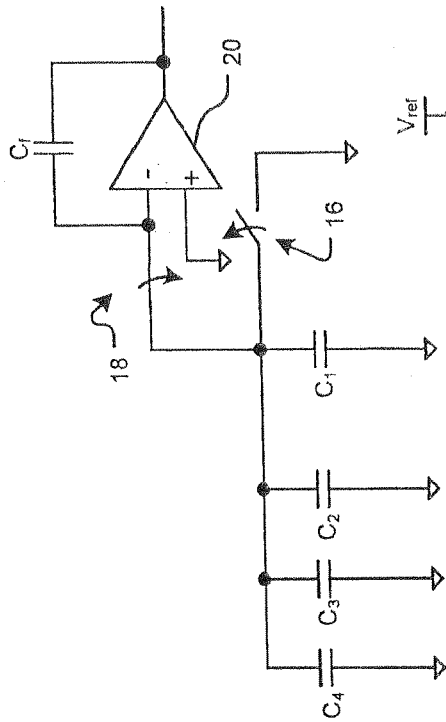
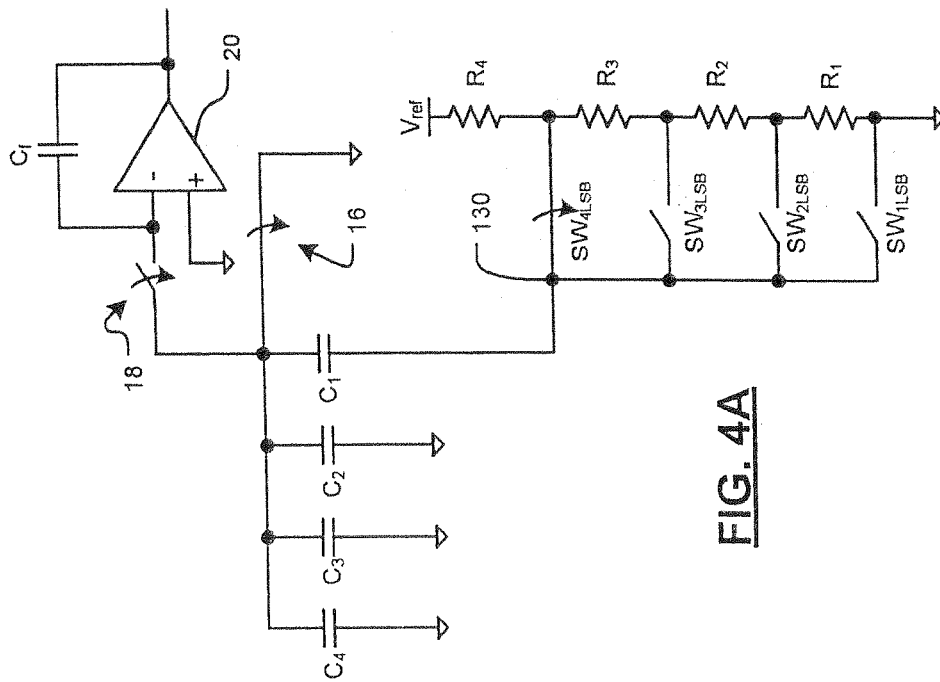
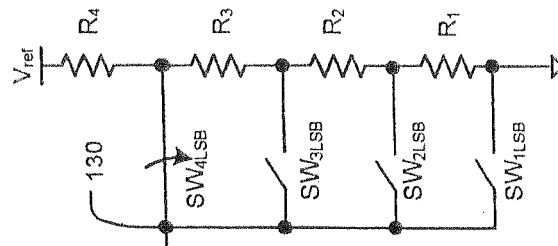
**FIG. 4B****FIG. 4A**

FIG. 4C

Code Switch		Switch Positions							
		[0000-0011]	[0000-0011]	[0100-0111]	[0100-0111]	[1000-1011]	[1000-1011]	[1100-1111]	[1100-1111]
MSB 2 bits	SW4MSB	G	G	G	G	G	G	C	G
	SW3MSB	G	G	G	G	C	G	V	G
	SW2MSB	G	G	C	G	V	G	V	G
	SW1MSB	C	G	V	G	V	G	V	G
LSB 2 bits	SW4LSB	O	O	O	O	O	O	O	O
	SW3LSB	O	O	O	O	O	O	O	O
	SW2LSB	O	O	O	O	O	O	O	O
	SW1LSB	C	O	O	O	O	O	O	O

$V = V_{ref}$
 C = Node 130
 G = Ground
 O = Open
 C = Closed

FIG. 4D

Code Switch		Switch Positions							
		[0000-0011]	[0000-0011]	[0100-0111]	[0100-0111]	[1000-1011]	[1000-1011]	[1100-1111]	[1100-1111]
MSB 2 bits	SW4MSB	G	A	G	A	G	A	C	A
	SW3MSB	G	A	G	A	C	A	V	A
	SW2MSB	G	A	C	A	V	A	V	A
	SW1MSB	C	A	V	A	V	A	V	A
LSB 2 bits	SW4LSB	O	O	O	O	O	O	O	O
	SW3LSB	O	O	O	O	O	O	O	O
	SW2LSB	O	O	O	O	O	O	O	O
	SW1LSB	C	O	O	O	O	O	O	O

$V = V_{ref}$
 C = Node 130
 G = Ground
 O = Open
 C = Closed
 A = Amp Output

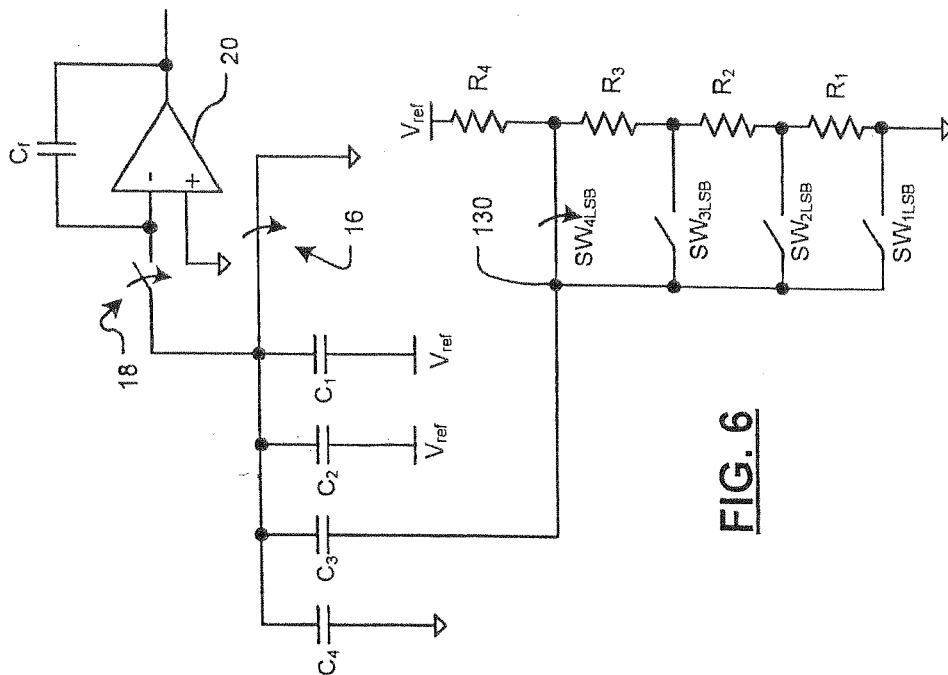


FIG. 5

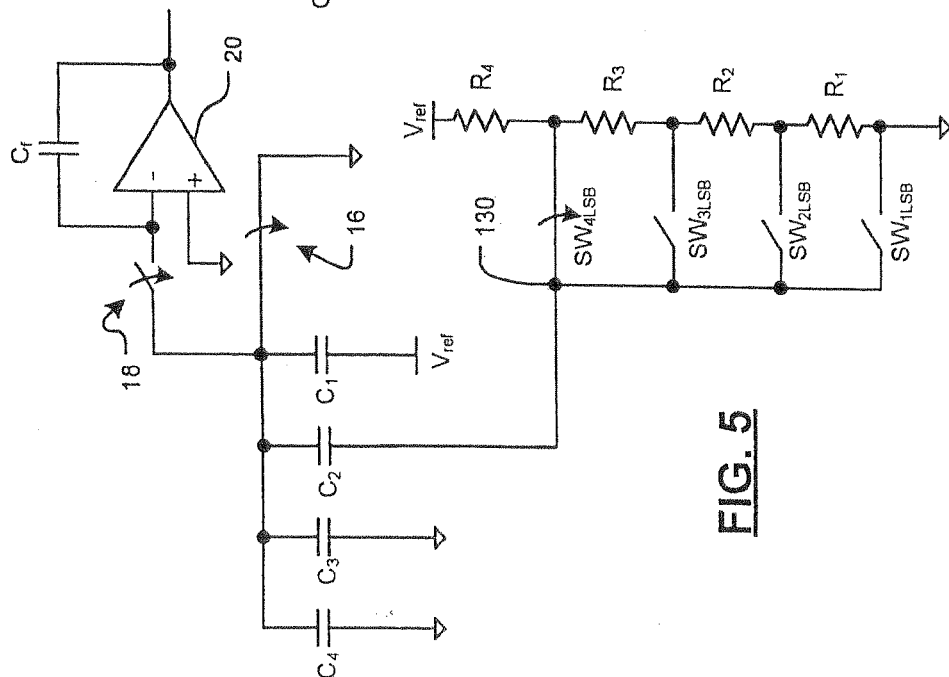


FIG. 6

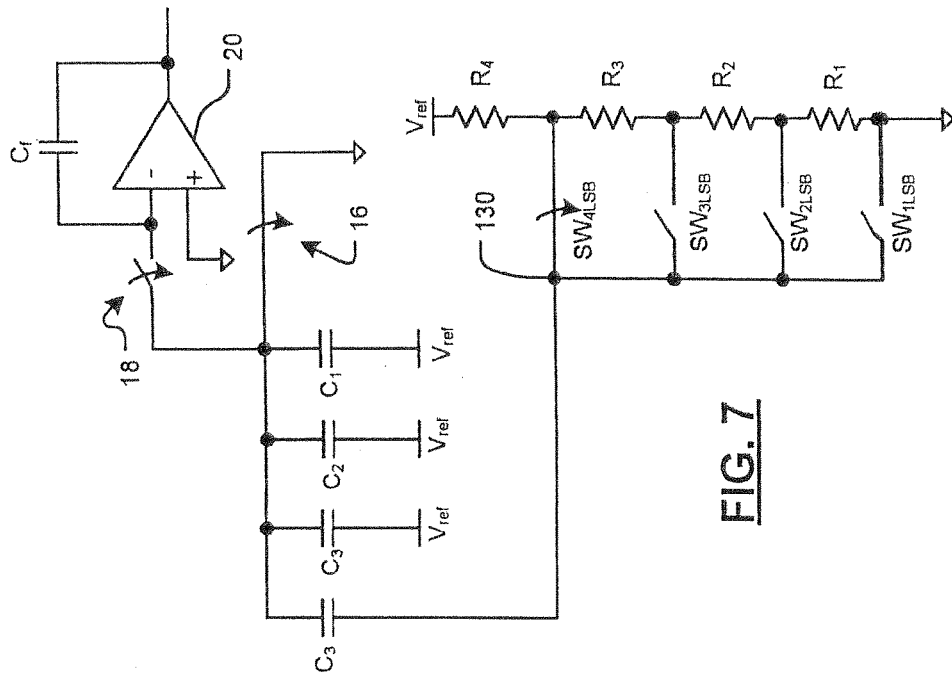
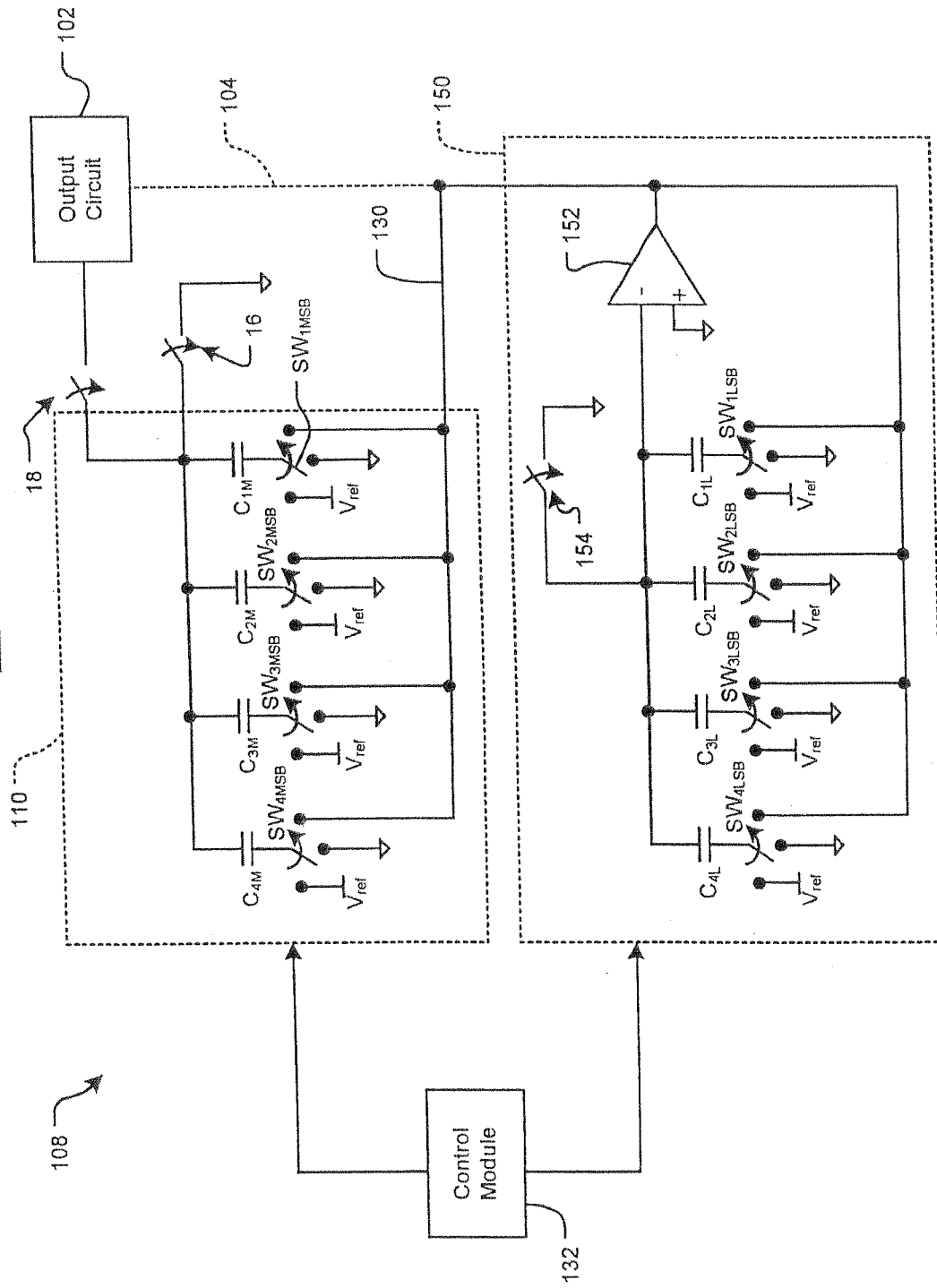
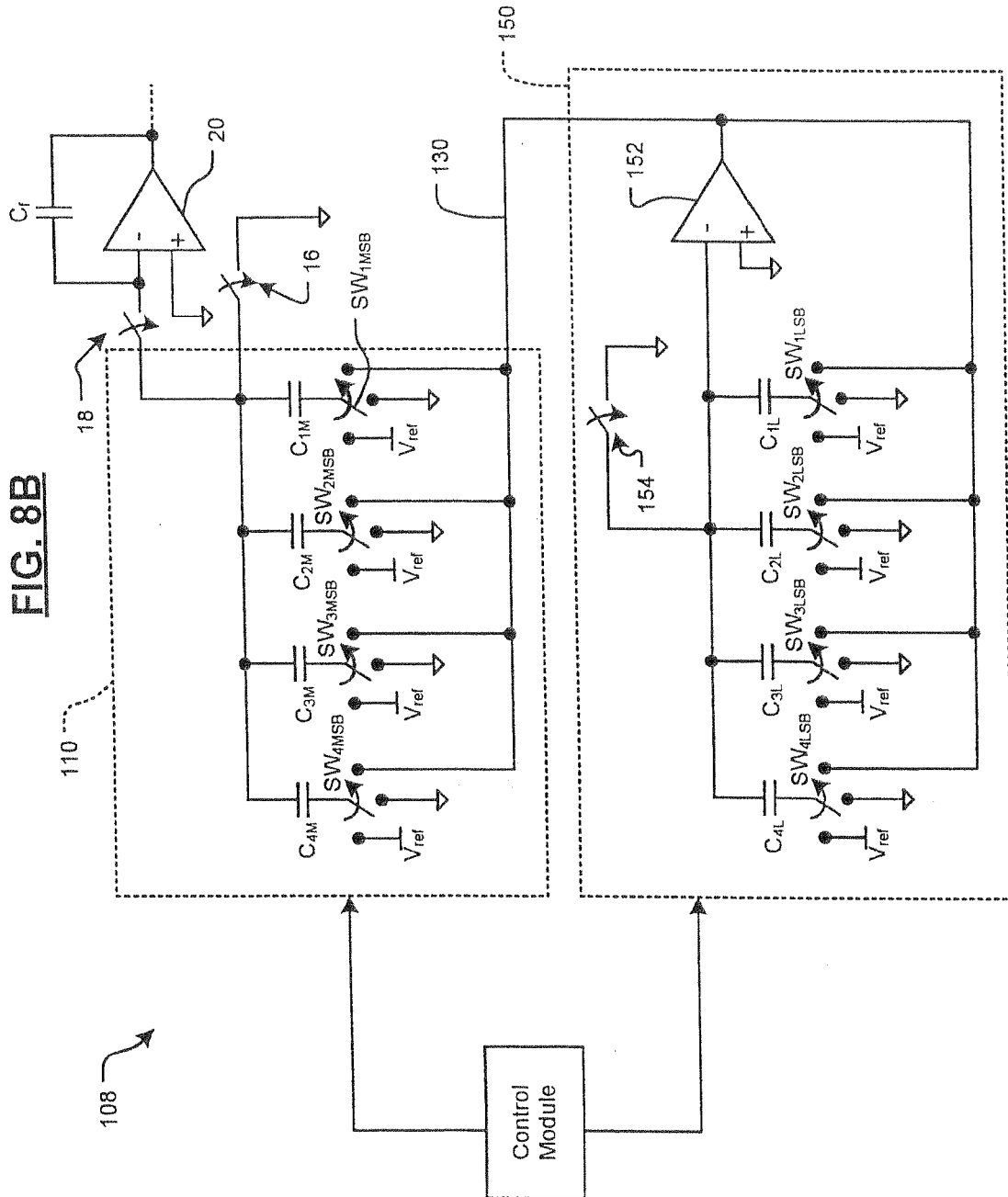
**FIG. 7**

FIG. 8A



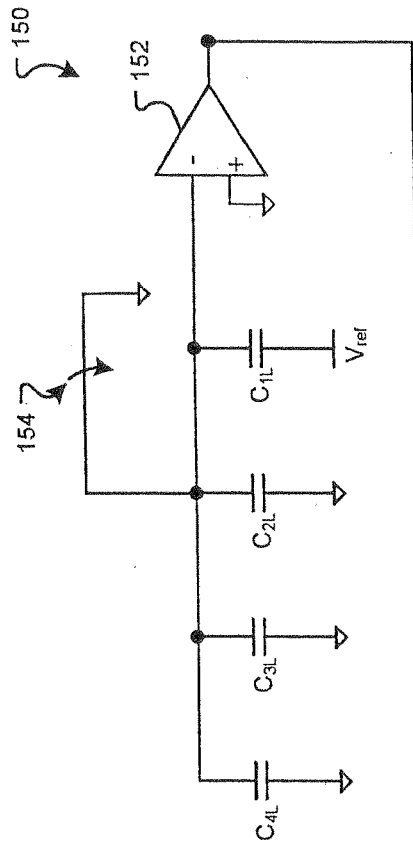


FIG. 8C

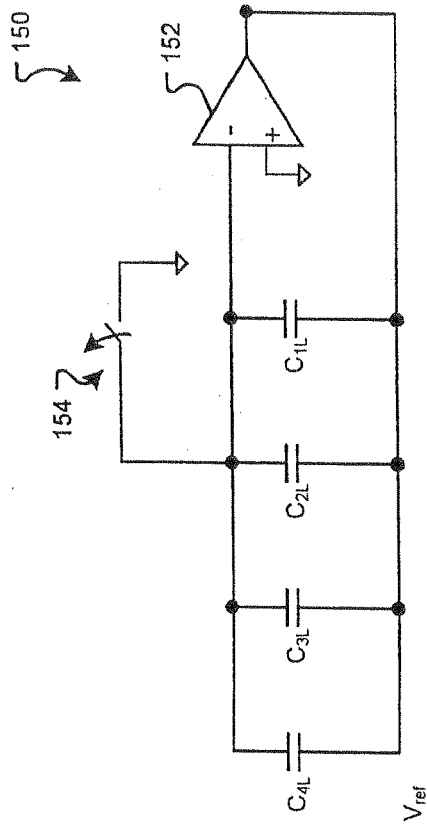


FIG. 8D

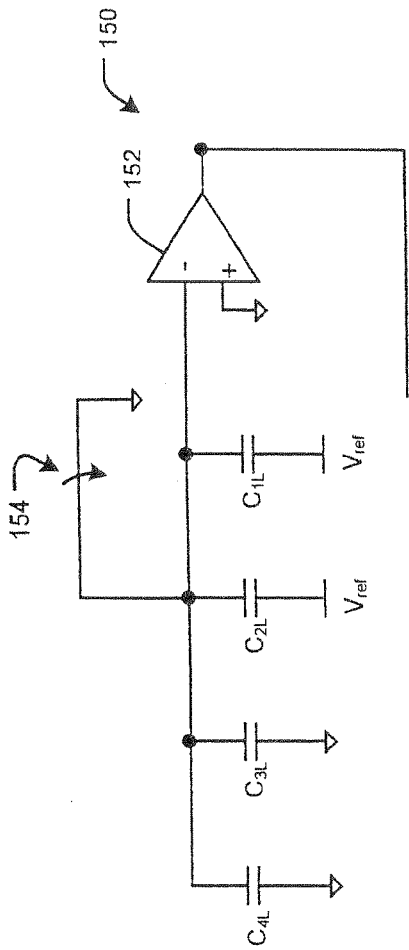


FIG. 8E

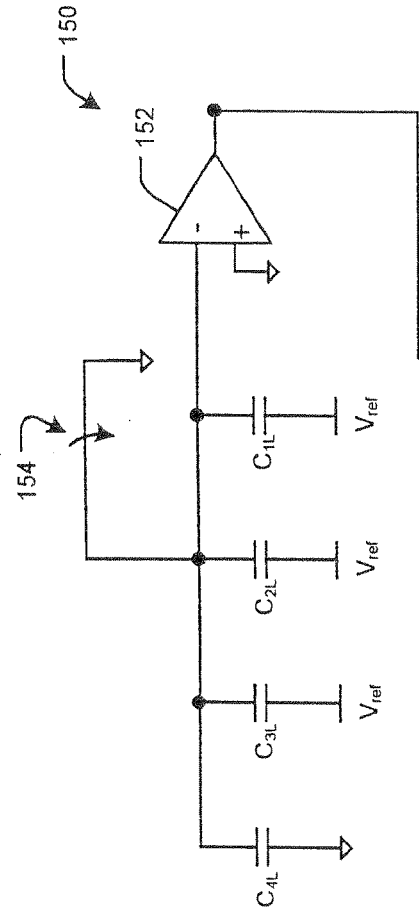


FIG. 8F

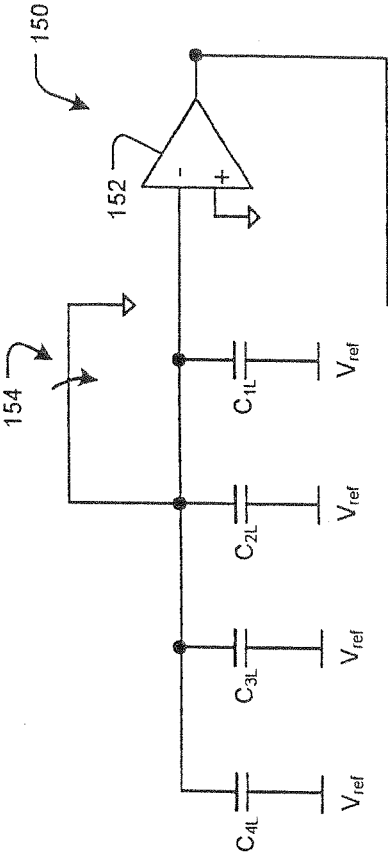
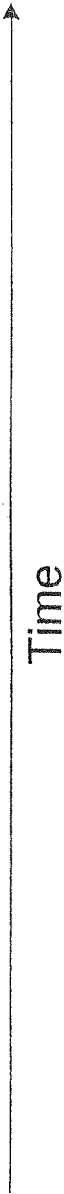


FIG. 8G

Sample L	Integ L	Sample M	Integ M	Sample L	Integ L	Sample M	Integ M
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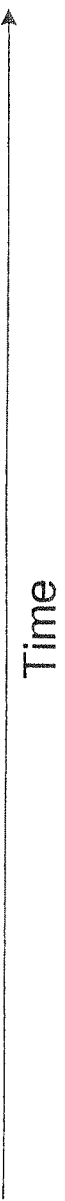
FIG. 8H



Sample L	Integ L	Sample M	Integ M
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Sample L	Integ L	Sample M	Integ M
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FIG. 8I



Code		Switch Positions											
Switch		[0000-0011]						[0100-0111]					
		Sample-LSB	Hold-LSB	Sample-MSB	I or H-MSB	Sample-LSB	Hold-LSB	Sample-MSB	I or H-MSB	Sample-LSB	Hold-LSB	Sample-MSB	I or H-MSB
MSB 2 bits	SW4MSB	G	G	G	G or A	G	G	G	G or A	G	G	G	G or A
	SW3MSB	G	G	G	G or A	G	G	G	G or A	G	G	G	G or A
	SW2MSB	G	G	G	G or A	G	G	G	G or A	G	G	C	G or A
	SW1MSB	G	G	C	G or A	G	G	V	G or A	G	G	V	G or A
LSB 2 bits	SW4LSB	G	G	F	X	F	X	G	X	X	X	F	X
	SW3LSB	G	G	F	X	F	X	G	X	X	X	F	X
	SW2LSB	G	G	F	X	F	X	G	X	X	X	F	X
	SW1LSB	G	G	F	X	F	X	G	X	X	X	F	X
		0 to 0.75Vref						Vref to 1.75Vref					
Code		Switch Positions											
Switch		[1000-1011]						[11100-1111]					
		Sample-LSB	Hold-LSB	Sample-MSB	I or H-MSB	Sample-LSB	Hold-LSB	Sample-MSB	I or H-MSB	Sample-LSB	Hold-LSB	Sample-MSB	I or H-MSB
MSB 2 bits	SW4MSB	G	G	G	G or A	G	G or A	G	G or A	G	G	C	G or A
	SW3MSB	G	G	C	G or A	G	G or A	G	G or A	G	G	V	G or A
	SW2MSB	G	G	V	G or A	G	G or A	G	G or A	G	G	V	G or A
	SW1MSB	G	G	V	G or A	G	G or A	G	G or A	G	G	V	G or A
LSB 2 bits	SW4LSB	G	G	F	X	F	X	G	X	F	F	F	X
	SW3LSB	G	G	F	X	F	X	G	X	F	F	F	X
	SW2LSB	G	G	F	X	F	X	G	X	F	F	F	X
	SW1LSB	G	G	F	X	F	X	G	X	F	F	F	X
		2Vref to 2.75Vref						3Vref to 3.75Vref					

$V = V_{ref}$
 C = Node 130
 G = Ground
 F = Feedback
 X = Don't Care
 A = Amp Output

FIG. 8J

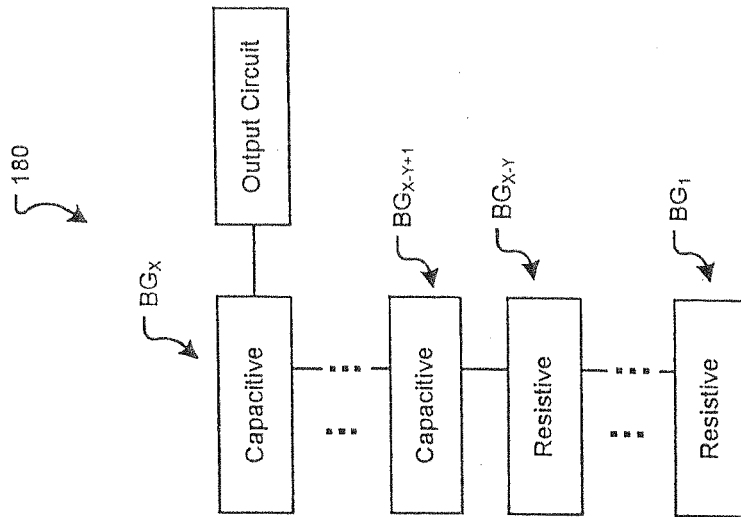


FIG. 9B

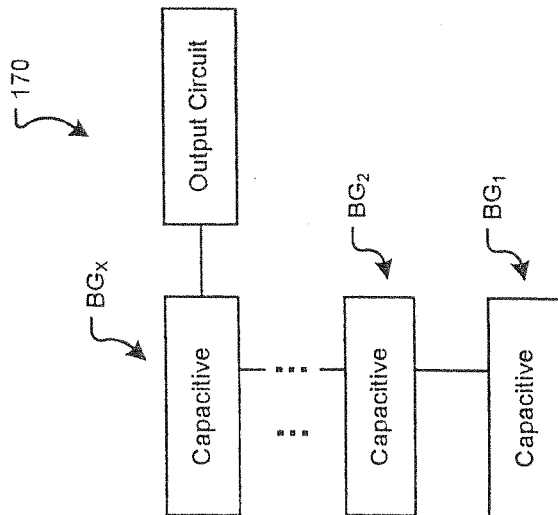


FIG. 9A

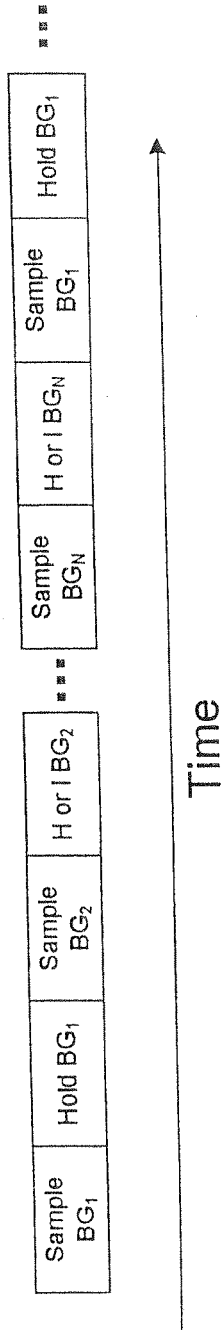


FIG. 9C

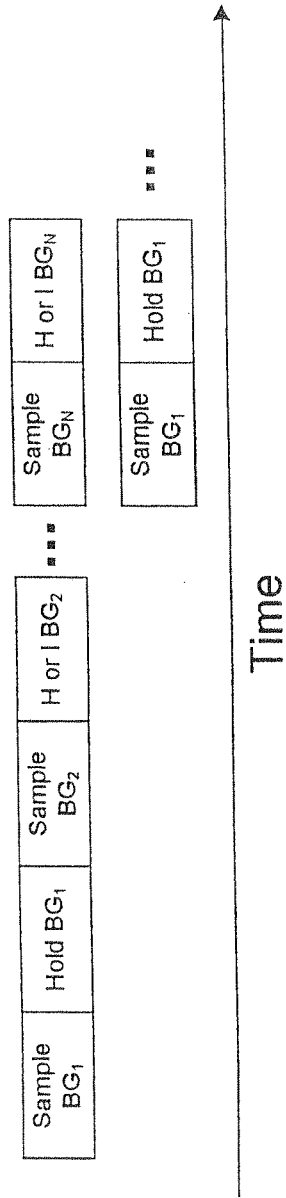


FIG. 9D

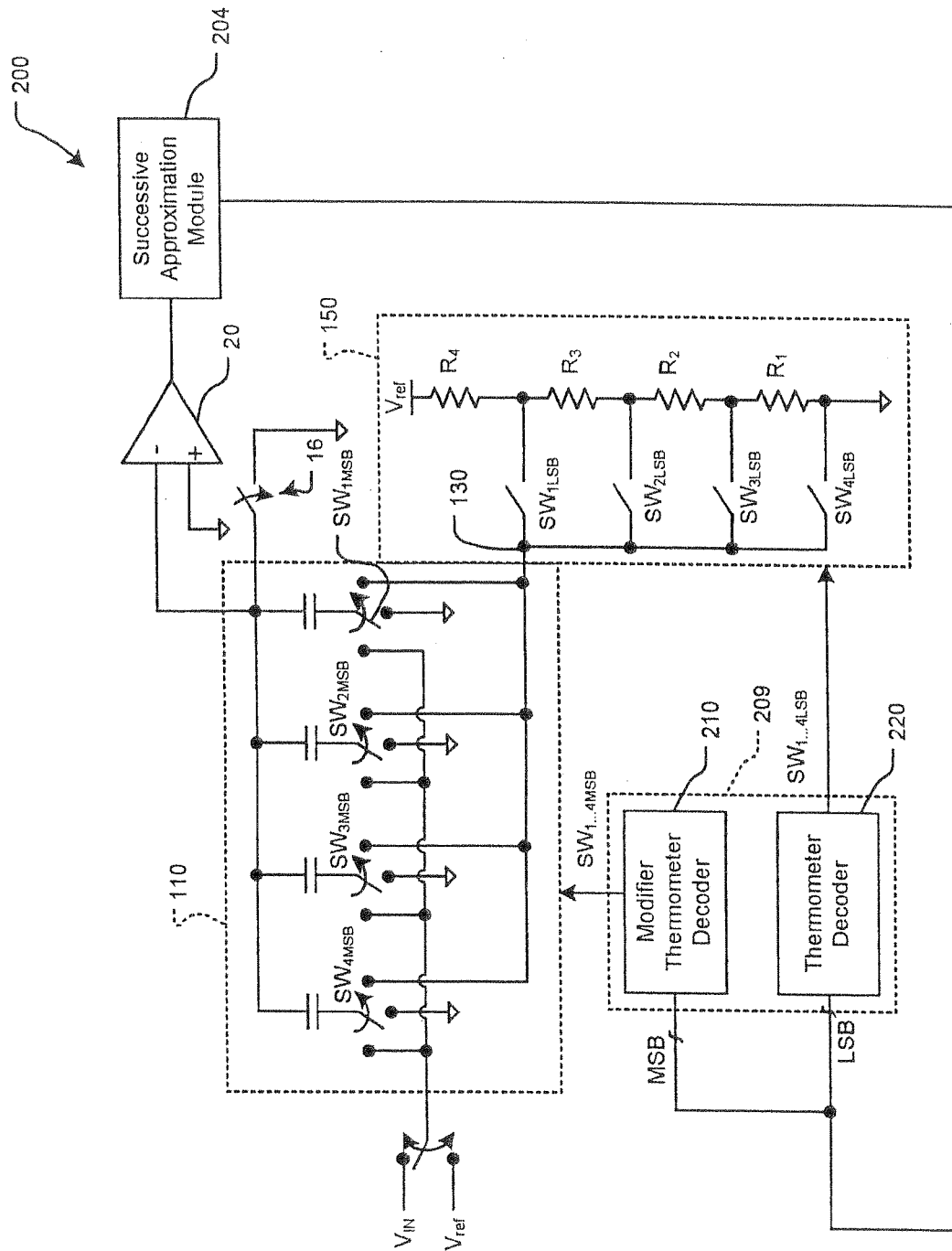


FIG. 10

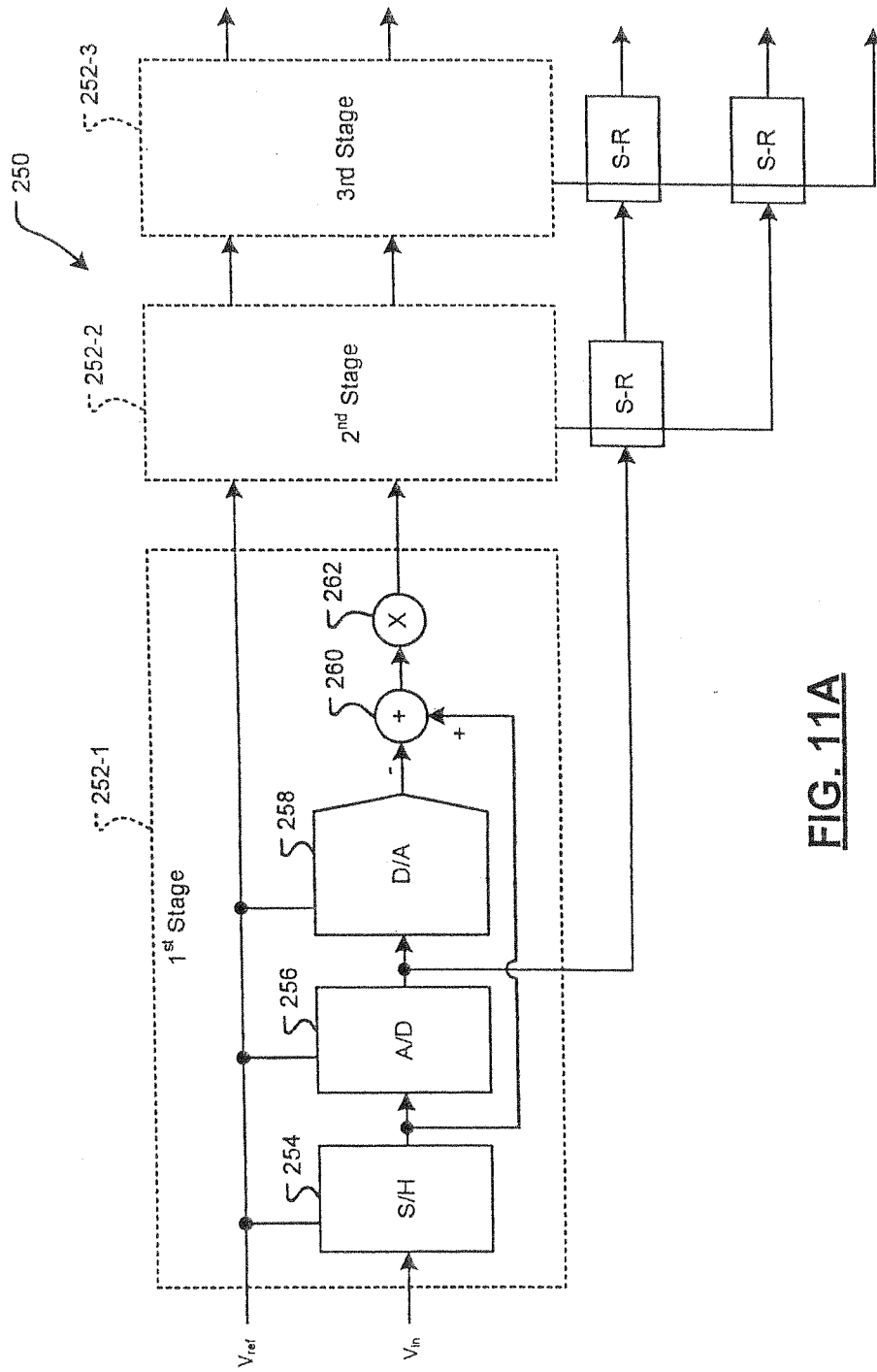


FIG. 11A

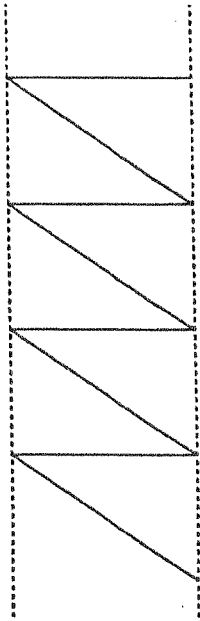


FIG. 11B

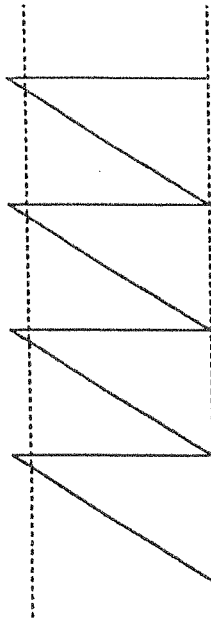


FIG. 11C

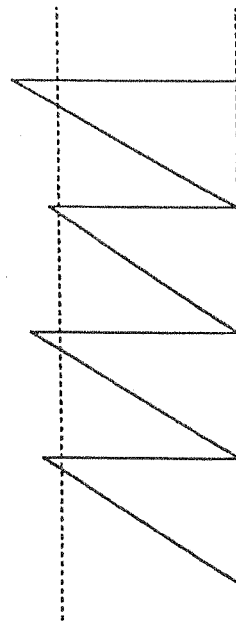


FIG. 11D

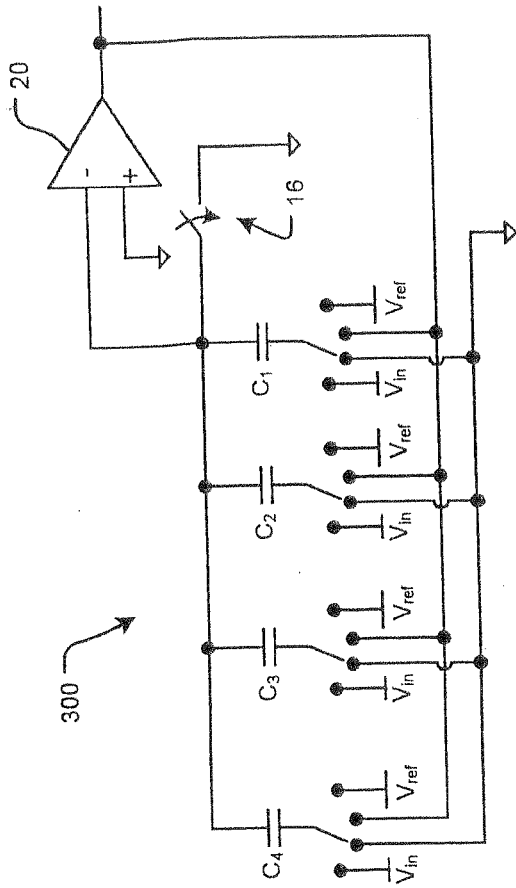


FIG. 12A

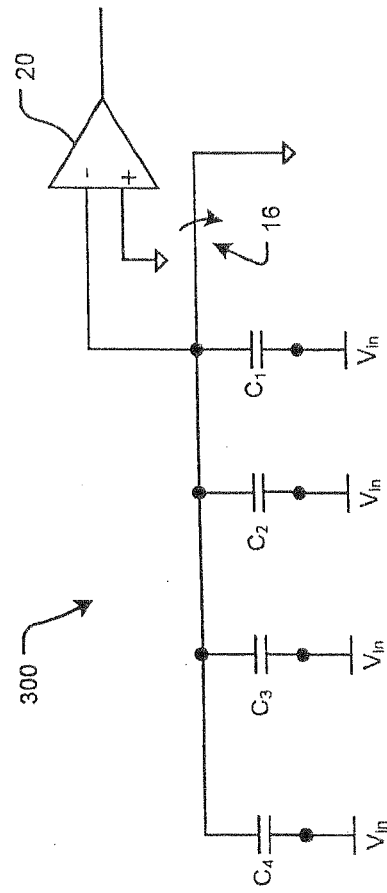


FIG. 12B

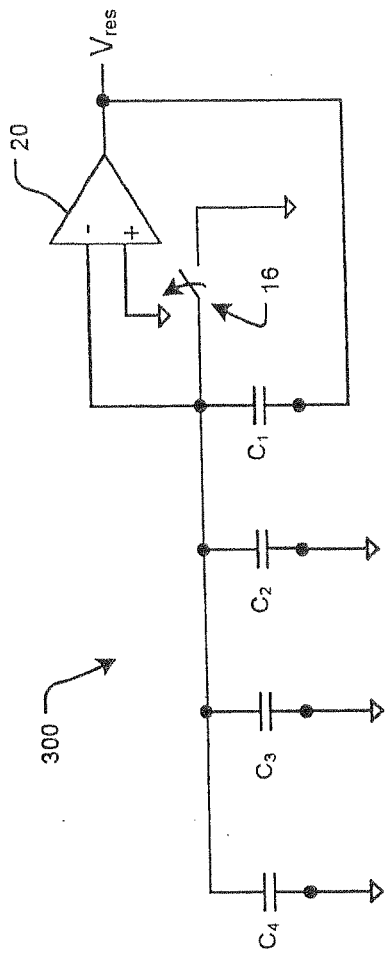


FIG. 12C

Switch Positions											
Switch	A		B		C		D		E		F
	Sample	Residue Amp	Sample	Residue Amp	Sample	Residue Amp	Sample	Residue Amp	Sample	Residue Amp	
4	Vin	G	Vin	G	Vin	G	Vin	G	Vin	F	
3	Vin	G	Vin	G	Vin	F	Vin	Vref	Vin	Vref	
2	Vin	G	Vin	F	Vin	Vref	Vin	Vref	Vin	Vref	
1	Vin	F	Vin	Vref	Vin	Vref	Vin	Vref	Vin	Vref	

V_{in} = input voltage
 G = Ground
 V_{ref} = reference voltage
 F = Feedback

FIG. 12D

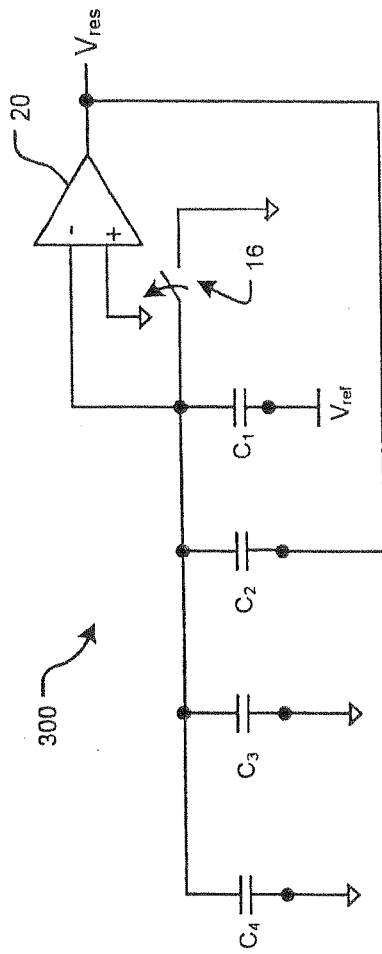


FIG. 13

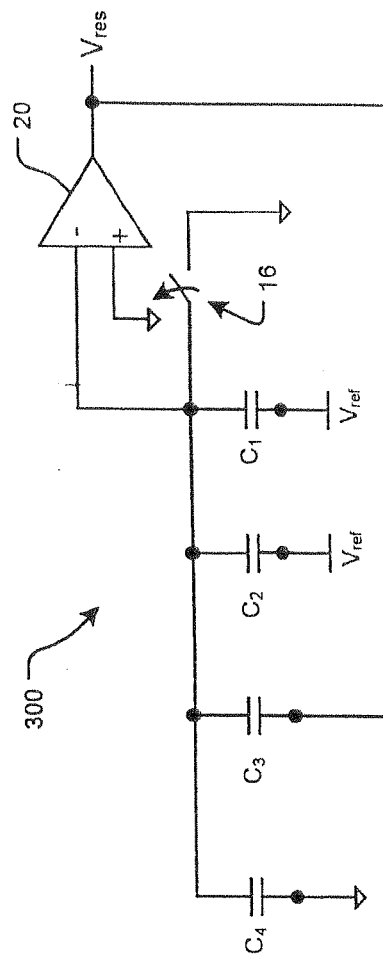


FIG. 14

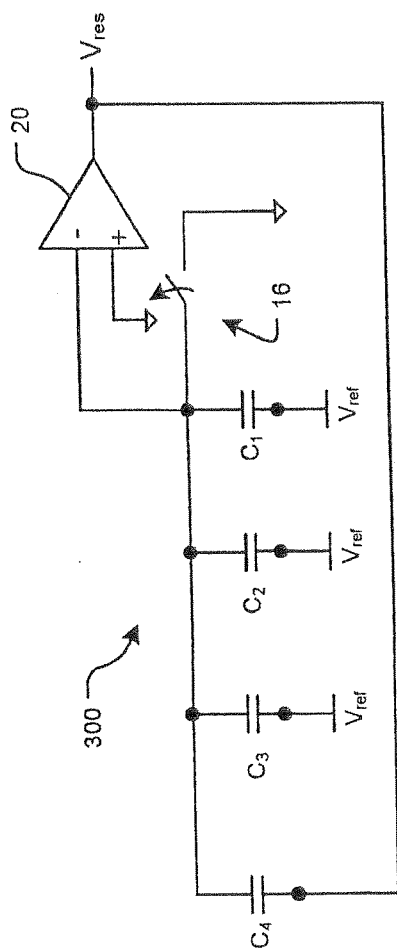


FIG. 15

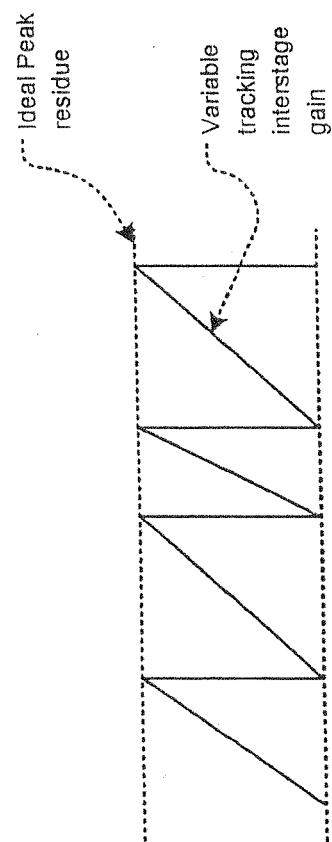


FIG. 16

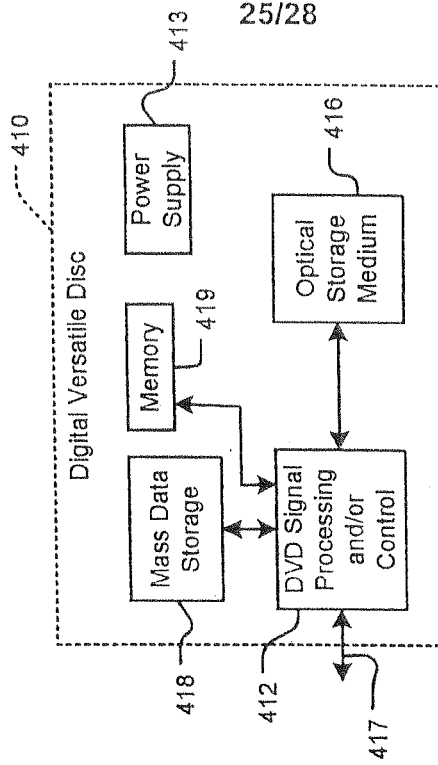


FIG. 17B

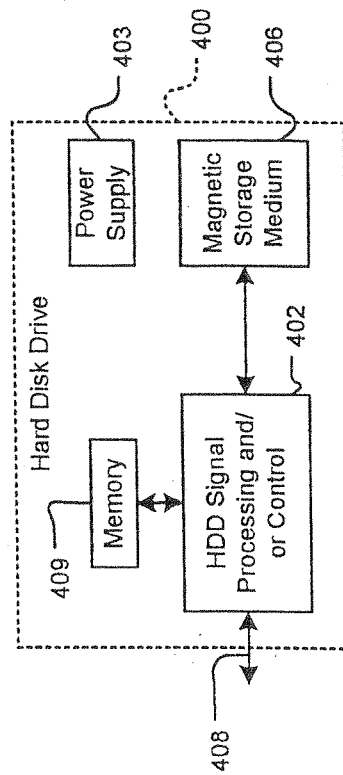


FIG. 17A

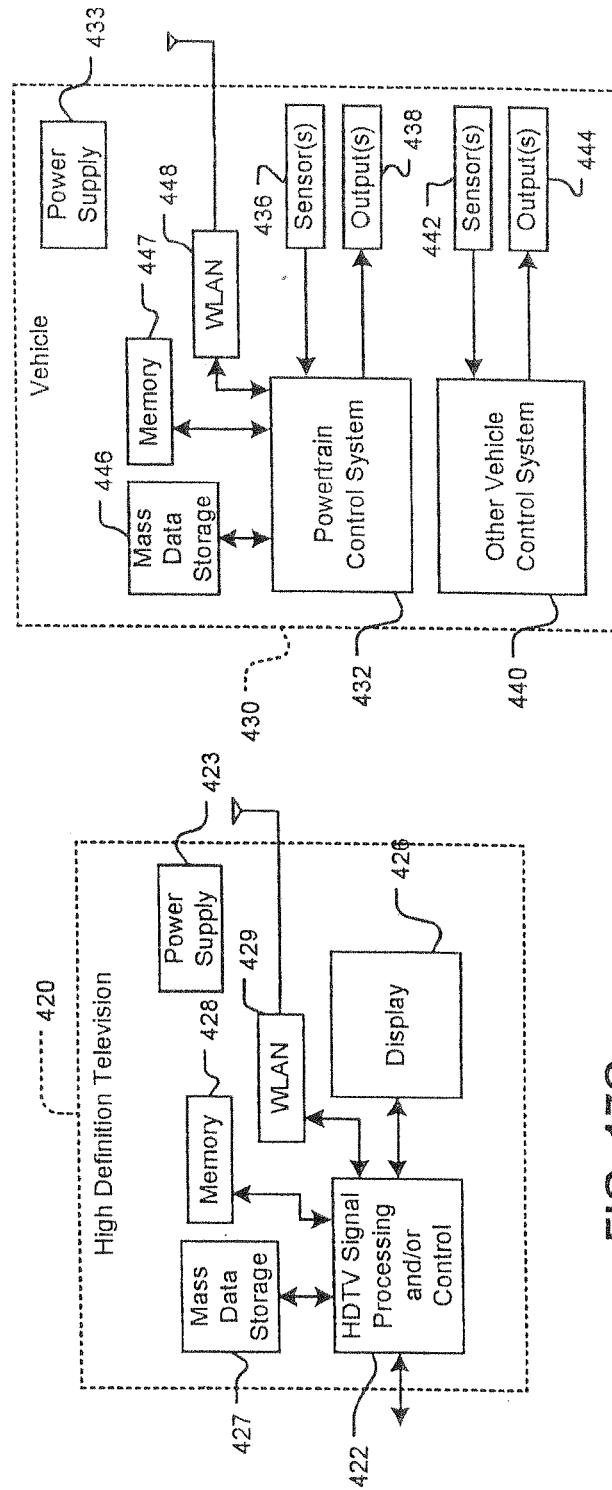


FIG. 17C

FIG. 17D

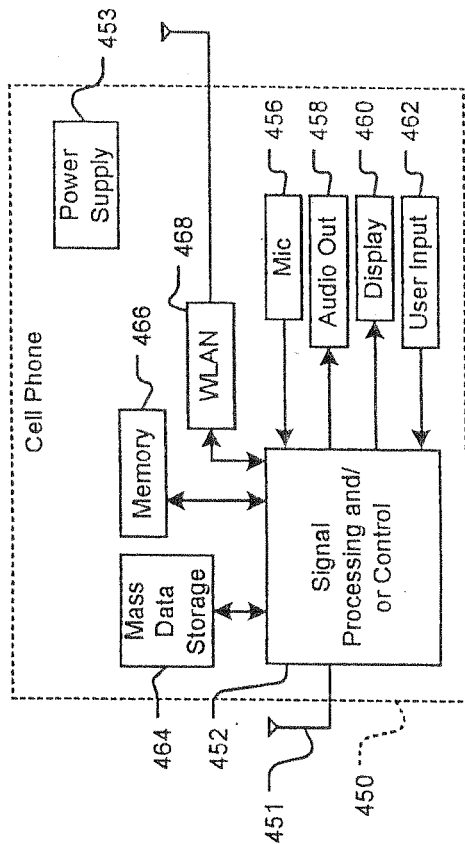


FIG. 17E

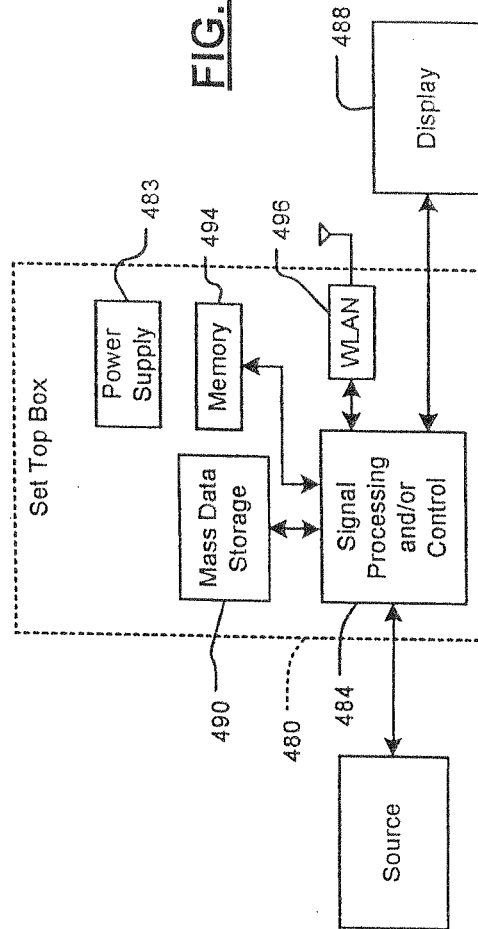


FIG. 17F

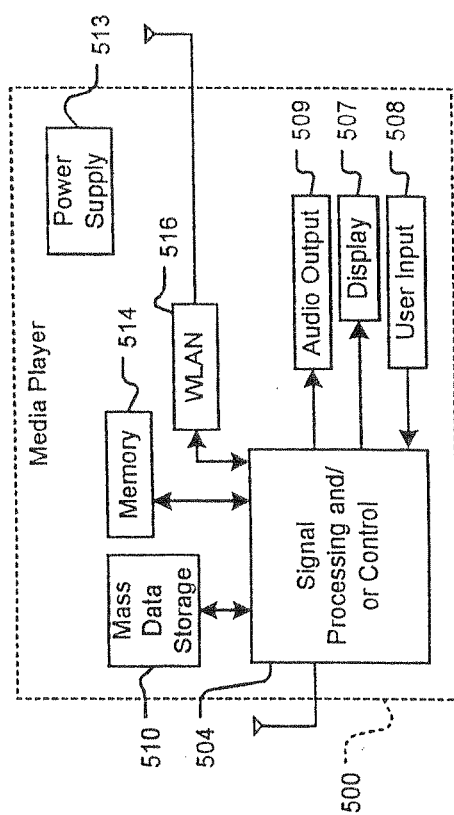


FIG. 17G