PROCESS TO DISSOLVE THE OXIDE LAYER IN THE PERIPHERAL RING OF A STRUCTURE OF SEMICONDUCTOR-ON-INSULATOR TYPE

The present invention concerns a process to treat a structure of semiconductor-on-insulator type (SOI) successively comprising a carrier substrate, an oxide layer and a thin layer of semiconductor material, and more particularly a treatment process with which it is possible to avoid delaminating the semiconductor layer during thermal treatment to dissolve the oxides.

In the area of structures of semiconductor-on-insulator type (SOI) it is known to apply thermal treatment to cause diffusion of at least part of the oxygen from the buried oxide layer through the thin semiconductor layer, so as to reduce or eliminate the thickness of this oxide layer.

This dissolution step can be applied to the entire structure, or it can be applied locally i.e. to dissolve the oxide layer - in whole or in part - in determined regions of the SOI structure, corresponding to a desired pattern, whilst preserving

the initial oxide layer in the other regions. This is termed "local dissolution" of the oxide layer.

The application of this dissolution thermal treatment or of any other type of thermal treatment, such as surface smoothing or an epitaxy step, may cause a phenomenon of de-wetting as mentioned in document WO 2007/048928. It was observed by the inventors of the present invention that this phenomenon was particularly triggered on the periphery of the structure, and more generally at every point in the structure in which the buried oxide is exposed i.e. in contact with the outside, or at every point in which the thin layer is so thin (a few tens of nanometres or less) that it becomes morphologically unstable when the structure is brought to high temperature thereby exposing the buried oxide.

This de-wetting phenomenon is greater the thinner the thickness of the thin layer (for example less than 100 nm).

It is accompanied by a phenomenon of etching of the buried oxide if this oxide is exposed to the treatment atmosphere and in contact with the thin layer in Si for example, as per the reaction:

$SiO_2 + Si \rightarrow$ (gaseous) $2\,SiO$

At the "three-point" contact of Si/SiO2/ treatment atmosphere, the buried oxide (SiO2) reacts with the silicon of the thin layer to form volatile SiO complexes, which are carried into the treatment atmosphere.

It is recalled that in substrates of semiconductor-on-insulator type (SOI) obtained by bonding there is no bonding on the edge of the assembled substrates on account of the presence of

peripheral chamfers on the contacted surfaces. Therefore after transfer of the thin layer, in silicon for example, the final substrate has a peripheral ring in which transfer did not take place and at which the buried oxide is exposed.

Phenomena of de-wetting and etching which may occur during thin layer thermal treatments lead to an extensive defective region over a distance of up to 1 cm on the periphery of the substrate when this substrate is exposed to thermal treatment e.g. dissolution thermal treatment.

This defectiveness may also occur at any other point of the starting substrate, at which the buried oxide is directly exposed or lies under a thin layer of reduced thickness. The defect is possibly a through defect (also called "HF defect") in the thin layer and therefore exposes the buried oxide to the treatment atmosphere. It may concern regions of the substrate in which the thin layer is of much narrower thickness than the mean thickness of this layer, making exposure of the buried oxide to the treatment atmosphere possible if the thickness of the thin layer should be reduced during treatment.

These phenomena make the substrate unfit for uses in the usual areas of application of these substrates, such as the fabrication of electronic components (e.g. "memory" and "logic" components) in the regions in which such defects occur.

Embodiments of the invention seek to overcome this disadvantage by proposing a process of simple design and low-cost to obtain a structure of semiconductor-on-insulator type (SOI) not comprising any de-wetting or etch phenomena, at least on all or part of its periphery.

According to an aspect of the invention, there is provided a process to treat a structure of semiconductor-on-insulator type, which successively comprises a carrier substrate, an oxide layer and a thin layer of semiconductor material, said structure having a peripheral ring in which the oxide layer is exposed, said process comprising the application of a main thermal treatment in a neutral or controlled reducing atmosphere, wherein the thin layer has at least twice the thickness of the oxide layer, the method comprising a step of covering at least an exposed peripheral part of the oxide layer, prior to said main thermal treatment, and wherein the latter treatment is conducted under controlled time and temperature conditions so as to urge at least part of the oxygen of the oxide layer to diffuse through the thin semiconductor layer, leading to controlled reduction of the thickness of the oxide layer.

By the expression "at least an exposed peripheral part of the oxide layer" is meant that the regions in the proximity of the exposed part of buried oxide are also covered in which the thin layer is of very narrow thickness. This thickness will come to be reduced during thermal treatment, which means that the underlying oxide layer could be exposed or become morphologically unstable during treatment. Therefore with annealing at 1100°C, advantageously provision must be made for at least 10 nm of layer over the oxide, and at 1200°C provision is advantageously made for at least 50 nm of layer over the oxide in the vicinity of the periphery.

According to advantageous, non-limiting embodiments of this process:

- the main thermal treatment is a smoothing thermal treatment;

- additional thermal treatment, called creep treatment, is applied directly before said main thermal treatment to cause creep of the semiconductor layer over the exposed peripheral part of the oxide layer;
- creep thermal treatment is carried out by very rapid application of thermal treatment at a final temperature in the order of 1200°C;
- creep thermal treatment is conducted at the final temperature for a time of less than 3 minutes;
- creep thermal treatment is performed with a temperature rise of more than 20°C/second, preferably in the order 50°C/second;
- the oxide layer has a thickness in the region of 10 nm, whilst said thin layer has a thickness at least ten times greater;
- creep thermal treatment is conducted in a hydrogen and/or argon atmosphere;
- prior to the main thermal treatment and/or after the creep thermal treatment, a mask is formed on the exposed peripheral part of the buried oxide;
- the mask is formed locally on the semiconductor layer to allow local dissolution during the thermal treatment step;
- said layer of semiconductor material is in silicon;
- said oxide layer is in silicon oxide.

Other advantages and characteristics of the invention will become better apparent from the following description of several variants of embodiment, given as non-limiting examples of the process conforming to the invention, with reference to the appended drawings in which:

- Figure 1 illustrates a structure of semiconductor-on-insulator type prior to oxide dissolution treatment according to the invention,

- Figure 2 is a detailed view of the ring of the structure of semiconductor-on-insulator type illustrated Figure 1,

- Figure 3 illustrates one step in the treatment process of the structure according to the invention,

- Figures 4 and 5 illustrate the steps of a variant of embodiment of the treatment process according to the invention,

- Figures 6 to 8 illustrate the steps of another variant of embodiment of the treatment process according to the invention.

With reference to Figure 1, a dissolution treatment, described in detail below, is applied to a structure of semiconductor-on-insulator (SOI) type, successively comprising from its base towards its surface a carrier substrate 1, an oxide layer 2, and a semiconductor layer 3.

The carrier substrate essentially acts as stiffener for the SOI structure.

For this purpose, it typically has a thickness in the order of a few hundred micrometres.

The carrier substrate 1 can be a bulk substrate or a composite substrate i.e. consisting of a stack of at least two layers of different materials.

The carrier substrate 1 may for example comprise one of the following materials: Si, Ge, SiGe, GaN, sapphire.

The semiconductor layer comprises at least one semiconductor material such as Si, Ge, or SiGe.

The semiconductor layer 3 may optionally be composite i.e. consisting of a stack of layers of semiconductor materials.

The material of the semiconductor layer 3 may be single-crystalline, polycrystalline, or amorphous. It may or may not be porous and may or may not be doped.

In a particularly advantageous manner, the semiconductor layer 3 is adapted to receive electronic components.

The thin semiconductor layer 3 has a thickness of less than 5000 Å, and preferably less than 2500 Å to allow sufficiently rapid diffusion of the oxygen. The thicker the semiconductor layer 3, the slower the rate of dissolution of the oxide.

The diffusion of oxygen through a semiconductor layer 3 of thickness greater than 5000 Å is very slow, and on this account little advantageous at industrial level.

The oxide layer 2 is buried in the structure, between the carrier substrate 1 and the semiconductor layer 3; it is therefore generally designated in the trade under the acronym BOX, for Buried Oxide Layer.

The SOI structure is fabricated using any layering technique known to the person skilled in the art, involving bonding.

Amongst these techniques mention may be made of the Smart-Cut process (registered trademark) which chiefly comprises the following steps:

i) forming an oxide layer 2 on the carrier substrate 1 or on a donor substrate containing the semiconductor layer 3,

ii) forming a weakened region in the donor substrate, the weakened region defining the thin semiconductor layer 3 to be transferred,

iii) bonding the donor substrate onto the carrier substrate, the oxide layer 2 being positioned at the bonding interface,

iv) splitting the donor substrate along the weakened region to transfer the thin semiconductor layer 3 onto the carrier substrate 1.

This technique is known to the person skilled in the art and will therefore not be further described herein. It is referred for example to: "Silicon-On-Insulator Technology: Materials to VLSI, 2nd Ed." by Jean-Pierre Colinge, Kluwer Academic Publishers, p.50-51.

It is also possible to use a technique consisting of bonding, onto the carrier substrate 1, a donor substrate comprising the semiconductor layer 3, one and/or the other of the substrates being coated with an oxide layer 2, then of reducing the thickness of the donor substrate via its back face so as only to leave the thin semiconductor layer 3 on the carrier substrate 1.

The SOI substrate obtained can then be subjected to conventional finishing treatments (polishing, planarizing, cleaning, etc.).

In these processes to form the SOI structure, the oxide layer 2 is formed on the donor substrate or on the carrier substrate 1 by thermal oxidation (in which case the oxide is an oxide of the material of the substrate which underwent oxidation) or by deposit e.g. of silicon oxide (SiO_2).

The oxide layer 2 can also be a native oxide layer, resulting from natural oxidation of the donor substrate and/or of the carrier substrate 1 in contact with the atmosphere.

On the other hand, tests performed on SOI structures obtained using the SIMOX process did not allow any oxide dissolution to be observed, which was attributed to an inferior oxide quality due to the method with which it was obtained. In this respect, reference may be made to the article by L. Zhong *et al*, Applied Physics Letters 67, 3951 (1995).

It is specified that before starting the bonding step it is possible to conduct cleaning or plasma activation steps on one and/or the other of the surfaces in contact, these steps being well known to the person skilled in the art, in order to enhance bonding energy.

To limit the duration of dissolution treatment and to facilitate the covering step, the oxide layer 2 of the SOI structure generally has a thin or ultrathin thickness i.e. between 50 and 1000 Å, preferably between 100 and 250 Å.

Also, with reference to Figure 2, the SOI structure obtained using one of the above-described techniques has a so-called ring region 4 on its periphery in which the oxide layer 2, in particular its flank, is exposed i.e. part of the oxide layer is in contact with the atmosphere. This ring 4 may extend over all or part of the periphery of the SOI structure.

With reference to Figure 3, the process of the invention consists of depositing a mask 5 on the ring 4 prior to the thermal dissolution treatment so that the oxide layer 2, in particular its flank, is not in contact with the atmosphere.

Preferably, the mask 5 covers not only the exposed oxide but also the peripheral part of the semiconductor layer 3 which is thinned. The thickness

of this layer effectively tends to be reduced during dissolution treatment. The presence of the mask on the periphery of the semiconductor layer (over a width of a few micrometres) therefore makes it possible to prevent the oxide located underneath this thinner layer from being exposed during dissolution, through thinning effect and/or morphological instability at high temperature.

This mask 5 is obtained in a material capable of forming a barrier against diffusion of the oxygen atoms during the dissolution thermal treatment, and it is able to withstand the conditions of thermal dissolution treatment.

Said mask 5 may solely cover the ring 4, to allow subsequent so-called "full wafer" dissolution, i.e. dissolution of the oxide layer over the entire structure.

According to one variant, the mask may also be deposited on determined regions of the semiconductor layer, for the purpose of local dissolution. In a particularly advantageous manner, during one same step the mask is formed on the ring and on the regions of the semiconductor layer underneath which it is not desired to dissolve the oxide.

The forming of this mask 5 can be obtained using conventional photolithography techniques.

Typically, the mask-forming method comprises the following successive steps:

- Forming a layer of material intended to form the mask, over the entire surface of the semiconductor layer, by deposit;

- Depositing a layer of photoresist over the entire surface of the preceding layer;

- Local insulation of the resin through a photolithographic mask;

- Selective removal of the insulated regions by dilution with a solvent for example;

- Then, through the openings formed in the resin, etching the exposed regions of the mask layer. Etching is typically dry etching (plasma) to which the resin is resistant. The material of the mask on the other hand is etched by this plasma.

This example is evidently non-limiting, and any technique which can be used to form the mask on the desired regions of the SOI can be used.

For example, silicon nitride (of general formula SiN comprising different possible stoechiometric coefficients) is a preferred material to form the mask since it is easy to use (i.e. to deposit and then remove after dissolution treatment) and does not contaminate the silicon.

However, any other material forming a barrier against diffusion of the oxygen and withstanding the conditions of the treatment can be used for the mask.

The mask 5 has a typical thickness of 1 to 50 nm, and is preferably in the order of 20 nm.

After depositing the mask 5, the process therefore comprises a thermal dissolution treatment step which consists of applying a thermal treatment in a neutral or controlled reducing atmosphere, and under controlled time and temperature conditions, so as to urge at least part of the oxygen of the oxide layer 2 to diffuse through the thin semiconductor layer 3, leading to controlled reduction in oxide thickness.

It is noted that with the presence of the mask 5 on the ring it is possible to avoid triggering of the

de-wetting and/or etch phenomenon of the SOI structure at the peripheral ring and in its vicinity.

Preferably, the initial structure is chosen so that it has no or very few defects passing through the upper thin layer, which may expose the underlying oxide i.e. buried layer (in this case the term "HF defect" is used). This avoids or limits the number of points at which the phenomenon of de-wetting or etching of the oxide could be triggered by the atmosphere of the dissolution treatment.

Therefore for a SOI (Si thin layer), substrates can be chosen having no or less than five "HF defects" per 300 mm wafer, which is currently an achievable defect level.

In the remainder of the description, the example used will be the application of the dissolution treatment to a structure in which the thin semiconductor layer is in silicon i.e. a "silicon-on-insulator" (SOI) structure.

The mechanisms of oxide dissolution in a SOI structure are described in detail in the article by O. Kononchuk *et al*, "Internal Dissolution of Buried Oxide in SOI Wafers", Solid State Phenomena Vols. 131-133 (2008) pp 113-118, to which reference may be made.

During the treatment, the SOI structure is placed in an oven in which a gas flow is generated to form a neutral or reducing atmosphere.

The gas flow may therefore contain argon, hydrogen and/or a mixture thereof.

It is important to note that the phenomenon of dissolution only occurs when there is a sufficient gradient between the concentration of oxygen in the

atmosphere and the concentration of oxygen on the surface of the oxide layer.

Therefore, it is considered that the oxygen content of the atmosphere in the oven must be lower than 10 ppm which, taking leakages into account, requires an oxygen content in the gas flow of less than 1 ppb.

In this respect, reference may be made to the article by Ludsteck *et al*, "Growth model for thin oxides and oxide optimization", Journal of Applied Physics, Vol. 95, No. 5, Mars 2004.

These conditions cannot be obtained in a conventional oven, which generates too many leaks to allow such a low content to be reached; the oven needs to be specially designed for optimum sealing (reduced number of parts to avoid number of gaskets, use of solid parts, etc.).

On the contrary, a concentration of oxygen in the atmosphere of more than 10 ppm halts dissolution and promotes oxidation of the exposed silicon.

With a SOI, the dissolution treatment is applied at a temperature of between 1100 and 1300°C, preferably in the order of 1200°C. For ultrathin SOI structures (thin silicon layer of 200 Angström or less), dissolution temperatures between 1050°C and 1100°C can be considered. These ultrathin SOI structures being particularly sensitive to the de-wetting phenomenon, it will be sought to lower the treatment temperature.

It is noted that the phenomenon of dissolution may also be observed at these low temperatures if the upper silicon layer is effectively ultrathin.

The higher the temperature, the faster the rate of oxide dissolution. However, the treatment

temperature must remain lower than the melting point of silicon.

For example, to dissolve an oxide thickness of 20 Å under a thin silicon layer of 1000 Å, the thermal treatment conditions are: 1100°C for 2 hours, 1200°C for 10 minutes, or 1250°C for 4 minutes. It is pointed out however that these values depend in particular on the residual oxygen concentration in the dissolution oven. Therefore, greater dissolved thicknesses have also been observed.

After this thermal dissolution treatment, the mask 5 can be removed by dry or wet etching.

Evidently, the mask 5 could be removed by any appropriate means known to the person skilled in the art without departing from the scope of the invention.

According to one variant of embodiment of the process according to the invention, with reference to Figure 4, prior to a dissolution treatment such as previously described a so-called creep thermal treatment is applied to a structure of semiconductor-on-insulator-type (SOI) successively comprising from its base to its surface a carrier substrate 1, an oxide layer 2, and a semiconductor layer 3, said structure also comprising a ring 4 in which the oxide layer 2 is exposed.

This creep thermal treatment consists of rapidly applying a temperature in the order of 1200°C to the structure for a time of less than 3 minutes, said creep thermal treatment preferably being conducted in a hydrogen and/or argon atmosphere.

This creep thermal treatment, with reference to Figure 5, causes creep of the semiconductor layer 3 until it covers the exposed peripheral part of the

buried oxide i.e. until the semiconductor of said layer 3 fully covers the oxide which was initially in contact with the atmosphere. It may also lead to masking the buried oxide at the through defects present on the surface of the wafer.

The thickness of the semiconductor material covering the oxide must be sufficient, with respect to the thickness of the oxide to be dissolved, to prevent the oxide from becoming exposed or made morphologically unstable during the dissolution treatment owing to the above-mentioned thinning of the semiconductor layer during this treatment. It is known that during the dissolution of an oxide thickness e, a thickness in the order of e/2 of the surface layer is etched. It is therefore necessary to make provision for a surface layer having at least twice the thickness of the oxide layer that is to be dissolved, to avoid exposing the oxide layer during this dissolution and causing the onset of a three-point contact: oxide/surface layer/treatment environment.

Preferably, a thickness ratio of more than two is chosen between the oxide to be dissolved and the surface layer, e.g. six or seven.

Therefore, it is preferable for the insulator layer to have a relatively narrow thickness compared with the upper layer of semiconductor material (e.g. 10 nm buried oxide for a thin layer of 70 nm). This configuration facilitates encapsulation of the buried layer by creep of the semiconductor layer. Therefore, after creep, the thickness of the semiconductor layer at the previously exposed peripheral part of the buried oxide and in its vicinity may be greater than 10 nm, even 50 nm or more.

Also, a relatively narrow thickness of the insulator layer makes it possible to reduce the required dissolution time. It is therefore possible to choose an insulator thickness of between 5 nm and 50 nm, typically between 10 and 25 nm.

A thermal dissolution treatment is then applied as described previously, to obtain dissolution of the oxide without causing peripheral deterioration of the structure. Intermediate steps between the creep step and the dissolution step must be avoided or limited so as not to expose the buried oxide (thinning by sacrificial oxidation for example or other smoothing heat treatment, etc.). Nonetheless, some cleaning or sacrificial oxidation treatment may be tolerated provided they do not cause too much thinning of the treated layer.

Under an electronic microscope, a cross-section of an SOI edge after different treatments shows the following:

- cleaning before thermal treatment: the "lateral" oxide is exposed;
- after this thermal treatment: the efficiency of the creep phenomenon is evidenced;
- after a thinning step by oxidation/deoxidation of the preceding structure, to bring the thickness of the thin semiconductor layer to the desired final thickness, it is observed that the buried oxide is not exposed. Therefore the structure could undergo a dissolution treatment without any risk of causing a de-wetting phenomenon.

According to one last variant of embodiment of the process according to the invention, with reference to Figures 6 to 8, prior to a dissolution

treatment a so-called creep thermal treatment is applied in the same manner as previously described to a structure of semiconductor-on-insulator type (SOI) successively comprising from its base towards its surface a carrier substrate 1, an oxide layer 2 and a semiconductor layer 3, said structure also comprising a ring 4 in which the oxide layer 2 is exposed.

This creep thermal treatment consists of applying a temperature in the order of 1200°C to the structure for a time of less than 3 minutes, said creep thermal treatment preferably being conducted in a neutral or reducing atmosphere e.g. hydrogen and/or argon.

Said creep thermal treatment, with reference to Figure 7, causes creep of the semiconductor layer 3 until it covers the quasi-entirety of the ring 4 i.e. until the semiconductor of said layer 3 covers most of the oxide which was initially in contact with the atmosphere. In this particular embodiment the semiconductor layer 3, after creep thermal treatment, covers the flank of the oxide layer 2; nonetheless the upper edge of said oxide layer 2 remains in contact with the atmosphere.

The process, with reference to Figure 8, then comprises a step to form a mask 5 on the ring 4 so as to cover fully the oxide layer 2 i.e. all the parts of the oxide layer 2 which are in contact with the atmosphere after the creep thermal treatment.

Said mask 5 is obtained in any material forming a barrier against oxygen diffusion and withstanding the conditions of dissolution thermal treatment. Additionally, it is formed using any suitable process such as described previously.

A dissolution thermal treatment is then applied such as previously described, to obtain dissolution of the oxide without causing defects on the periphery of the structure, then the mask 5 can be removed by etching or any other appropriate means known to the person skilled in the art.

Finally, the examples just described are evidently only particular illustrations of the process according to the invention, and they are in no way limiting regarding the areas of application of the invention.

In particular, the invention applies to any thermal treatment conducted on a structure of SOI type when the thickness of the upper layer is relatively thin and the treatment temperature and the thickness of the semiconductor layer may possibly cause a phenomenon of de-wetting of the thin layer during the thermal treatment.

Example 1:

Fabrication of a SOI substrate having a final buried oxide layer of 4 nm.

First, a SOI is fabricated having an oxide layer of 10 nm and a thin layer of 3000 nm. This is obtained by:

- Implanting ions in a donor substrate, bonding via an oxide layer of 10 nm onto a receiver substrate and splitting along the implanted region (standard Smart Cut process - registered trademark);
- "RTA" (Rapid Thermal Annealing) to smooth the surface and "encapsulate" the buried oxide on the peripheral region (and at the through-defects on the surface of the wafer);

- Sacrificial oxidation of the layer to bring the surface layer to a final thickness of 2000 Å. It is verified that this step has not caused exposure of the buried oxide at the peripheral regions;
- Dissolution thermal treatment at 1200°C for around 3 hours to arrive at a buried oxide thickness of 4 nm.

On the end product no degradation is seen in the number of defects before and after dissolution treatment, whether at the centre of the wafer or on its periphery.

Example 2

A SOI substrate is provided comprising a thin layer of 300 nm and a buried oxide of 10 nm.

A dissolution mask is formed (using conventional lithography steps) to mask the regions in which the oxide layer is to be preserved. The mask also extends over the peripheral part of the wafer (a few microns either side of the oxide flank).

Dissolution thermal treatment is then conducted at 1150°C for 1 hour, to cause the buried oxide to disappear entirely at the mask openings.

The mask is then removed and it is ascertained that there is no deterioration in end defectiveness.

CLAIMS

1. Process to treat a structure of semiconductor-on-insulator type, successively comprising a carrier substrate, an oxide layer, and a thin layer of semiconductor material, said structure having a peripheral ring in which the oxide layer is exposed, said process comprising the application of a main thermal treatment in a neutral or controlled reducing atmosphere,

wherein the thin layer has at least twice the thickness of the oxide layer, the method comprising a step of covering at least an exposed peripheral part of the oxide layer, prior to said main thermal treatment, and

wherein this latter treatment is conducted under controlled time and temperature conditions so as to urge at least part of the oxygen of the oxide layer to diffuse through the thin semiconductor layer, leading to controlled reduction of the thickness of the oxide layer.

2. Process according to claim 1, wherein said main thermal treatment is a smoothing thermal treatment.

3. Process according to any of the preceding claims, wherein an additional so-called creep thermal treatment is applied directly before said main thermal treatment, to cause creep of the semiconductor layer over the exposed peripheral part of the oxide layer.

4. Process according to claim 3, wherein the creep thermal treatment is conducted by

very rapid application of a thermal treatment at a final temperature in the order of 1200°C.

5. Process according to claim 4, wherein said creep thermal treatment is performed with a temperature rise of more than 20°C/second, preferably in the order of 50°C/second.

6. Process according to either of claims 3 or 5, wherein the creep thermal treatment is conducted at the final temperature for a time of less than 3 minutes.

7. Process according to any of the preceding claims, wherein said oxide layer has a thickness in the order of 10 nm, whilst said thin layer has a thickness at least ten times greater.

8. Process according to any of claims 3 to 7, wherein the creep thermal treatment is conducted in an atmosphere of hydrogen and/or argon.

9. Process according to any of the preceding claims, wherein, prior to the main thermal treatment and/or after the creep thermal treatment, a mask is formed on the exposed peripheral part of the buried oxide.

10. Process according to claim 9, wherein the mask is formed locally on the semiconductor layer to allow local dissolution during the thermal treatment step.

11. Process according to any of the preceding claims, wherein said layer of semiconductor material is in silicon.

12. Process according to any of the preceding claims, wherein said oxide layer is in silicon oxide.