

CLAIMS:

1. A method used in forming a memory array comprising strings of memory cells, comprising:
 - forming a stack comprising vertically-alternating first tiers and
5 second tiers;
 - forming horizontally-elongated trenches into the stack to form laterally-spaced memory-block regions;
 - forming a wall in individual of the trenches laterally-between immediately-laterally-adjacent of the memory-block regions, the forming of
10 the wall comprising:
 - lining sides of trenches with insulative material comprising at least one of an insulative nitride and elemental-form boron; and
 - forming a core material in the trenches to span
15 laterally-between the at least one of the insulative nitride and the elemental-form boron.
2. The method of claim 1 wherein the insulative material comprises an insulative nitride.
3. The method of claim 1 wherein the insulative material
20 comprises elemental-form boron.
4. The method of claim 1 wherein the insulative material comprises both of an insulative nitride and elemental-form boron.
5. The method of claim 1 comprising forming the individual
25 trenches to have an uppermost minimum lateral width in a vertical cross-section, the insulative material on each side of the core material having a lateral width of 1% to 20% of the uppermost minimum lateral width in the vertical cross-section.

6. The method of claim 1 comprising:

before forming the wall in the individual trenches, isotropically etching away and replacing sacrificial material that is in the conductive tiers with conducting material of individual conductive lines;

5 forming individual memory cells of the strings of memory cells to comprise channel material of channel-material strings in the memory-block regions, a gate region that is part of one of the individual conductive lines in individual of the conductive tiers, and a memory structure laterally-between the gate region and the channel material of the channel-material strings in
10 the individual conductive tiers, forming the channel-material strings before forming the conducting material of the individual conductive lines; and after the replacing, forming the wall in the individual trenches.

7. A method used in forming a memory array comprising strings of memory cells, comprising:

15 forming a stack comprising vertically-alternating first tiers and second tiers;

forming horizontally-elongated trenches into the stack to form laterally-spaced memory-block regions;

20 through the trenches, isotropically etching away and replacing sacrificial material that is in the conductive tiers with conducting material of individual conductive lines;

forming individual memory cells of the strings of memory cells to comprise channel material of channel-material strings in the memory-block regions, a gate region that is part of one of the individual conductive lines in
25 individual of the conductive tiers, and a memory structure laterally-between the gate region and the channel material of the channel-material strings in the individual conductive tiers, forming the channel-material strings before forming the conducting material of the individual conductive lines;

30 after the replacing, forming a wall in individual of the trenches laterally-between immediately-laterally-adjacent of the memory-block regions, the forming of the wall comprising:

lining sides of trenches with insulative material comprising at least one of an insulative nitride and elemental-form boron that is directly against the conducting material of
35 the individual conductive lines; and

forming a core material in the trenches spanning laterally between the at least one of the insulative nitride and the elemental-form boron, the forming of the core material comprising:

- 5 forming a laterally-outer silicon dioxide that is directly against said at least one of insulative nitride and elemental-form boron; and
- forming polysilicon directly against and to span laterally-between said laterally-outer silicon dioxide.

- 10 8. A memory array comprising strings of memory cells, comprising:
- a vertical stack comprising alternating insulative tiers and conductive tiers, the conductive tiers individually comprising conductive lines;
- strings of memory cells in the stack comprising channel material
- 15 extending through the insulative tiers and the conductive tiers; individual of the memory cells comprising the channel material, a gate region that is part of one of the conductive lines in individual of the conductive tiers, and a memory structure laterally-between the gate region and the channel material in the individual conductive tiers; and
- 20 walls individually extending through the insulative tiers and the conductive tiers laterally between immediately-adjacent of the conductive lines, the walls individually comprising laterally-outer insulative material and a core material spanning laterally-between the laterally-outer insulative material, the laterally-outer insulative material comprising at least one of an
- 25 insulative nitride and elemental-form boron.

9. The memory array of claim 8 wherein the laterally-outer insulative material comprises an insulative nitride.

10. The memory array of claim 9 wherein the insulative nitride comprises one or more of boron nitride, carbon nitride, silicon nitride,
- 30 silicon nitride carbide, and germanium nitride.

11. The memory array of claim 8 wherein the laterally-outer insulative material comprises elemental-form boron.

12. The memory array of claim 8 wherein the laterally-outer insulative material comprises both insulative nitride and elemental-form boron.

13. The memory array of claim 8 wherein the laterally-outer
5 insulative material is devoid of oxygen.

14. The memory array of claim 8 wherein the at least one of insulative nitride and elemental-form boron is directly against conducting material of the conductive lines.

15. The memory array of claim 8 wherein the core material at least
10 predominately comprises insulative material.

16. The memory array of claim 8 wherein the core material at least predominately comprises conductive material.

17. The memory array of claim 8 wherein the core material at least predominately comprises semiconductive material.

18. The memory array of claim 17 wherein the semiconductive
15 material at least predominately comprises undoped elemental-form silicon.

19. The memory array of claim 8 wherein, in a vertical cross-section, the laterally-outer insulative-material on each side of the core material has a lateral width of 1% to 20% of an uppermost minimum lateral
20 width of the individual wall in the vertical cross-section.

20. The memory array of claim 8 wherein the core material is homogenous.

21. The memory array of claim 8 wherein the core material is not homogenous.

22. The memory array of claim 21 wherein the core material
25 comprises a laterally-outer insulative oxide and a laterally-inner material that is not an insulative oxide.

23. The memory array of claim 22 wherein the laterally-outer insulative material comprises silicon nitride.

24. The memory array of claim 21 comprising void space in the core material.

25. The memory array of claim 8 comprising NAND.

26. A memory array comprising strings of memory cells,
5 comprising:
a vertical stack comprising alternating insulative tiers and conductive tiers, the conductive tiers individually comprising conductive lines comprising conducting material;
strings of memory cells in the stack comprising channel material
10 extending through the insulative tiers and the conductive tiers; individual of the memory cells comprising the channel material, a gate region that is part of one of the conductive lines in individual of the conductive tiers, and a memory structure laterally-between the gate region and the channel material in the individual conductive tiers; and
15 walls individually extending through the insulative tiers and the conductive tiers laterally-between two of the conductive lines, the walls individually comprising laterally-outer insulative material and a core material spanning laterally-between the laterally-outer insulative material, the laterally-outer insulative material comprising at least one of an
20 insulative nitride and elemental-form boron that is directly against the conducting material of the conductive lines, the core material comprising:
a laterally-outer silicon dioxide that is directly against
said at least one of insulative nitride and elemental-form boron;
and
25 polysilicon directly against and spanning laterally-between said laterally-outer silicon dioxide.