

AN INTEGRATED CIRCUIT

Field of the invention

- 5 The present invention relates to an integrated circuit and elements thereof, in particular an on-chip antenna and a guard ring.

Background of invention

- 10 As Integrated Circuits (ICs) are progressively made smaller, there arises a need for suitable small antennae which are to be used with the ICs, especially on-chip antennae. Of the currently available types of on-chip antennae, a certain type uses planar spiral coils, which allow exchange of energy and signals between receivers and transmitters by magnetic flux flowing through the coils.
- 15 Such antennae share space on the IC chip layer on which they are disposed with related circuitry. The efficiency of antennae is an important factor and it is a disadvantage of such an on-chip antenna of this type that it has low power transfer rate.
- 20 Designs of such on-chip antennae have been proposed in the following US patents:

U.S. Pat. No. 6,373,447 proposes dividing an IC surface into two areas, a peripheral area and a central area. Figure 6 of the patent, which is reproduced

as FIG. 1 herein, shows a plan view of an embodiment 100 of an IC chip having two antennae 104, 124 in the portions labelled 112 and 114 on the IC chip 102. The antennae and the circuitry share the central area with the circuitry disposed within a portion 110 of the central area 108 of the chip 102. If more antennae
5 are implemented, the antennae will occupy more area and therefore reduce the area available for the circuitry.

U.S. Pat. No. 4,724,427 proposes a transponder device. Figure 9 of the patent is reproduced as FIG. 2 herein, which is a plan view of a monolithic IC chip with
10 a generalised topographical layout of the various types of circuits used within the transponder device. An antenna coil 220 is etched around the periphery of the chip substrate 298. Located in the centre of the coil 220 is implementing circuitry of the antenna coil, such as logic circuits 200, a programmable memory array 202 and memory control logic 204. Even though the antenna coils are
15 disposed around the periphery of the chip, the antenna shares the die area with circuitry.

The proposals in US 6,373,447 and US 4,724,427 lead to a reduction in available space on an IC chip for implementing circuitry and to poor RF power
20 transfer to the antenna because the antenna is too close to the circuitry and peripheral devices, such as bond pads and guard rings. Traces of metal in the circuitry and bond pad affect field distribution which results in less magnetic flux flowing through the antenna coils.

It is an object of one aspect of the invention to provide an antenna structure which alleviates at least one disadvantage of the prior art, and/or provides the general public with a useful choice.

- 5 In IC chip design, guard rings are sometimes used to protect the die and IC chip circuitry from damage. Examples of damage which can occur are contamination by environmental foreign impurities or ionic compounds that penetrate exposed edges of a diced chip and mechanical damage including micro-cracks that is produced when a wafer is diced. The guard ring also protects the integrated
10 circuit from breakdown by providing a low-resistance path for surge currents.

Normally, a guard ring in an IC is a closed loop structure formed by metal layers that are connected by via-holes. It is a disadvantage of a guard ring that, while
15 protecting the IC, the guard ring consumes power, especially when a coil-type on-chip antenna is integrated with the IC, and also produces counteractive magnetic flux which weakens the magnetic field and decreases the power transfer rate of the antenna. The reason is that a current is induced in the guard ring producing heat and counteractive magnetic flux. Guard rings usually have
20 similar structures as antenna coils, which is why any guard ring around an IC circuitry will be induced to produce a current which absorbs RF energy.

Some guard ring structures have been proposed in the following US patents:

U.S. Pat. 5,811,874 and U.S. Pat. 6,163,065 disclose various structures of metal can be used as guard rings offering improved protection to the IC.

However, the guard ring still suffers from the problem that current is induced and the power transfer rate to the antenna becomes poor.

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U.S. Pat. No. 5,811,874 discloses a semiconductor chip package device having a rounded or chamfered metal layer guard ring. Figure 7 and Figure 8 of the patent, reproduced as FIG. 3 herein, shows enlarged partial views of portions of a guard ring 312 on a chip 300. The guard ring 312 has chamfered 328 or
10 rounded 330 corners. The chamfered 328 or rounded 330 corners are meant to provide prevention against shear deformation, cracking of the metal and passivation.

U.S. Pat. No. 6,163,065 discloses an energy-absorbing stabilised guard ring.

15 The guard ring has castellated portions at its corners. The castellated portions prevent breaking of the guard ring during reliability tests, when shear forces are act on the guard ring, and also prevent delamination of the passivation layer. Figure 4 of the patent, reproduced as FIG. 4 herein, shows an encircled castellated portion 453 of a guard ring 404 (in a die).

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While showing alternative structures of guard rings, these patents do not address the problem of induced current in the guard ring compromising the power transfer to the antenna.

It is an object of another aspect of the invention to provide a guard ring that alleviates this problem of the prior art, and/or provides the general public with a useful choice.

5 Summary of the invention

According to the invention in a first aspect, there is provided an integrated circuit antenna device having an antenna and processing circuitry therefor, the antenna and circuitry being formed on separate layers of the integrated circuit.

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Preferably the integrated circuit includes a plurality of insulating layers and a plurality of conductive layers and the antenna is separated from the circuitry by an insulating layer thicker than the conductive layers and other insulating layers.

15 The antenna is preferably separated from the circuitry by an insulating layer of at least $5\mu\text{m}$ thickness, most preferably by an insulating layer of a thickness in the range $5\mu\text{m}$ to $20\mu\text{m}$.

The antenna and circuitry may be formed as separate portions of the integrated
20 circuit.

An electrical connection may be provided between layers of the integrated circuit, the electrical connection being provided with pads at each end, a first pad being arranged to receive a connection to a device external to the

integrated circuit and a second pad arranged for internal connection within the integrated circuit and wherein said first pad is larger than said second pad and at least one further electrical connection arranged for internal connection between two layers within the integrated circuit and having further pads at each end may be provided, wherein the further pads are smaller than the first pad.

The aerial may be formed on more than one layer of the integrated circuit.

A conductive guard ring may be disposed on a layer of the integrated circuit and the guard ring is preferably discontinuous and/or having two ends and a gap therebetween. The gap is preferably not straight and the ends may inter-engaging portions which preferably comprise at least one elongate finger. If the guard ring has a corner, the gap is preferably disposed at the corner. The guard ring may be formed from a plurality of conductive layers and each layer may be separated from the next by an insulation layer.

A capacitor and/or a high voltage breakdown circuit may be disposed across the gap.

The inductance of the ring and the capacitance across the gap may be such as to form an energy storage network which is preferably tuned to the resonant frequency of the network is tuned to a working frequency of the antenna.

The guard ring is preferably formed as a plurality of conductive segments, adjacent segments each having a said pair of ends and a said gap therebetween.

- 5 The guard ring is disposed on the same layer as the aerial or the integrated circuit and may further comprise at least one further guard ring, the guard rings being disposed on respective layers of the integrated circuit, with the guard rings preferably being electrically connected, the guard rings being disposed on the same layers as the aerial, the processing circuitry or both.

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The guard ring may be of spiral topology.

According to the invention in a second aspect, there is provided an integrated circuit comprising a circuit component and a guard ring around the component

- 15 wherein the guard ring has first and second ends and a gap therebetween.

The gap is preferably not straight and the ends may inter-engaging portions which preferable comprise at least one elongate finger. If the guard ring has a corner, the gap is preferably disposed at the corner. The guard ring may be
20 formed from a plurality of conductive layers and each layer may be separated from the next by an insulation layer.

A capacitor and/or a high voltage breakdown circuit may disposed across the gap.

The inductance of the ring and the capacitance across the gap may be such as to form an energy storage network which is preferably tuned to the resonant frequency of the network is tuned to a working frequency of the antenna.

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The guard ring is preferably formed as a plurality of conductive segments, adjacent segments each having a said pair of ends and a said gap therebetween.

10 The component may comprise an aerial.

A plurality of guard rings may be disposed on respective layers of the integrated circuit and the guard rings may be electrically connected.

15 According to the invention in a third aspect, there is provided, an integrated circuit device having a plurality of layers, an electrical connection between two said layers of the integrated circuit, the electrical connection being provided with pads at each end, a first pad being arranged to receive a connection to a device external to the integrated circuit and a second pad arranged for internal
20 connection within the integrated circuit and wherein said first pad is larger than said second pad.

Preferably at least one further electrical connection is arranged for internal connection between two said layers within the integrated circuit and having

further pads at each end and wherein the further pads are smaller than the first pad.

According to the invention in a fourth aspect there is provided a guard ring for
5 an integrated circuit, the guard ring being arranged to form an energy storage
device preferably comprising at least one inductor and at least one capacitor
connected together to form the ring which may be tuned to a resonant
frequency. Where the guard ring is provided adjacent an antenna, the
resonant frequency preferably tuned to an operating frequency of the antenna.

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According to the invention in a fifth aspect there is provided a guard ring for an
integrated circuit, wherein the guard ring is discontinuous, preferably having first
and second ends and a gap formed there between. The antenna may be of
spiral topology.

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According to the invention in further aspects, an antenna or device having an
antenna of the previous aspects of the invention may be arranged to disposed
between two in phase antennae, between a further antenna and a high
magnetic permeability element or in an arrangement with a further antenna
20 disposed on one side of the device and an open loop of high magnetic
permeability material extending from the further antenna to the opposed side of
the device.

The various aspects of the invention are preferably used in RFID technology.

Brief description of the drawings

- 5 Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a plan view of a prior art integrated circuit (IC) chip according to U.S. Pat. No. 6,373,447;

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FIG. 2 is a plan view of a prior art monolithic semiconductor chip according to U.S. Pat. No. 4,724,427;

- 15 FIG. 3 is an enlarged partial view showing two variations of a prior art metal layer guard ring according to U.S. Pat. No. 5,811,874;

FIG. 4 is a plan view of a prior art IC with a guard ring having castellated portions, according to U.S. Pat. No. 6,163,065;

- 20 FIG. 5 shows a cross-sectional view of a semiconductor wafer for an integrated circuit, according to one embodiment of the present invention showing the structure of an on-chip antenna.

FIG. 6 is a plan view of a second embodiment of the invention showing the structure of a guard ring.

FIG. 7 is a plan view of examples of gap capacitors of the guard ring of Fig. 6.

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FIG. 8 is a view of a three-dimensional interdigital capacitor;

FIG. 9 is a circuit diagram of an equivalent circuit of the guard ring of Fig. 6;

10 FIG. 10 is a circuit diagram of an equivalent circuit of the guard ring of Fig. 6 and the on-chip antenna of Fig. 5;

FIG. 11 is a plan view of a third embodiment of the invention having two antenna coils combined with a guard ring;

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FIG. 12 is a plan view of a fourth embodiment of the invention having one octagonal antenna coil combined with a guard ring;

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FIG. 13 is a cross-sectional view similar to the embodiment of Fig. 5, of the embodiment of Fig. 12;

FIG. 14 is a schematic view of a fifth embodiment of the invention showing an antenna structure having two in-phase antennae and a third, sandwiched, on-chip antenna;

FIG. 15 is a schematic view of a sixth embodiment of the invention showing an antenna structure similar to the fifth embodiment but with one antenna replaced by a disc of high μ material; and

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FIG. 16 is a schematic view of a seventh embodiment of the invention showing an antenna structure similar to the fifth embodiment having an open loop of high μ material replacing one antenna.

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Detailed description of the preferred embodiments

FIG. 5 shows a cross-sectional view of an integrated circuit according to a first embodiment of the present invention. The view shows a semiconductor wafer 15 500 comprising a typical IC portion 501 and an add-on portion 502. The IC portion 501 has usual function blocks typically found in an integrated circuit. The add-on portion 502 provides an on-chip antenna for the integrated circuit. The processing circuitry for the antenna is not provided in the add-on portion, but in the IC portion, so the circuitry does not compete with the antenna for 20 space in the add-on portion, thus allowing the size of the antenna to be made larger. The portions may be fabricated in the same foundry or in different foundries and assembled subsequently.

In the IC portion 501, circuitry is formed on a substrate 503 having insulating, dielectric 504 layers and metal layers 505, 506 formed on respective dielectric layers 504. The metal layer 506 would usually be the top metal layer of the IC portion 501 in a typical construction. A passivation layer 510 is formed on the top metal layer 506 to protect the IC portion 501.

The add-on portion 502 comprises an add-on dielectric layer 512, which is typically the thickest layer of the wafer and is formed on the passivation layer 510. An add-on metal layer 513 is formed on the add-on dielectric layer 512 and an on-chip antenna 515 is formed in the same layer as the metal layer 513.

The thickness of the add-on dielectric layer 512 affects the power transfer rate of the on-chip antenna. A thicker add-on dielectric layer 512 provides a greater distance between the on-chip antenna 515 and the IC portion 501 leading to higher power transfer rate and a thickness greater than $5\mu\text{m}$ is preferred, most preferably in the range $5\text{-}20\mu\text{m}$.

Via-holes 516a and 516b are used to connect the on-chip antenna 515 with the IC portion 501. The via holes 516 a,b are filled with electrical conductive material, normally copper, connected to top pads 519 a,b and bottom pads 509 a,b. The top pads 519a and 519b are in the same metal layer 513 as is the antenna 515. The bottom pads 509a and 509b are in the top metal layer 506 of the IC portion 501.

A passivation layer 514 is formed on the add-on metal layer 513 to protect the die and circuitry. There is an open area 525 in the passivation layer 514 for exposure of a bond pad 521. The bond pad 521 is in the add-on metal layer 513 and is connected with the IC portion 501 through an electrical conductor formed from electrical conductive material, normally copper, disposed in via-hole 517 and bottom pad 509c.

The area of the top pads 519 and bottom pads 509 should preferably be as small as possible in order to avoid or reduce power dissipation. For this reason, these pads are smaller than conventional larger size pads such as pad 521 which is used for external connection to the IC. The relatively smaller size pads 509,519 are adequate for the internal connections between the IC and add-on portions.

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The integrated circuit 500 is provided with a guard ring. Two alternative types of guard ring are shown in Fig. 5, labelled 507 and 508 although it will be understood that only one or the other will be provided in any particular integrated circuit 500. Guard ring 507 is only formed in the IC portion 501; Guard ring 508 is formed in both the in IC portion 501 and add-on portion 502. Fig 5 shows the cross-section of guard ring 507, formed of three sub-rings in the three metal layers 505,506 and connected by electrical connections through three via-holes 507a between the metal layers. The guard ring 508 is formed in

of three sub-rings in the three metal layers 505,506 and is connected by electrical connections through three via-holes 508a and also by a sub-ring in add-on metal layer 520 connected to the other sub-rings by an electrical connection through via-hole 518 in the add-on dielectric layer 512. Guard ring 508 can protect the whole integrated circuit inclusive of the add-on portion 502. The number of sub-layers of the guard ring need not be three and can be one (in each portion in the case of ring 508) or more than one, provided the layers are electrically connected.

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FIG. 6 shows a general structure of a guard ring which is a second embodiment of the present invention. The guard ring structure to be explained can be used for all the sub-rings of either guard ring 507,508 in Figure 5. Fig. 6 is a plan view of a metal layer of an integrated circuit 601 showing a guard ring 602

15 disposed in a peripheral region. The guard ring 602 is composed of segments of metal 603 such as copper or any suitable metal/alloy having gap capacitors 604, 605 which are formed between the segments of metal 603. Capacitors 607 and diodes 608a and 608b are formed between adjacent ends of the segments 603 in an IC active area 610. A centre portion 606 of the active area 610 is the area in which the circuitry of the integrated circuitry lies. A feature of the guard ring 602 is that it is discontinuous, not being closed loop of metal, and thus does not produce large induced currents in response to magnetic flux. Consequently, the guard ring 602 does not degrade the performance of circuitry sensitive to such eddy currents such as an on-chip antenna.

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- As shown in Fig 6, the ends of each segment forming the guard ring 602 have extended digits (or finger-like extensions) which interleave with the digits of another segment (603, 609 for example) forming adjacent but non-contacting surfaces between which there will be capacitance under an applied voltage and form the gap capacitors 604, 605. The gap capacitors 605 are disposed along a side of the guard ring and the gap capacitors 604 at a corner of the guard ring 602. Either or both kinds of gap capacitors 604, 605 may be used.
- 10 An advantage of the gap capacitors is that surrounding magnetic flux does not produce an induced current inside the guard ring 602 since this is not a closed loop and can absorb transient current disturbance to a certain degree while preventing eddy currents and yet, at the same time, the guard ring protects the die from damage by invasion of foreign impurities or ionic contamination in the
- 15 manner of a conventional unbroken guard ring. Furthermore, a guard ring with such gap capacitors, especially if the gap capacitors are at the corner of the guard ring, can withstand greater shear forces and also can better prevent delamination of the passivation layer when undergoing temperature reliability tests than a conventional guard ring, due to broken segments of the guard ring,
- 20 since as the extent of shrinkage of metal and dielectric are different, shear stresses are applied on the metal layer resulting in the deformation of the metal layer, in the worst case, cracks in the metal layer and dielectric. As the metal of proposed guard ring is already "broken", which has more flexibility for displacement. As the expansibility of metal is different from dielectric, if the

metal at the corner is solid, the stresses applied on the corner metal come from two orthogonal directions. The area of the metal at the corner becomes larger than that of the dielectric when the temperature increases and result can be delamination of the corner metal if the shear stresses are strong enough. Again,
5 the gap between the ends of metal provides displacement flexibility to alleviate this.

FIG. 7 shows four gap capacitors, being two alternative designs 701,702;
703,704 of gap capacitors 604, 605 respectively. The gap capacitor 701 is an
10 interdigital capacitor formed at the corner of a guard ring. The gap capacitor 702 is a simple mitred gap that has a lower capacitance when a voltage is applied across it than the capacitor 701 which also provides a tortuous path for impurities or ionic contamination, but is cheaper and simpler to fabricate. The gap capacitor 703 is an interdigital capacitor formed in the middle of a guard
15 ring. The gap capacitor 704 is a simple end-to-end gap in the middle of a guard ring which has the same advantages and disadvantages as capacitor 702.

FIG. 8 is a three-dimensional view of a multi-layer interdigital gap capacitor 800. of conductive segments 802, 803 which are part of a guard ring are interleaved
20 in five metal layers 804 disposed between four intermediate dielectric (insulator) layers 806, the metal layers 804 being connected by via holes 805 filled with conductive material. . The fingers of each adjacent layer 804 are the reverse pattern of the next so the fingers 801 of the layers 804 are interdigitally

disposed both laterally and depth-wise. The multi layer guard ring can be manufactured by usual IC manufacturing processes.

In the event that a large current surges through the guard ring 602, the gap
5 capacitors 604,605 may breakdown resulting in damage of the guard ring. To prevent this, a pair of diodes 608a, 608b is connected between every two adjacent segments 603, 609 of the guard ring 602. The diodes are disposed with connected anodes to present in normal use an open circuit connection to current induced in any segment. The pair of diodes 608a, 608b behaves as a
10 high impedance device preventing any flow of current from one segment to the other under normal operating conditions, thus maintaining the open loop condition of the guard ring. When there is a power surge and the voltage across the pair of diodes is greater than the breakdown voltage of the diodes 608a, 608b, both the diodes 608a, 608b will allow the surge of current to flow through.
15 The pair of the diodes 608a, 608b becomes highly resistive as soon as current surge subsides. In other words, the guard ring 602 as a whole acts as a closed loop when there is large current surge in a high voltage condition.

The guard ring 602 also acts to reduce heat loss induced by a high frequency
20 current and the resultant counteractive magnetic flux. In the event that a voltage having a high frequency is induced in the guard ring, the gap capacitors become a low-resistive device which allows a current to flow inside the guard ring 602. At the same time, however, as the frequency is high, the segments behave as inductors. Thus, the segments and gap capacitors form a resonant

network of inductors and capacitors. The energy of an induced current is thus transferred between the gap capacitors and segments of metal instead of lost as emitted heat.

- 5 Where the integrated circuit is provided with an on-chip antenna, as the energy is transferred between the segments and the gap capacitors, some of the energy is received by the antenna (which in all likelihood induced a current in the guard ring to provide the energy in the first place). In this way, the guard ring 602 boosts antenna performance and, unlike guard rings in the prior art, is
10 not a load which consumes signal power.

To improve the performance of the guard ring 602 as a booster, the intrinsic resonant frequency of the guard ring 602 can be tuned to the working frequency of any on-chip antenna implemented in the IC chip by adjusting the size and the
15 number of gap capacitors. Additional capacitors can be connected in parallel to the gap capacitors to tune down the resonant frequency of the guard ring when the working frequency of the antenna is very low. FIG.6 shows an example of how the additional capacitors 607 shown in Fig 6 provide this function.

Additional tuning can be performed by varying the L characteristics of the guard
20 ring segments.

FIG. 9 shows a circuit 901 equivalent to the guard ring 602 under high frequency induction (with minimal resistance R ignored in this simple model). The inductor 902 is the equivalent device of a guard ring segments (603, 609

for example) and the capacitor 903 is the equivalent device of gap capacitors 604,605, additional capacitors 607 and diodes pairs 608 a,b.

FIG. 10 shows an equivalent circuit 1000 of an IC chip having a guard ring

5 1001 to demonstrate the boost effect of the guard ring.. A power source 1005 is connected to a source antenna 1004, such as an external scanner antenna in RFID. A load 1003, for example a TAG circuit in RFID receives energy from source antenna 1004 via a receiving on-chip antenna 1002, as well as from the guard ring 1001 to feed load 1003.

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FIG. 11 is a plan view of an antenna layer of a third embodiment of an integrated circuit, designated 1101 having the general structure of the embodiment of Figure 5 and a guard ring 1102 of the structure shown in Fig. 6, being a sub-ring of the guard ring structure 508 of Fig. 5, surrounding two

15 antenna coils 1103, 1107. The antenna coils 1103, 1107 are formed on an add-on layer and therefore do not compete for area with the chip circuitry which is disposed below. A contact 1105 of antenna 1103, having a relatively small area, is connected with the circuitry of the IC portion 501. A contact 1104, having a large area, is connected either to the circuitry in the IC portion 501 or to an

20 external antenna (not shown) to further enhance power transfer. A contact 1106, shown at the lower left corner, is a bond pad connecting to the circuitry in the IC portion 501.

FIG. 12 is a plan semi-transparent view similar to Fig. 11 of a fourth embodiment, designated 1200 of an integrated circuit 1201 with a guard ring 1202 having an octagonal antenna coil 1203. The octagonal antenna coil 1203 is laid on two add-on metallic layers, one on top of the other and therefore does not compete for valuable active area with the chip circuitry. Tracks 1203 and 1204 are in different metallic layers that are connected by electrical connections through via-holes.

The cross sectional structure of the embodiment of Figure 12 is shown in Fig. 13, where similar components are given the same reference numerals as in Fig. 5 with the addition of 800. Additionally, the add-on portion has two add-on layers 1311a, 1313 and two add-on dielectric layers 1312, 1311b. The add-on dielectric layer 1311b need not be a thicker layer like the layer 1312.

Via-holes 1320 filled with conductive material are used to connect the two add-on metal layers 1311a and 1313 electrically and the octagonal antenna can be formed in add-on metal layers 1311a and 1313.

The octagonal antenna can also be formed in one add-on metal layer in the add-on portion and in the top metal layer in IC portion. With such a structure in order to prevent performance degradation, the proportion of the antenna on the top metal layer is minimized, for example restricting this to the antenna track portion at the point where the track crosses over itself.

An advantage of this embodiment is that the antenna can be directly connected to a differential circuit in the integrated circuit portion 501 upon which the add on portions are disposed, in the manner of the embodiment of Fig. 5. In such a case, the contacts 1205 and 1206 can be used as a pair of differential contacts that can be used with a differential circuit laid in the IC portion 501. Any point in the antenna tracks 1203, 1204 such as point 1207, can be used as an additional contact if more than one signal contact port, such as a signal ground port, is needed.

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In RFID, there are two components, the tag and the scanner, with the scanner reading the identity of the tag in a contactless manner by RF transmission/reception. The on-chip aerial described is for use with the tag, of which it forms part. In such an application, the tag circuitry would be provided on the IC portion.

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The RF field of the coil antenna decreases rapidly if the distance normal to the plane of the antenna exceeds a threshold value. The power transfer rate is also sensitive to the space between two corresponding antennae. To improve the power transfer rate, particularly (but not exclusively) for an RFID application, three further embodiments of the present invention will now be described with reference to Figs. 14 to 16. In these embodiments, the central antenna is the on-chip antenna and in the case of an RFID application, forms part of the tag,

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as noted above,, with the surrounding antenna structure in each case being connected to an RFID scanner.

FIG. 14 shows two in-phase antenna coils 1401 and 1402 and another antenna
5 coil 1403 arranged to form a sandwich structure as shown. A port 1404 is used to feed or receive a signal from the two in-phase antennae. Another port 1405 is used to feed or receive a signal from the antenna 1403. With the sandwich structure, due to the interaction between the two in-phase antennae, more energy is collected and the field between the two in-phase antennae becomes
10 more uniform. The performance of the antenna 1405 is also insensitive to position due to the compensative magnetic flux distribution of the in-phase antennae leading to small ripples in the field along axis A upon which the antenna 1405 is disposed.

15 FIG. 15 shows a further embodiment with one antenna coil replaced by a disc of high permeability μ material 1502 such as ferrite . A high μ material disc 1502 is placed opposite to antenna 1501. Antenna 1503 is inserted in the gap between the antenna 1501 and the high μ material disc 1502 forming a sandwich structure. The magnetic flux can be concentrated in the high μ material so that
20 the magnetic field strength is enhanced. As a result, the power transfer rate is improved. The ports 1504, 1505 are the feeding ports of antennae 1501, 1503 respectively

FIG. 16 shows another embodiment 1600 an open loop 1606 of high μ material such as ferrite is placed around and opposite a first antenna 1603. One end 1605 of the loop has a disc 1608 inserted into the centre of a first antenna ; the other end has a disc 1607 positioned opposite the first antenna 1601. Magnetic
5 flux flows from the first antenna 1601 to a second antenna 1602 flows through the disc 1607, the loop 1606 and the disc 1608 and back to the first antenna 1601. The energy is thus focused around antenna 1602 because of the high μ material loop 1606. The coupling between antenna 1601 and 1602 is thus increased that the efficiency of the antenna system is improved. The ports
10 1603, 1604 are the feeding ports of antennae 1601, 1602 respectively.

It should be understood that the embodiments described herein are but
15 embodiments of underlying concepts of the invention. Alternatives to the embodiments, though not described, are intended to be within in the scope of this invention as claimed. For example, the ends forming the gap capacitors may be of any form. Where these are inter-engaging, the elements need not be fingers but any other inter-engaging shapes such as inter-engaging triangles or
20 arcuate portions.; The inter-engaging portions need not correspond one to the shape of the other and may comprise only a single portion on each segment. The material of the segments forming the guard ring may not be a metal, as long as the material exhibits the necessary properties for example, polycrystalline silicon may be used. The capacitors 607 and diode pairs 608

may be placed in layers above or underneath the gap capacitors 605 and not necessarily alongside the gap capacitors 605 and the diode pairs may be arranged with their cathodes connected rather than their anodes. Other PN junction devices such as varactors, bipolar junction transistors, or Metal Oxide

5 Semiconductor Field Effect Transistors may be used instead of diodes.

Furthermore, the guard ring may be of any discontinuous form and may be a single segment, with the gap capacitor formed between free ends of the segment. The segment may be of spiral form and may have ends wider than the main body of the segment, to increase capacitative effect. The segments

10 may also be placed in a plurality of nested rings, with each ring having one or more segments.

Claims

1. An integrated circuit antenna device having an antenna and processing circuitry therefor, the antenna and circuitry being formed on separate layers
5 of the integrated circuit.
2. A device as claimed in claim 1 wherein the integrated circuit includes a plurality of insulating layers and a plurality of conductive layers and the antenna is separated from the circuitry by an insulating layer thicker than the conductive layers and other insulating layers.
- 10 3. A device as claimed in claim 1 wherein the antenna is separated from the circuitry by an insulating layer of at least $5\mu\text{m}$ thickness.
4. A device as claimed in claim 3 wherein the antenna is separated from the circuitry by an insulating layer of a thickness in the range $5\mu\text{m}$ to $20\mu\text{m}$.
5. A device as claimed in any one of the preceding claims wherein the antenna
15 and circuitry are formed as separate portions of the integrated circuit.
6. A device as claimed in any one of the preceding claims further comprising an electrical connection between layers of the integrated circuit, the electrical connection being provided with pads at each end, a first pad being arranged to receive a connection to a device external to the integrated
20 circuit and a second pad arranged for internal connection within the integrated circuit and wherein said first pad is larger than said second pad.
7. A device as claimed in claim 6 further comprising at least one further electrical connection arranged for internal connection between two layers

within the integrated circuit and having further pads at each end and wherein the further pads are smaller than the first pad.

8. A device as claimed in any one of the preceding claims wherein the aerial is formed on more than one layer of the integrated circuit.

5 9. A device as claimed in any one of the preceding claims further comprising a conductive guard ring disposed on a layer of the integrated circuit.

10. A device as claimed in claim 9 wherein the guard ring is discontinuous.

11. A device as claimed in claim 9 or claim 10 wherein the guard ring has two ends and a gap therebetween

10 12. A device as claimed in claim 11 wherein the gap is not straight.

13. A device as claimed in claim 11 or claim 12 wherein the ends have inter-engaging portions.

14. A device as claimed in claim 13 wherein the portions each comprise at least one elongate finger.

15 15. A device as claimed in any one of claims 11 to 14 wherein a capacitor is disposed across the gap.

16. A device as claimed in any one of claims 11 to 15 wherein a high voltage breakdown circuit is disposed across the gap.

17. A device as claimed in any one of claims 11 to 16 wherein the guard ring
20 has a corner and the gap is disposed at the corner.

18. A device as claimed in any one of claims 11 to 17 wherein the guard ring is formed from a plurality of conductive layers.

19. A device as claimed in claim 18 wherein each layer is separated from the next by an insulation layer.

20. A device as claimed in any one of claims 10 to 19 wherein the inductance of the ring and the capacitance across the gap are such as to form an energy storage network.
21. A device as claimed in claim 20 wherein the resonant frequency of the
5 network is tuned to a working frequency of the antenna.
22. A device as claimed in any one of claims 11 to 19 wherein the guard ring is formed as a plurality of conductive segments, adjacent segments each having a said pair of ends and a said gap therebetween.
23. A device as claimed in any one of claims 11 to 22 wherein the guard ring is
10 disposed on the same layer as the aerial.
24. A device as claimed in any one of claims 11 to 22 further comprising at least one further guard ring, the guard rings being disposed on respective layers of the integrated circuit.
25. A device as claimed in claim 24 wherein the guard rings are electrically
15 connected.
26. A device as claimed in claim 24 or 25 wherein the guard rings are disposed on the same layers as the aerial, the processing circuitry or both.
27. A device as claimed in claim 10 wherein the guard ring is of spiral topology.
28. An integrated circuit comprising a circuit component and a guard ring around
20 the component wherein the guard ring has first and second ends and a gap therebetween.
29. A device as claimed in claim 28 wherein the gap is not straight.
30. A device as claimed in claim 28 or claim 29 wherein the ends have inter-engaging portions.

31. A device as claimed in claim 30 wherein the portions each comprise at least one elongate finger.
32. A device as claimed in any one of claims 28 to 31 wherein a capacitor is disposed across the gap.
- 5 33. A device as claimed in any one of claims 28 to 32 wherein a high voltage breakdown circuit is disposed across the gap.
34. A device as claimed in any one of claims 28 to 33 wherein the guard ring has a corner and the gap is disposed at the corner.
35. A device as claimed in any one of claims 28 to 34 wherein the guard ring is
10 formed from a plurality of conductive layers.
36. A device as claimed in claim 35 wherein the conductive layers are separated by insulation layers.
37. A device as claimed in any one of claims 28 to 36 wherein the guard ring is formed as a plurality of conductive segments, adjacent segments each
15 having a said pair of ends and a said gap therebetween.
38. A device as claimed in any one of claims 28 to 37 wherein the component comprises an aerial.
39. A device as claimed in any one of claims 28 to 37 further comprising at least one further guard ring, the guard rings being disposed on respective layers
20 of the integrated circuit.
40. A device as claimed in claim 30 wherein the guard rings are electrically connected.
41. An integrated circuit device having a plurality of layers, an electrical connection between two said layers of the integrated circuit, the electrical

connection being provided with pads at each end, a first pad being arranged to receive a connection to a device external to the integrated circuit and a second pad arranged for internal connection within the integrated circuit and wherein said first pad is larger than said second pad.

- 5 42. A device as claimed in claim 41 further comprising at least one further electrical connection arranged for internal connection between two said layers within the integrated circuit and having further pads at each end and wherein the further pads are smaller than the first pad.

43. A guard ring for an integrated circuit, the guard ring being arranged to form
10 an energy storage device.

44. A guard ring as claimed in claim 43 comprising at least one inductor and at least one capacitor connected together to form the ring.

45. A guard ring as claimed in claim 44 wherein the at least one inductor and at least one capacitor are tuned to a resonant frequency.

- 15 46. A guard ring as claimed in claim 45 provided adjacent an antenna, the antenna having an operating frequency to which the resonant frequency is tuned.

47. In combination a device as claimed in any one of claims 1 to 27 disposed between two in phase further antennae.

- 20 48. In combination a device as claimed in any one of claims 1 to 27 disposed between a further antenna and a high magnetic permeability element.

49. In combination a device as claimed in any one of claims 1 to 27, a further antenna disposed on one side of the device and an open loop of high

magnetic permeability material extending from the further antenna to the opposed side of the device.

50. A guard ring for an integrated circuit, wherein the guard ring is discontinuous.

5 51. A guard ring as claimed in claim 50 having first and second ends and a gap formed there between.

52. A guard ring as claimed in claim 50 or claim 51, of spiral topology.

53. An RFID device including a device, guard ring or combination as claimed in any one of the preceding claims.

10 54. An RFID tag including a device as claimed in any one of claims 1 to 46

55. A combination as claimed in any one of claims 47 to 49 wherein the device is connected to a RFID tag

56. A combination as claimed in any one of claims 47 to 49 or 55 wherein the further antenna is connected to an RFID scanner.